MAXIM

1992 NEW RELEASES DATA BOOK

Featuring:

- ***"HOT" Product Features***
- ***Data Sheets***
- ***Application Notes***
- ***Free Sample Request Cards***

1992 ANALOG DESIGN GUIDE SERIES
Book 1

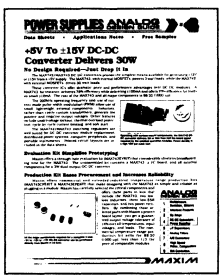
HOW TO USE THE 1992 NEW RELEASES DATA BOOK

Maxim's 1992 New Releases Book brings together over 150 new products from 10 product groups in a single, easy-to-use "Design Guide" format. Each product group section contains: (1) A brief overview of key products and pricing information; (2) Data sheets for all products in the group (3) Application notes using group products in a variety of ways to solve commercial and industrial design problems.

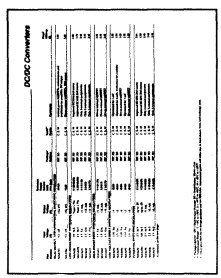
If, after reviewing this information, you need specific samples for further evaluation, all you need to do is fill out one of the sample request cards at the front of the book and send it to Maxim for prompt fulfillment.

There are several ways to locate a specific product or product group:

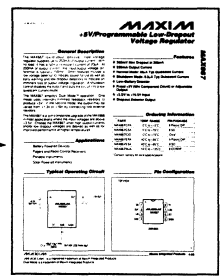
1	Multiplexers, Switches, Military
2	Interface Products
3	Op Amps
4	DC-DC Converters, Power Supplies
5	µP Supervisory
6	Analog Filters
7	A/D Converters
8	High Speed: Video, Comparators
9	D/A Converters



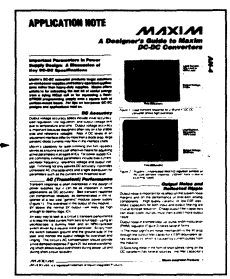
OVERVIEW



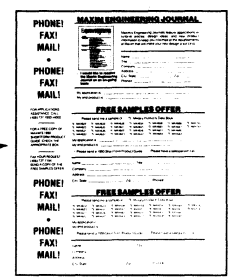
PRICING



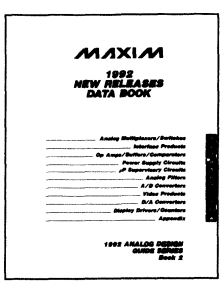
DATA SHEETS



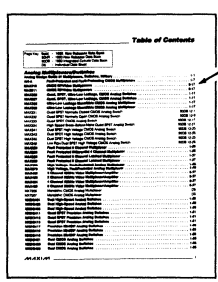
APP NOTES



FREE SAMPLES



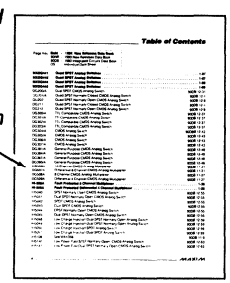
LOCATE PRODUCT SECTIONS BY TAB NUMBER



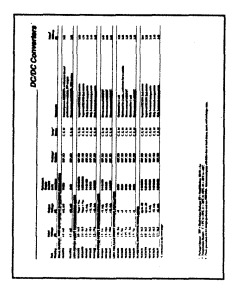
MAXIM PART NUMBER INDEX

*Data sheets included in this book indicated in **bold** face*

Cross reference to data sheets on Maxim parts not included in this book



ALPHA-NUMERIC PART INDEX CROSS REFERENCED TO OTHER MAXIM BOOKS



SELECTION TABLES WITH SPECS, COMMENTS, PRICING

MAXIM

1992 NEW RELEASES DATA BOOK

1992 ANALOG DESIGN GUIDE SERIES Book 1

Introduction

Maxim Integrated Products designs, develops, manufactures and markets a broad range of linear and mixed-signal integrated products for use in a variety of electronic products. These products "connect" the real (analog) world to the digital world. They detect, measure, amplify and convert real world signals, such as temperature, pressure or sound, into digital signals a computer can process. Over the past eight years, Maxim has introduced over 430 products - more analog ICs than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. The Company's products include: data converters and references, RS-232 interface circuits, amplifiers, power control circuits, timers and counters, display circuits, multiplexers and switches, voltage detectors and filters. Recognizing the growing demand for CMOS, the emerging technology of the future, Maxim has focused increasingly on CMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

New Releases

During the past year more than 70 new products have been added to our product lines. These, and other older but unique Maxim products, are collected into a single volume in this new data book. We hope that this enables you to have quick access to "what is new and exciting from Maxim". Older products, and some recently introduced second-source products are left out of this book, but can be located using the Table of Contents or the Index. You can get data sheets for these products by contacting your local Sales Representative, or the factory directly.

Customer Service

Customer Service Representatives are available during normal business hours to provide you with information on orders placed directly with the factory or by any of our franchised distributors. Please see the Appendix for a list of domestic and international sales representatives, and distributors.

Technical Support

The technical literature in this volume discusses the operation and applications of Maxim products as they apply to design problems. In addition to the individual data sheets/applications notes in this book, Maxim offers a full line *Integrated Circuits Data Book*, a *Military Products Data Book*, and a free subscription to the *Maxim Engineering Journal* - a quarterly magazine covering the application of Maxim analog ICs. For on-line technical support you can talk with a senior applications engineer at (408) 737-7600 extension 4000 or, after normal business hours, you can FAX in your questions at (408) 736-1831.

Reliability

Providing reliable, innovative analog ICs that solve customer problems is the cornerstone of Maxim's existence. Our programs offering free burn-in at 150°C (for all DIPs) and complete lot traceability, life test and pressure pot qualification are unique in the industry.

On July 1, 1988, Maxim became a certified manufacturer of MIL-STD-883 Class B, Rev. C products. To date, the company has announced over 167 of its 430 products screened to military standards, 40 are in qualification and more are scheduled for qualification in the future.

All of Maxim's products are available screened to a "High Reliability" flow that emulates Rev. C, MIL-STD-883, Class B standards. These "/HR" parts are fully tested over the military temperature range and are sold at significantly lower prices than /883 compliant products.

Following Maxim's charter to provide analog solutions in silicon, we will continue to offer /883B Rev. C and /HR devices, SMDs (Standard Military Drawings) when available and SCDs (Customer Source Control Drawings) in the future. We welcome you to visit our new facilities for a first hand inspection and look forward to the opportunity to serve you. Contact your local Sales Representative or the factory directly, (408) 737-7600 extension 6283, for more information.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.
4,700,286, 4,679,134, 4,636,930, 4,859,963, 4,857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577, 4,859,963, 4,999,761, 4752700.

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90DB - 1990 Integrated Circuits Data Book
DS - Individual Data Sheet

Analog Multiplexers/Switches

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Interface Products

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Op Amps/Buffers/Comparators

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Power-Supply Circuits

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DS - Individual Data Sheet

Appendix

MAXIM

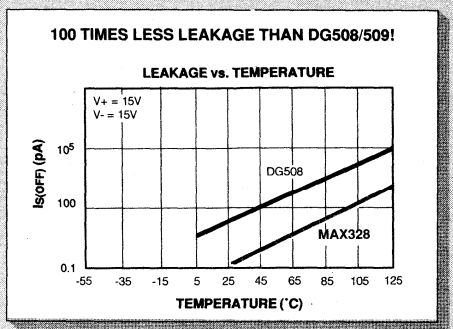
Analog Multiplexers/Switches

1pA Muxes & Switches Reduce Errors from High-Impedance Sources

Add 110V AC Fault Protection with External 40kΩ Resistors

For data-acquisition systems that require up to 16-bits accuracy over temperature, the MAX326/MAX327 CMOS switches and MAX328/MAX329 CMOS multiplexers (muxes) offer 1pA typical leakage currents—at least 10 times lower than any other analog switch or mux available today. Low leakage improves system accuracy by reducing the voltage error across source impedances and on-resistances. It also allows the use of high-value input resistors to protect against input overvoltage—40kΩ protects against 110V AC faults while adding only 40nV of error with 1pA input leakages. In addition, 2pC charge injection is 3 times lower than other available multiplexers.

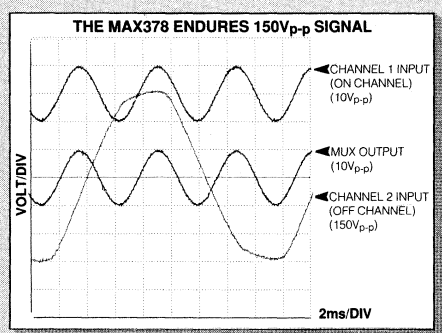
And to lower system costs while allowing maximum design flexibility, the MAX326/MAX327 operate from both single (+10V to +30V) and dual (±5V to ±18V) power supplies.



The MAX328/329 typically have less than 1pA leakage at +25°C.

Muxes Withstand ±75V Fault Voltages

Only Nanoamperes of Input Current Under All Fault Conditions



To demonstrate the ruggedness of the MAX378, an off channel (CH2) is overdriven with a 150Vp-p AC signal. This channel survives, and the adjacent on channel (CH1) is unaffected during this abuse.

If your data-acquisition system requires protection against power-supply shutdown and/or overvoltage signals on both input and output pins, Maxim's new MAX378 and MAX379 multiplexers (muxes) are the solution. They withstand overvoltages of ±60V while operating, or ±75V with the power supplies off.

The MAX378 is an 8-channel, single-ended mux; the MAX379 is a 4-channel, differential mux.

These muxes feature a series N-channel/P-channel/N-channel MOSFET structure that provides additional fault protection. If the supplies are turned off while input voltages are still present, all input channels turn off, resulting in mere nano-amperes of input leakage current. Less than 2nA leakage during overvoltage means that "on" channels are unaffected by overdrawn "off" channels and can still be measured. The Maxim switch structure not only protects itself, it protects downstream circuitry and upstream signal sources as well.

Maxim's Military Program

Maxim's MIL-STD-883 (/883) program tests the devices per Method 5004 and performs Quality Conformance Inspection per Method 5005, Groups A, B, C, and D. As a result, Maxim's /883 products comply fully with paragraph 1.2.1 of MIL-STD-883.

For complete electrical specifications on the available /883-compliant products, use the enclosed response card to request Maxim's *Military Products Data Book.*

Parts currently /883 compliant:

MAX154AMRG	MX7521UQ
MAX154BMRG	MX7521TQ
MAX158AMJI	MX7521SQ
MAX158BMJI	MX7524UQ
MAX160MJN	MX7524TQ
MAX162CMRG	MX7524SQ
MAX231MJD	MX7528UQ
MAX232MJE	MX7528TQ
MAX232MLP	MX7528SQ
MAX233MJP	MX7533UQ
MAX674MJA	MX7533TQ
MAX674MTV	MX7533SQ
MAX675MTV	MX7541SQ
MAX675MJA	MX7541TQ
MAX8211MJA	MX7541ASQ
MAX8211MTV	MX7541ATQ
MAX8212MJA	MX7542GTQ
MAX8212MTV	MX7542TQ
MX580SH	MX7542SQ
MX580TH	MX7572SQ05
MX580UH	MX7572SQ12
MX581TH	MX7824UQ
MX581SH	MX7824TQ
MX584TH	MX7828UQ
MX584SH	MX7828TQ
MX584TE	REF01AJ
MX584SE	REF01AZ
MX7225UQ	REF01J
MX7225TQ	REF01Z
MX7226TQ	REF02AJ
MX7520UQ	REF02AZ
MX7520TQ	REF02J
MX7520SQ	REF02Z

Parts currently under /883 qualification:

DG200AAA	MAX310MJE
DG200AAK	MAX311MJE
DG201AAK	MAX333MJP
DG202AK	MAX334MJE
DG300AAA	MAX358MJE
DG300AAK	MAX359MJE
DG301AAA	MAX543BMJA
DG301AAK	MAX663MJA
DG302AAK	MAX690MJA
DG303AAK	MAX691MJE/MLP
DG304AAA	MAX692MJA
DG304AAK	MAX693MJE/MLP
DG305AAA	MAX694MJA
DG305AAK	MAX695MJE
DG306AAK	MAX696MJE
DG307AAK	MAX697MJE
DG381AAA	MAX7645AM/BMJP
DG381AAK	MAX8211MTV
DG384AAK	MAX8212MTV
DG387AAA	MX536A
DG387AAK	MX574A
DG390AAK	MX7224
DG506AAK	MX7543
DG507AAK	MX7545
DG508AAK	MX7548
DG509AAK	MX7574
DG528AK	MX7574
DG529AK	MX7628
IH6108MJE	OP07AJ
IH6208MJE	OP07AZ
IH6116MJI	OP07J
IH6216MJI	OP07Z
MAX170BMJA	

DESC approved devices to Standard Military Drawings (SMDs) currently available:

SMDs	MAXIM P/N	SMDs	MAXIM P/N
5962-8987701EA	MAX232MJE	5962-8876401LA	MX7824TQ
5962-89877012C	MAX232MLP	5962-8876402LA	MX7824UQ
8551401GC	REF02AJ	5962-8876403XA	MX7828TQ
8551401PA	REF02AZ	5962-8876404XA	MX7828UQ
5962-8958101GC	REF01AJ	5962-8759101LA	MX7572SQ12
5962-8958101PA	REF01AZ	5962-8759102LA	MX7572TQ12
5962-8958102GC	REF01J	5962-8759104LA	MX7572SQ05
5962-8958102PA	REF01Z	5962-8759105LA	MX7572TQ05
5962-8948101VA	MX7541ASQ	5962-8961603VA	MX7574TQ
5962-89481012C	MX7541ASE	5962-89616032C	MX7574TE
5962-8948102VA	MX7541ATQ	5962-8961604VA	MX7574SQ
5962-89481022C	MX7541ATE	5962-89616042C	MX7574SE

★ FUTURE PRODUCTS ★

MAX388/389 High-Voltage, Fault-Protected Muxes with Latches

Features:

- ♦ ±75V Max Overvoltage Protection with Supplies Off; ±60V Max with Supplies On
- ♦ Internal Channel-Address Latches
- ♦ All Channels Turn Off When Power Supplies are Off
- ♦ No Supply-Current Increase During Fault Conditions
- ♦ Only Nanoamperes of Input Current Under All Fault Conditions
- ♦ Operate From ±4.5V to ±18V Supplies
- ♦ Latchup-Proof Construction

MXDG400 Family

In July 1991, Maxim will begin the introduction of 18 new analog switches and multiplexers. (See the following pages for a complete list of products and their key specifications.)

The MXDG400 family features low leakage (0.25nA max, MXDG401-425) and fast switching speeds ($t_{(OFF)}$ = 100ns max, MXDG401-405), offering greater accuracy at a price comparable to previous generations. Extremely-low charge injection (1pC typ, MXDG441/442) minimizes signal distortion, while low on-resistance (35Ω max, MXDG401-425) reduces signal error, for increased performance and reliability. Many devices can also operate from single supplies for application in battery-powered systems. And Maxim's wide range of package options will include skinny DIP and small outline for surface-mount applications.

Part Number	Function	Plug-In Upgrade for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Price† 1000-up ($)
MAX326	4 SPST NO	DG201A/211	2500	0.01	1000	500	0.8/2.4	0.25/0.1	3.63
MAX327	4 SPST NC	DG202/212	2500	0.01	1000	500	0.8/2.4	0.25/0.1	3.63
MAX331	4 SPST NC	DG201A/211	175	1	600	450	0.8/2.4	0.01/0.01	6.73
MAX332	4 SPST NO	DG202/212	175	1	600	450	0.8/2.4	0.01/0.01	6.73
MAX333	4 SPDT	DG211& DG212 Pair	175	5	1000	500	0.8/2.4	0.25/0.25	4.47
MAX334	4 SPST NC	DG201A/211	50	1	100	50	0.8/3.0		3.20
MXDG401	2 SPST NO	IH5041	35	0.25	150	100	0.8/2.4	0.001/0.001	††
MXDG403	2 SPDT	IH5043	35	0.25	150	100	0.8/2.4	0.001/0.001	††
MXDG405	2 DPST NO	IH5045	35	0.25	150	100	0.8/2.4	0.001/0.001	††
MXDG411	4 SPST NC	DG201A-2/211-12	35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG412	4 SPST NO	DG201A-2/211-12	35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG413	4 SPST		35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG417	SPST NC		35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG418	SPST NO		35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG419	SPDT		35	0.25	175	145	0.8/2.4	0.001/0.001	††
MXDG421	2 SPST NO (latches)		35	0.25	250	200	0.8/2.4	0.001/0.001	††
MXDG423	2 SPDT (latches)		35	0.25	250	200	0.8/2.4	0.001/0.001	††
MXDG425	2 DPST (latches)		35	0.25	250	200	0.8/2.4	0.001/0.001	††
MXDG441	4 SPST NC	DG201A/202	80	0.5	250	120	0.8/2.4	0.1/0.001	††
MXDG442	4 SPST NO	DG201A/202	80	0.5	250	120	0.8/2.4	0.1/0.001	††
MXDG444	4 SPST NC	DG211/212	85	0.5	250	120	0.8/2.4	0.001/0.001	††
MXDG445	4 SPST NO	DG211/212	85	0.5	250	120	0.8/2.4	0.001/0.001	††
DG200A	2 SPST NC	DG200A	70	2	1000	500	0.8/2.4	0.3/0.01	1.78
DG201A	4 SPST NC	DG201A	175	1	600	450	0.8/2.4	0.1/0.1	1.97
DG202	4 SPST NO	DG202	175	1	600	450	0.8/2.4	0.1/0.1	2.21
DG211	4 SPST NC	DG211	175	5	1000	500	0.8/2.4	0.1/0.1	1.47
DG212	4 SPST NO	DG212	175	5	1000	500	0.8/2.4	0.1/0.1	1.47
DG300A	2 SPST NC	DG300A	50	1	300	250	0.8/4.0	0.5/0.1	2.15
DG301A	SPDT	DG301A	50	1	300	250	0.8/4.0	0.1/0.1	2.15
DG302A	2 DPST NC	DG302A	50	1	300	250	0.8/4.0	0.1/0.1	2.78
DG303A	2 SPDT	DG303A	50	1	300	250	0.8/4.0	0.1/0.1	2.78

–Continued on the next page–

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

Analog Switches (continued)

Part Number	Function	Plug-In Upgrade for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Price† 1000-up ($)
DG304A	2 SPST NC	DG304A	50	1	250	150	3.5/11	0.1/0.1	2.42
DG305A	SPDT	DG305A	50	1	250	150	3.5/11	0.1/0.1	2.55
DG306A	2 DPST NC	DG306A	50	1	250	150	3.5/11	0.1/0.1	4.06
DG307A	2 SPDT	DG307A	50	1	250	150	3.5/11	0.1/0.1	2.78
DG308A	SPST NO	DG308A	100	1	200	150	3.1/11	0.1/0.1	2.16
DG309	SPST NC	DG309	100	1	200	150	3.5/11	0.1/0.1	2.16
HI201	4 SPST NO	HI201	70	5	400	300	0.8/2.4	0.3/0.1	2.00
DG381A	2 SPST NO	DG381A	50	1	300	250	0.8/4.0	0.1/0.1	3.24
DG384A	2 DPDT NC	DG384A	50	1	300	250	0.8/4.0	0.1/0.1	4.06
DG387A	SPDT	DG387A	50	1	300	250	0.8/4.0	0.1/0.1	3.24
DG390A	2 SPDT	DG390A	50	1	300	250	0.8/4.0	0.1/0.1	3.26
IH5041	2 SPST NC	IH5041	75	1	400	200	0.8/2.4	0.001/0.001	1.84
IH5043	2 SPDT	IH5043	75	1	400	200	0.8/2.4	0.001/0.001	2.36
IH5045	2 DPST NC	IH5045	75	1	400	200	0.8/2.4	0.001/0.001	2.44
IH5047	2 DPST NC	IH5045	75	1	400	200	0.8/2.4	0.001/0.001	2.44

Analog Multiplexers

Part Number	Function	Plug-In Upgrade for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX328	1-of-8	DG508	2500	0.02	1	±15	Ultra-low leakage	4.72
MAX329	2-of-8	DG509	2500	0.02	1	±15	Ultra-low leakage	4.72
MAX358	1-of-8	DG508, HI508A	1500	1.0	.5	-12.5 to +13.5	Fault protected to ±35V	5.48
MAX359	2-of-8	DG509, HI509A	1500	1.0	.5	-12.5 to +13.5	Fault protected to ±35V	5.48
MAX368	1-of-8	DG528	1500	2	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	6.36
MAX369	2-of-8	DG529	1500	1.0	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	6.36
MAX378	1-of-8	DG508, HI508A	3000	1.0	.75/.5	-12.5 to +13.5	Fault protected to ±75V	11.31
MAX379	2-of-8	DG509, HI509A	3000	1.0	.75/.5	-12.5 to +13.5	Fault protected to ±75V	11.31
MAX388	1-of-8	DG528	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±35V	13.54
MAX389	2-of-8	DG529	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±35V	13.54

–Continued on the next page–

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Analog Multiplexers (continued)

Part Number	Function	Plug-In Upgrade for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MX7501	1-of-8	AD7501	300	5	1.5/1.0	±15	Plug-in replacement for AD7501	5.00
MX7502	2-of-8	AD7502	300	3	1.5/1.0	±15	Plug-in replacement for AD7502	5.00
MX7503	1-of-8	AD7503	300	5	1.5/1.0	±15	Plug-in replacement for AD7503	5.00
MX7506	1-of-16	AD7506	400	5	1.5/1	±15	Plug-in replacement for AD7506	9.20
MX7507	2-of-16	AD7507	400	5	1.5/1	±15	Plug-in replacement for AD7507	9.20
MXDG406	1-of-16	DG506A	100	2	.2/.15	±15	Plug-in replacement for DG506A	††
MXDG407	2-of-16	DG507A	100	2	.2/.15	±15	Plug-in replacement for DG507A	††
MXDG408	1-of-8	DG508A	100	0.5	0.150	±15	Plug-in replacement for DG508A	††
MXDG409	2-of-8	DG509A	100	0.5	0.150	±15	Plug-in replacement for DG509A	††
DG506A	1-of-16	DG506A	400	5	1/.4 (typ)	±15	Industry standard	5.63
DG507A	2-of-16	DG507A	400	5	1/.4 (typ)	±15	Industry standard	5.57
DG508A	1-of-8	DG508A	300	2	1/1.7	±15	Industry standard	3.23
DG509A	2-of-8	DG509A	300	2	1/1.7	±15	Industry standard	3.23
DG528	1-of-8	DG528	400	10	1.5	±15	Industry standard	3.57
DG529	2-of-8	DG529	400	10	1.5	±15	Industry standard	3.57
HI508A	1-of-8	HI508A	1500	2	.5	-12.5 to +13.5	Fault protected	5.88
HI509A	2-of-8	HI509A	1500	2	.5	-12.5 to +13.5	Fault protected	5.88
IH5108	Use MAX358							
IH5208	Use MAX359							
IH6108	Use DG508A							
IH6208	Use DG509A							
IH6116	Use DG506A							
IH6216	Use DG507A							
HI506	Use DG506A							
HI507	Use DG507A							
HI508	Use DG508A							
HI509	Use DG509A							

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

Fault-Protected and Fault-Protecting CMOS Multiplexers

Selecting an analog multiplexer (mux) for a measurement system involves more than just getting the pinouts and the number of channels right. Input signals (often imported from beyond the well-controlled world of the designer's printed circuit board) may sometimes exceed the supply voltages, and the supply voltages may be off (or on) at inopportune times. These conditions are called faults, and successful designs are "fault protected."

A suitable mux not only survives, but prospers in this environment. Its task is to switch the signals while protecting signal sources and the signals' destination. If the system involves redundancy (if the sources connect to several destinations simultaneously) the mux's task is compounded.

As an example, consider a hydraulic pressure transducer (strain-gauge bridge) in an aircraft, connected to a multiplexed alarm circuit and a multiplexed computer input. The typical strain gauge is a resistive bridge with 10V applied and produces 0 to 50mV across the differential bridge arms, approximately 5V above ground. The alarm circuit is fed by a mux that scans several such transducers, and it actuates when the differential voltage of any channel exceeds the preset value.

The same differential voltages feed an independent computer-driven mux that drives a cockpit display. Either mux must continue to operate if the other fails. Moreover, both must block the effect of a failed transducer, whose terminals can then source the full aircraft-battery voltage (28V). The alarm mux, computer mux, and transducers are interconnected by several connectors and many feet of unshielded wire, bundled in harnesses.

To further complicate the mux's job, a pilot can remove or apply power to any transducer during flight. And during maintenance, the connectors may be disconnected and reconnected while power to the various modules is either on or off. Because mux inputs tie directly to the connector pins, the mux must cope with harsh extremes of voltage:

- **High voltage with power off** - If one or more signal sources are energized while one mux is de-energized, that mux must not only avoid damage; it must also present high-impedance inputs that don't load the signal sources. It must maintain both forms of isolation whether power is on or off and during the transducer failure modes that apply 28V to its terminals.
- **High voltage with power on** - When a mux's inputs are exposed to voltages that exceed its supplies (typically ±15V), the mux must protect itself as well as the op amp or other circuit connected to its output. Two cases apply:
  - **High voltage on the selected channel** - The mux's inputs must not draw excessive current when voltage in the selected (on) channel exceeds the mux supply voltage. The mux also must limit V_{OUT} to a safe level under these conditions.
  - **High voltage at an off channel** - When voltage in excess of the supply is applied to an off channel, the mux must limit its input current while blocking feedthrough to the output.

A mux's protection can be included on chip or supplied externally. The traditional external scheme of Figure 1, for example, provides a current-limiting resistor and two shunt diodes for each channel (one channel shown). When a positive voltage at any input attempts to exceed the 12V zener voltage, the top diode turns on and clamps the mux input just above 12V. A similar mechanism handles negative inputs below -12V.

Though protection is excellent, the Figure 1 circuit uses discrete components. The method also places certain

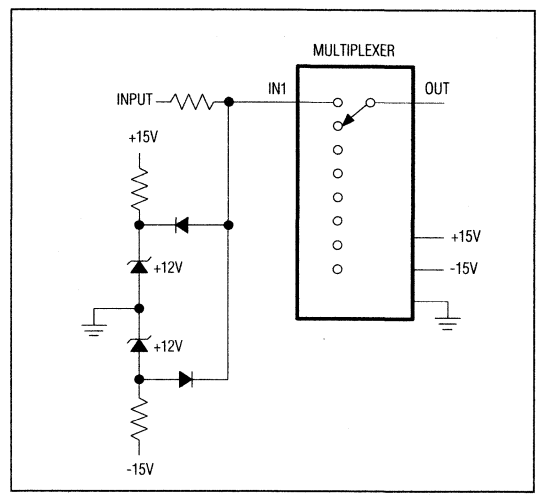


Figure 1. External Resistor/Diode Protection Circuit

Fault-Protected and Fault-Protecting CMOS Multiplexers

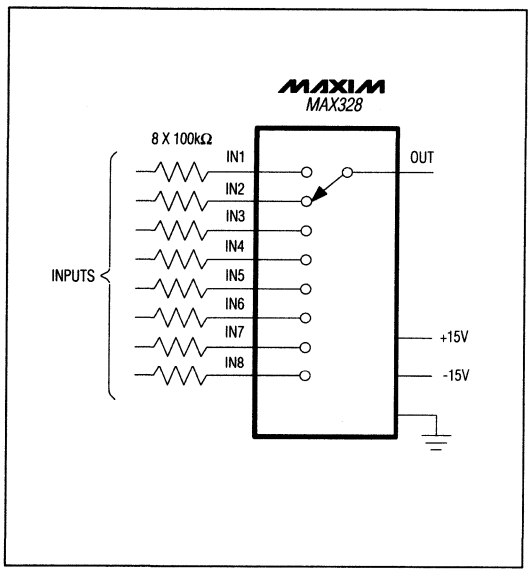


Figure 2. External-Resistor Protection

constraints on design, notably high current during fault conditions and diode-contributed leakage currents in the signal paths during normal operation. If this circuit were operating in the aircraft system, fault currents resulting from the turn-off of one mux would completely disrupt signals at the other mux.

A variation of the Figure 1 approach employs PN junctions inherent in the CMOS multiplexer chip in place of the external diodes, and adds an external resistor to each channel as before (Figure 2). The resistor value must provide adequate protection, but too high a value allows unacceptable voltage errors due to leakage current from the mux, especially at high temperatures.

Lower-value resistors minimize the error, but they also allow higher fault currents and may not provide adequate protection. (One manufacturer recommends low-valued resistors that allow high fault currents, but lets the user discover that the chip's power-dissipation limit won't allow simultaneous protection of all inputs.) With few exceptions, the compromise of accuracy and protection imposed by a diode-resistor network is not acceptable in the aircraft-system example mentioned above.

One such exception is the combination of external resistors with an 8-channel MAX328 or dual 4-channel MAX329 mux. These CMOS devices have ultra-low leakage: less than 3pA typical at +25C, rising to less than 20nA maximum at +125C. Low leakage allows use of relatively high-valued series resistors. A 100kΩ resistor, for instance, produces errors of 0.3μV at +25C and 2mV at +125C. The same resistor loads a 5V source by only 50μA when power is removed from the mux.

A nearly identical calculation shows that only 1.1mA flows in the internal protection diodes when you apply 110 VAC to the input resistor. This fault current is well below the allowed maximum (10mA continuous). It shows little change whether the mux power is on or off and makes a negligible contribution to power dissipation.

But before you specify 100kΩ resistors, keep in mind that error voltage depends on total current through the resistor, including (for example) input bias current from the op amp following the mux. What's more, the resistor combines with parasitic shunt capacitance to form a lowpass RC filter that may limit bandwidth. A more important limitation, the on-channel error caused by fault current flowing in an off channel, causes this configuration to fall short of design objectives in the aircraft example.

All design objectives can be met without external components, however, using the 8-channel MAX378 or the dual 4-channel MAX379 high-voltage, fault-protected mux. These devices have three MOSFETs (FETs) in series between each input and the output (one P-channel between two N-channel devices).

Each FET is biased and driven in a manner that affords nearly perfect protection whether the power is on or off. Inputs and output(s) are protected to ±60V with power on and to ±75V with power off. (Protection, in this case, means that any mux input becomes a virtual open circuit when connected to a voltage exceeding the supply, regardless of whether the input is selected or whether the mux power is on.)

Figure 3 is a test circuit for measuring off-channel input voltage vs. the resulting input leakage current. Data for the MAX378 (Figure 4) shows that input leakage during fault conditions is less than 20nA. A voltmeter at the mux output shows the effect of off-channel leakage on the selected channel. The effect with 100kΩ input resistors (less than 0.1mV) is hardly noticeable.

Fault-Protected and Fault-Protecting CMOS Multiplexers

V_{OUT} is limited by internal clamps to approximately 3V less than the supply rails, and ranges between ±12V with ±15V supplies. V_{OUT} collapses to 0V when the power is off.

Because MAX378/379 inputs and outputs are symmetrical and interchangeable, they are equally protected against applied fault voltages. Series current-limiting resistors are absent, so error voltages develop only across the internal FET's $r_{DS(ON)}$, 3kΩ total. Compared with the MAX328/329, the MAX378/379 can therefore operate with op amps of higher input bias current.

The latest generation of ultra-low-leakage analog muxes has simplified the design process considerably by expanding options and reducing limitations. New fault-protected analog muxes have transformed the process from one of circuit design to one of parts selection.

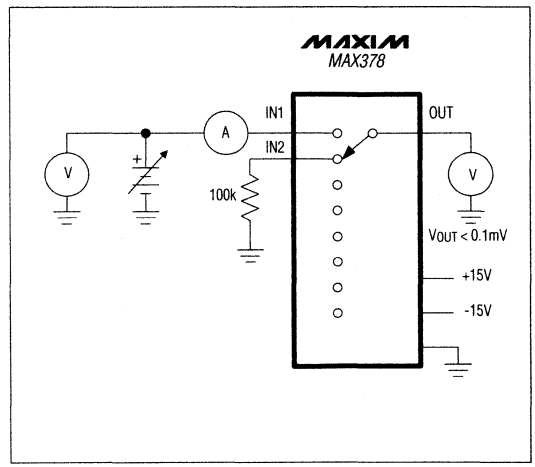


Figure 3. Input-Leakage Test Circuit

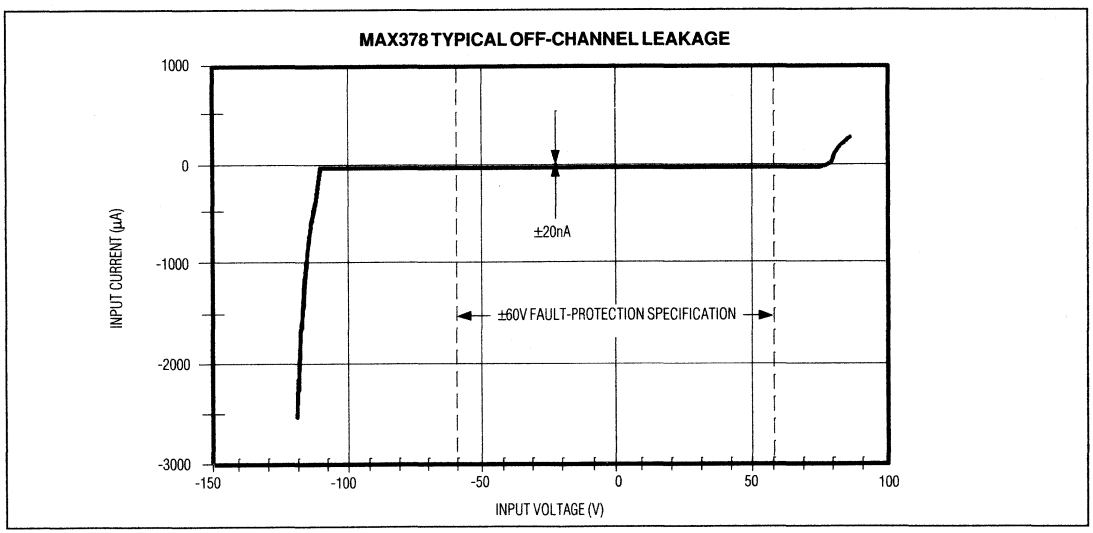


Figure 4. Off-Channel Leakage

19-3965; Rev 0; 4/91

MAXIM

Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

General Description

The MAX326/MAX327 quad, single-pole-single-throw (SPST), CMOS analog switches upgrade the DG201A/DG202 and DG211/DG212 with at least 100 times less leakage—the MAX326/MAX327 have 10pA maximum leakage, while the DG201A/DG202 have 1000pA and the DG211/DG212 have 5000pA. Low leakage currents support high system accuracy and make the devices useful for switching into high impedances, such as large-value feedback resistors in closed-loop gain configurations. And the MAX326/MAX327 logic inputs are CMOS and TTL compatible.

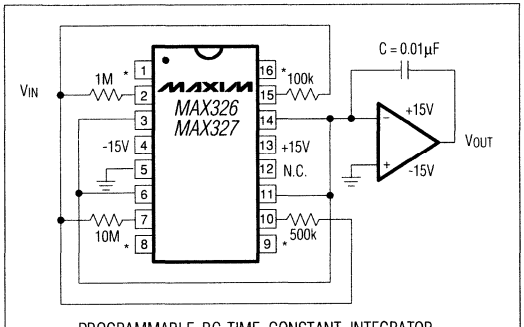
The MAX326/MAX327's low charge injection (3pC typ) minimizes signal error. Operation from single supplies (+10V to +30V), dual supplies (±5V to ±18V), and unbalanced combinations (i.e. +12V and -5V, or +5V and -15V) maximizes design flexibility. Both parts also feature interchangeable inputs/outputs and Maxim's standard latchup-proof construction.

Extremely low power consumption (5.25mW max) makes the MAX326/MAX327 ideal for portable applications. Other programmable applications include integrators with long RC time constants, current-to-voltage converters, high-gain amplifiers, and voltage dividers.

Applications

PBX, PABX
Military Radios
Sample-and-Hold Circuits
Winchester Disk Drives
Communication Systems
Guidance and Control Systems
Heads-Up Displays
Test Equipment

Typical Operating Circuit



PROGRAMMABLE RC-TIME CONSTANT INTEGRATOR
RC = 1ms TO 100ms IN FOUR STEPS

*NOTE: PINS 1, 8, 9, AND 16 ARE CHANNEL-CONTROL PINS.

Features

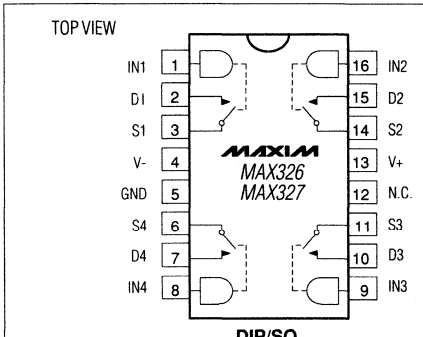
- ♦ **10pA Max Leakage (<1pA Typ)**
- ♦ **Plug-In, Low-Leakage Upgrades for DG201A/DG202 and DG211/DG212**
- ♦ **Interchangeable Inputs/Outputs**
- ♦ **CMOS and TTL Compatible**
- ♦ **3pC Typ Charge Injection**
- ♦ **Single- (+10V to +30V), Bipolar- (±5V to ±18V), or Unbalanced- (i.e. +12V and -5V) Supply Operation**
- ♦ **5.25mW Max Power Consumption**
- ♦ **Latchup-Proof Construction**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX326CPE	0°C to +70°C	16 Plastic DIP
MAX326CSE	0°C to +70°C	16 Narrow SO
MAX326CJE	0°C to +70°C	16 CERDIP
MAX326C/D	0°C to +70°C	Dice*
MAX326EPE	-40°C to +85°C	16 Plastic DIP
MAX326ESE	-40°C to +85°C	16 Narrow SO
MAX326EJE	-40°C to +85°C	16 CERDIP
MAX326MJE	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*
Ordering Information continued on page 6

Pin Configuration



DIP/SO

MAX326		MAX327	
LOGIC	SWITCH	LOGIC	SWITCH
0	ON	1	ON
1	OFF	0	OFF

Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... +40V
V_{IN} to GND ..... V-, V+
V_S, V_D (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
V+ to GND (V- = 0V) ..... +40V
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D 70mA
(pulsed at 1ms, 10% duty cycle max)
Continuous Total Power Dissipation (Note 2)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) .. 470mW
16-Pin Narrow SO (derate 10mW/°C above +70°C) .. 400mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW

Operating Temperature Ranges:
MAX32_C_ _ ..... 0°C to +70°C
MAX32_E_ _ ..... -40°C to +85°C
MAX32_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Exceeding this limit is acceptable as long as the S or D current is less than 20mA.
Note 2: All leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX32_M			MAX32_C/E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
SWITCH										
Analog-Signal Range	V_{ANALOG}		T_{MIN} to T_{MAX}			±15			±15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_D = ±10V, I_S = 100µA	T_A =+25°C		1.5	2.5		1.5	3.5	kΩ
			T_{MIN} to T_{MAX}		2.2	4		1.9	5	
On-Resistance Match			T_A =+25°C		5			5		%
Source-Off Leakage Current (Note 3)	$I_{S(OFF)}$	V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = -14V	T_A =+25°C		0.1	±10		0.1	±20	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
		V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = -14V, V_D = 14V	T_A =+25°C		0.2	±10		0.2	±20	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
Drain-Off Leakage Current (Note 3)	$I_{D(OFF)}$	V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = 14V, V_D = -14V	T_A =+25°C		0.1	±10		0.1	±20	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
		V_{IN} = 2.4V (MAX326), V_{IN} = 0.8V (MAX327), V_S = -14V, V_D = 14V	T_A =+25°C		0.2	±10		0.2	±20	pA
			T_{MIN} to T_{MAX}			±5			±5	nA
Drain-On Leakage Current (Note 3)	$I_{D(ON)}$	V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_S = V_D = 14V	T_A =+25°C		1	±20		1	±50	pA
			T_{MIN} to T_{MAX}			±10			±10	nA
		V_{IN} = 0.8V (MAX326), V_{IN} = 2.4V (MAX327), V_S = V_D = -14V	T_A =+25°C		2	±20		2	±50	pA
			T_{MIN} to T_{MAX}			±10			±10	nA
INPUT										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V	T_{MIN} to T_{MAX}	-1	-0.0004		-1	-0.0004		µA
		V_{IN} = 15V	T_{MIN} to T_{MAX}		0.003	1		0.003	1	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0V	T_{MIN} to T_{MAX}	-1	-0.0004		-1	-0.0004		µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX32_M			MAX32_C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY									
Positive Supply Current	I+	V_{IN} = 0V or 5V on all inputs		0.09	0.25		0.09	0.25	mA
Negative Supply Current	I-	V_{IN} = 0V or 5V on all inputs	-0.1	-0.00001		-0.1	-0.00001		mA
Power-Supply Range for Continuous Operation		(Note 4)	±4.5		±18	±4.5		±18	V
DYNAMIC									
Turn-On Time	t_{ON}	V_S = 2V, R_L = 1kΩ, C_L = 35pF (Figure 1)		500	1000		500	1000	ns
Turn-Off Time	t_{OFF}	V_S = 2V, R_L = 1kΩ, C_L = 35pF (Figure 1)		50	500		50	500	ns
Charge Injection	Q	C_L = 0.01µF, V_{GEN} = 0V, R_{GEN} = 0Ω		3			3		pC
Off Isolation (Note 4)	OIRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1V_{RMS}, f = 100kHz		70			70		dB
Crosstalk (Channel-to-Channel)	CCRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1V_{RMS}, f = 100kHz		90			90		dB
Source-Off Capacitance	$C_{S(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz		1.7			1.7		pF
Drain-Off Capacitance	$C_{D(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz		1.7			1.7		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz		6			6		pF

Note 3: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are sample tested for M-suffix devices at +25°C. E- and C- suffix devices are guaranteed at +25°C, but not tested. All leakage parameters are 100% tested at maximum rated operating temperatures, i.e. +70°C, +85°C, or +125°C.

Note 4: Electrical characteristics, such as $r_{DS(ON)}$, will change when power supplies other than ±15V are used. Power-supply range is a design characteristic, not production tested.

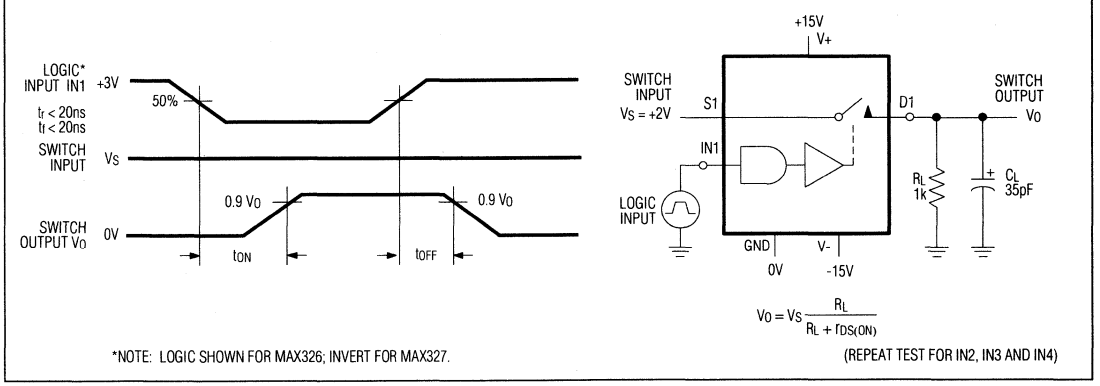
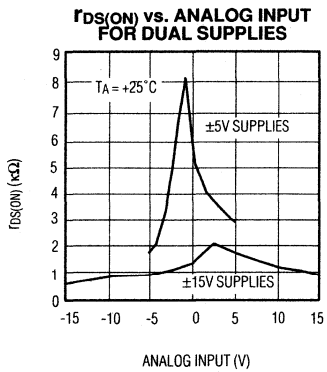
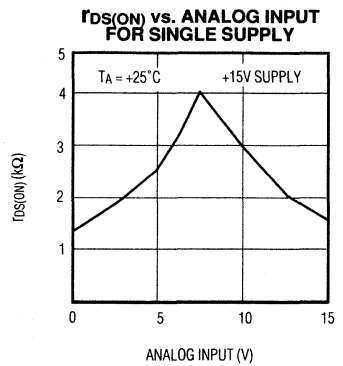


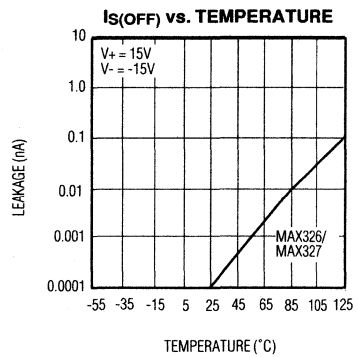
Figure 1. Switching-Time Test Circuit. Switch-output waveform shown for V_S = constant with logic-input waveform as shown. Note: V_S may be positive or negative as per switching-time test circuit. V_O is the steady-state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

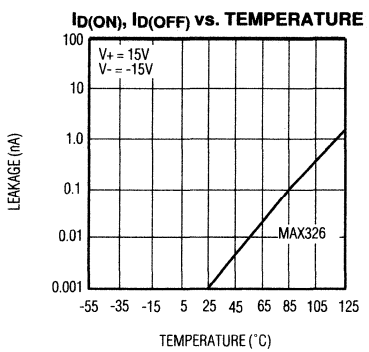
Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

Typical Operating Characteristics









Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

Application Hints

The MAX326/MAX327 are pin-compatible upgrades for the DG201A/DG202 and DG211/DG212. The MAX326/MAX327 feature significantly lower leakages (at least 100 times less at +25°C), but with higher on resistance. Low leakage minimizes signal error in most applications that require signal switching into high-impedance inputs of A/Ds or op amps. Switching times are virtually identical, as shown in Table 1.

Table 1. Switching Speeds with Various Power-Supply Combinations

POWER SUPPLY (V)	tON (µs)	tOFF (ns)
±15	0.5	50
±10	1	80
±5	2.5	200
+10	2.5	200
+15	1.5	100

The MAX326/MAX327 work well in single-supply applications from +10V to +30V. For these applications, V- should be connected to ground, and signal levels equal to the rail can be switched. ±5V to ±18V dual supplies can also be used to increase design flexibility.

Channel-to-channel on-resistance matching is typically better than 95% for a given analog input level. *Typical Operating Characteristics* show how $r_{DS(ON)}$ changes with various analog inputs and power-supply combinations.

While specified at TTL threshold levels, the logic threshold is roughly 1.5V ±0.2V and switches properly with CMOS input levels from -15V to +15V. Logic input levels should never be allowed to exceed the supply rails.

Protecting Against Fault Conditions

Fault conditions develop when power supplies are turned off with input signals still present, or when overvoltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased to conduct current from the signal source. If low current levels are required, the addition of external protection diodes is recommended (Figure 2).

To provide protection for overvoltages up to 20V above the supply rails, a 1N4001 or 1N914 diode should be placed in series with the positive and negative supplies (Figure 2). The addition of these diodes will reduce the analog signal range to 1V below the positive supply and 1V above the negative supply.

For signals that can be momentarily shorted to the 110VAC line, the addition of a 47kΩ, 1/2W resistor in series with the channel input is recommended. This will protect the switch and allow normal operation to continue once the fault condition abates. The throughput resistance will then be 47kΩ plus $r_{DS(ON)}$, but low switch leakage will reduce the error while maintaining superior system reliability.

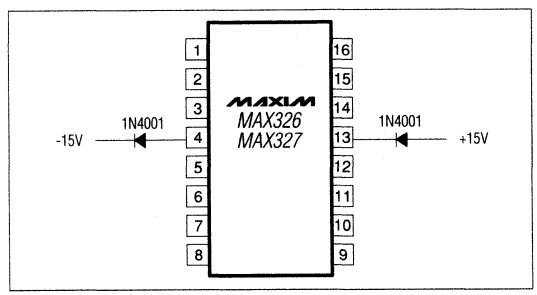


Figure 2. Protection Against Fault Conditions

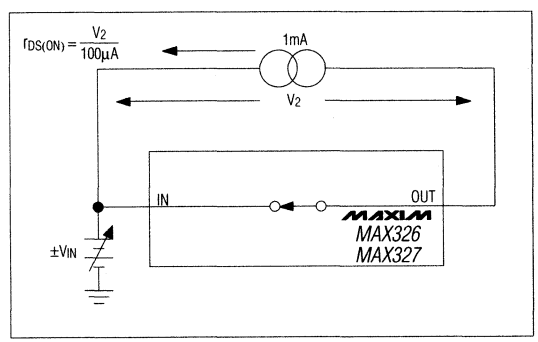


Figure 3. On Resistance vs. Analog-Signal Level Supply Voltage

Quad, SPST, Ultra-Low Leakage, CMOS Analog Switches

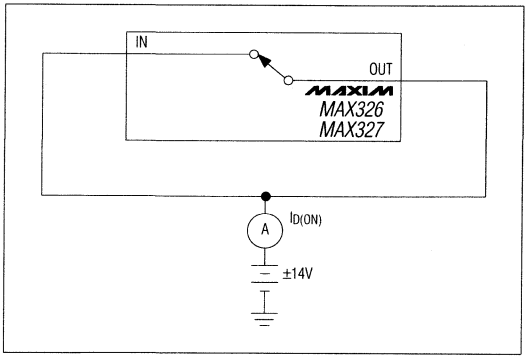


Figure 4. On Leakage Current Test Circuit

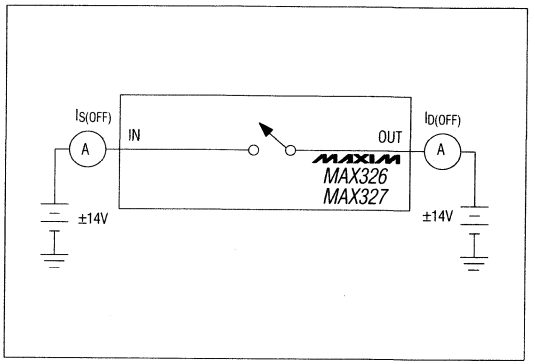


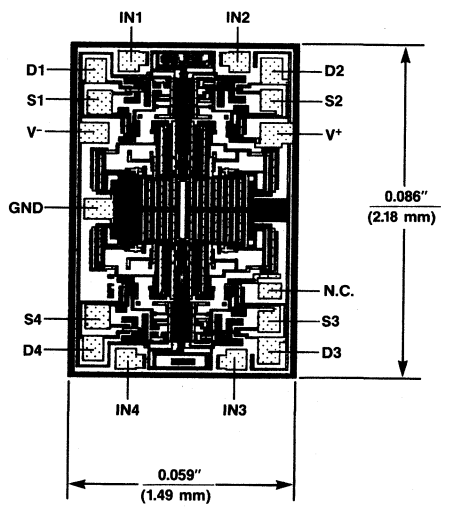
Figure 5. Off Leakage Current Test Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX327CPE	0°C to +70°C	16 Plastic DIP
MAX327CSE	0°C to +70°C	16 Narrow SO
MAX327CJE	0°C to +70°C	16 CERDIP
MAX327C/D	0°C to +70°C	Dice*
MAX327EPE	-40°C to +85°C	16 Plastic DIP
MAX327ESE	-40°C to +85°C	16 Narrow SO
MAX327EJE	-40°C to +85°C	16 CERDIP
MAX327MJE	-55°C to +125°C	16 CERDIP**

* Contact factory for dice specifications.
** Contact factory for availability and processing to MIL-STD-883.

Chip Topography



Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

General Description

The MAX328/MAX329 are monolithic CMOS analog multiplexers. The MAX328 is a single-ended, 1-of-8 device, and the MAX329 is a differential, 2-of-8 device.

Designed to provide the lowest possible "on" and "off" leakages, these multiplexers switch signals from high source impedance, providing the mux operates into a high input impedance op amp or A/D converter. The MAX328/MAX329 are pin-for-pin replacements for the popular DG508/DG509 in these applications.

Adding an external 40kΩ resistor to each input makes the MAX328/MAX329 an excellent fault-tolerant multiplexer. Low leakage (less than 1pA at 25°C) and 2.5kΩ on resistance allow the circuit to sustain 110V AC faults indefinitely while maintaining an error of less than 40nV for normal signals (i.e., 1pA times 40kΩ).

The MAX328/MAX329 work equally well with a single supply of 10V to 30V or dual supplies of ±5V to ±18V. They also perform well with unbalanced combinations of supply voltage, such as +12V and -5V or +5V and -15V. Low-power dissipation (1.9mW with ±15V supplies) allows use of the multiplexers in portable applications.

Applications

Control Systems

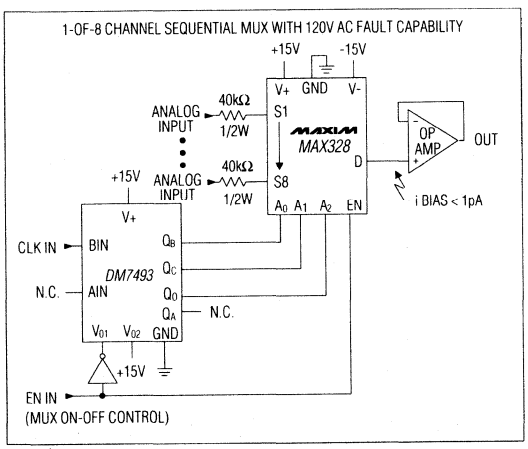
Data Logging Systems

Aircraft Heads-Up Displays

Data Acquisition Systems

Signal Routing

Typical Operating Circuit



Features

- ♦ **Ultra-Low "Off" and "On" Leakage: 1pA Typ**
- ♦ **Bi-Directional Operation (Use as Mux or Demux)**
- ♦ **TTL and CMOS Logic Compatibility**
- ♦ **Analog-Signal Range Includes Power-Supply Rails**
- ♦ **Switching Speeds Less Than 1.5µs**
- ♦ **Pin Compatible With DG508/DG509 and MAX358/MAX359**
- ♦ **Latch-Up Proof Construction**

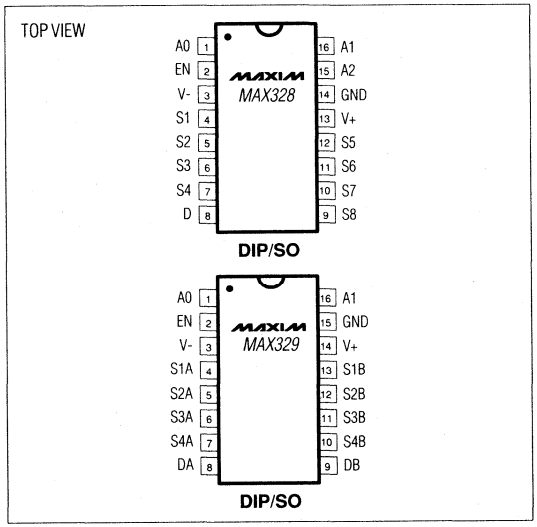
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX328CPE	0°C to +70°C	16 Plastic DIP
MAX328CWE	0°C to +70°C	16 Wide SO
MAX328CJE	0°C to +70°C	16 CERDIP
MAX328C/D*	0°C to +70°C	Dice
MAX328EPE	-40°C to +85°C	16 Plastic DIP
MAX328EWE	-40°C to +85°C	16 Wide SO
MAX328EJE	-40°C to +85°C	16 CERDIP
MAX328MJE	-55°C to +125°C	16 CERDIP

* *Contact factory for availability. Substrate may be allowed to float or be tied to V+.*

Ordering information continued on page 7.

Pin Configurations



Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... +44V
GND ..... +25V
Digital Inputs (Note 1), V_S, V_D ..... -2V to (V+ + 2V)
Current (Any Terminal, Except S or D) 30mA
Continuous Current, S or D 10mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max) 40mA

Operating Temperature Range:
MAX328/329 C _ _ ..... 0°C to +70°C
MAX328/329 E _ _ ..... -40°C to +85°C
MAX328/329 M _ _ ..... -55°C to +125°C
Power Dissipation (Package) (Note 1)
16-Pin CERDIP (Note 2) 900mW
16-Pin Plastic DIP (Note 3) 470mW
16-Pin Wide SO (Note 4) 750mW
Storage Temperature ..... -65°C to +150°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended peroids may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS MAX328M MAX329M MIN	TYP	MAX	LIMITS MAX328C/E MAX329C/E MIN	TYP	MAX	UNITS
SWITCH											
Analog-Signal Range		V_{ANALOG}			±15			±15			V
Drain-Source On Resistance		$r_{DS(on)}$	V_D = 10V, I_S = 100µA	Seq. Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V		1.5	2.5		1.5	3.5	kΩ
			V_D = -10V, I_S = 100µA			1.0	2.5		1.0	3.5	
Greatest Change In Drain-Source On-Resistance Between Channels		$\Delta r_{DS(on)}$	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ \mathbf{Max} - r_{DS(on)}\ \mathbf{Min}}{r_{DS(on)}\ \mathbf{Ave}}\right)$ $-10V \le V_S \le +10V$			2			2		%
Source-Off Leakage Current (Note 5)		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V		0.1	±10		1	±50	pA
			V_S = -10V, V_D = 10V			0.3	±10		0.3	±50	
Drain-Off Leakage Current (Note 5)	MAX328	$I_{D(off)}$	V_D = 10V, V_S = -10V	V_{EN} = 0V		0.3	±20		0.3	±50	pA
			V_D = -10V, V_S = 10V			1.0	±20		1.0	±50	
	MAX329		V_D = 10V, V_S = -10V			0.3	±10		0.3	±25	
			V_D = -10V, V_S = 10V			0.5	±10		0.5	±25	
Drain-On Leakage Current (Note 5)	MAX328	$I_{D(on)}$	$V_{S(all)}$ = V_D = 10V	Seq. Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V		3.0	±50		3.0	±100	pA
			$V_{S(all)}$ = V_D = -10V			2.0	±50		2.0	±100	
	MAX329		$V_{S(all)}$ = V_D = 10V			1.5	±25		1.5	±50	
			$V_{S(all)}$ = V_D = -10V			1.0	±25		1.0	±50	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MAX328M MAX329M MIN	TYP	MAX	LIMITS MAX328C/E MAX329C/E MIN	TYP	MAX	UNITS
INPUT										
Address Input Current, Input Voltage High	I_{AH}	V_A = 2.4V			.001	±1		.001	±1	µA
		V_A = 15V			.001	±1		.001	±1	
Address Input Current, Input Voltage Low	I_{AL}	V_{EN} = 2.4V	All V_A = 0V		.001	±1		.001	±1	µA
		V_{EN} = 0V			.001	±1		.001	±1	
DYNAMIC										
Switching Time Of Multiplexer	$t_{transition}$	See Figure 1				1.0			1.5	µs
Break-Before-Make Interval	t_{open}	See Figure 2			0.2			0.2		µs
Enable Turn-On Time	$t_{on(EN)}$	See Figure 3				1.0			1.5	µs
Enable Time-Off Time	$t_{off(EN)}$	See Figure 3				0.7			1.0	µs
OFF Isolation	OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF V_S = 7VRMS, f = 500kHz			84			84		dB
Source-Off Capacitance	$C_{S(off)}$	V_S = 0V	V_{EN} = 0V, f = 1MHz		1.8			1.8		pF
Drain-Off Capacitance MAX328	$C_{D(off)}$	V_D = 0V	V_{EN} = 0V, f = 1MHz		8.0			8.0		pF
Drain-Off Capacitance MAX329					4.0			4.0		
Charge Injection	$Q_{(inj)}$	VA = +10V			2			2		pc
		VA = 0V			3			3		
		VA = -10V			4			4		
SUPPLY										
Positive Supply Current	I+	V_{EN} = 2.4V	V_A = 0V/5V		4.5	200		4.5	200	µA
Negative Supply Current	I-	V_{EN} = 2.4V	V_A = 0V/5V		1	-100		1	-100	
Power-Supply Range For Continuous Operation (Note 6)	V_{OP}			±5		±18	±5		±18	V

Note 1: All leads soldered or welded to PC board.
Note 2: Derate 12mW/°C above +75°C.
Note 3: Derate 6.3mW/°C above +75°C.
Note 4: Derate 10mW/°C above +75°C.
Note 5: Leakage parameters I_S(Off), I_D(Off), and I_D(On) are sample tested for M suffix devices at +25°C. The E and C suffix devices are guaranteed at +25°C, but not production tested.
Note 6: Electrical characteristics, such as On Resistance, will change when power supplies other than ±15V are used. Power-supply range is a design characteristic, not production tested.

Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.

Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V+ = +15V, V- = -15V, GND = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS						UNITS
					MAX328M MAX329M			MAX328C/E MAX329C/E			
					MIN	TYP	MAX	MIN	TYP	MAX	
SWITCH											
Analog-Signal Range		V_{ANALOG}			±15			±15			V
Drain-Source On Resistance		$r_{DS(on)}$	V_D = 10V, I_S = 100µA	Seq. Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V		2.2	4		1.9	5	kΩ
			V_D = -10V, I_S = 100µA			1.5	4		1.2	5	
Source-Off Leakage Current (Note 7)		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V			±5			±5	nA
			V_S = -10V, V_D = 10V				±5			±5	
Drain-Off Leakage Current (Note 7)	MAX328	$I_{D(off)}$	V_D = 10V, V_S = -10V	V_{EN} = 0V			±20			±20	nA
			V_D = -10V, V_S = 10V				±20			±20	
	MAX329		V_D = 10V, V_S = -10V				±10			±10	
			V_D = -10V, V_S = 10V				±10			±10	
Drain-On Leakage Current (Note 7)	MAX328	$I_{D(on)}$	$V_{S(all)}$ = V_D = 10V	Seq. Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V			±20			±20	nA
			$V_{S(all)}$ = V_D = -10V				±20			±20	
	MAX329		$V_{S(all)}$ = V_D = 10V				±10			±10	
			$V_{S(all)}$ = V_D = -10V				±10			±10	
INPUT											
Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V			.01	±1		.01	±1	µA
			V_A = 15V			.01	±1		.01	±1	
Address Input Current, Input Voltage Low		I_{AL}	V_{EN} = 2.4V	All V_A = 0V		.01	±1		.01	±1	µA
			V_{EN} = 0V			.01	±1		.01	±1	

Note 7: Leakage parameters are 100% tested at maximum rated operating temperature, i.e., +70°C, etc.

TRUTH TABLE - MAX328

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE - MAX329

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Note: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

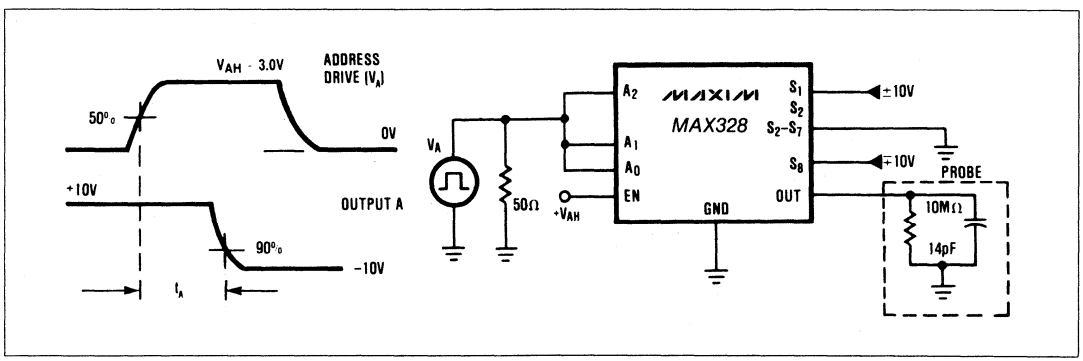


Figure 1. Access Time vs. Logic Level (High)

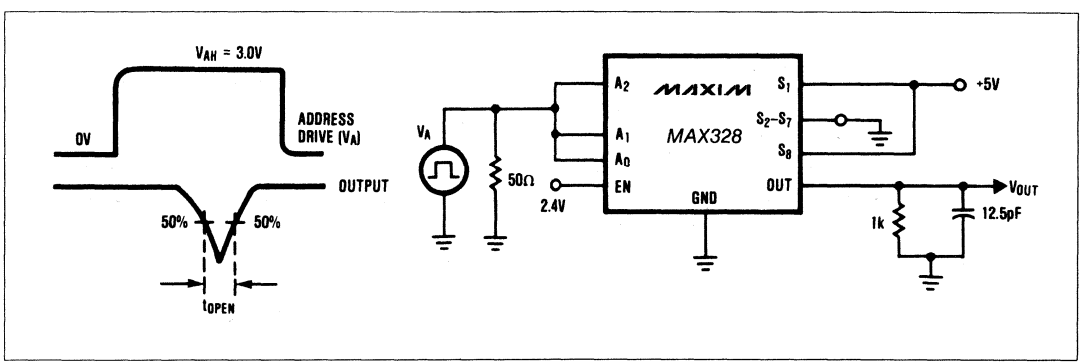


Figure 2. Break-Before-Make Delay (t_{OPEN})

Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

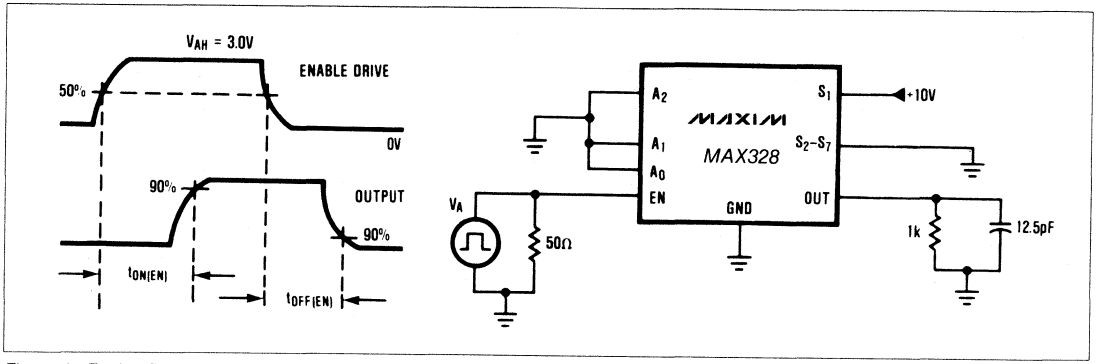
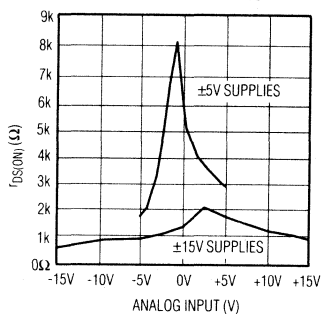


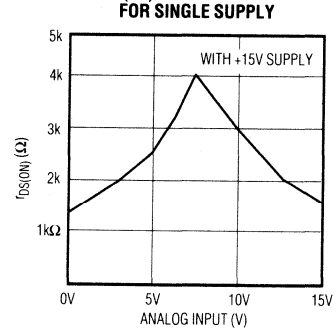
Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

Typical Operating Characteristics

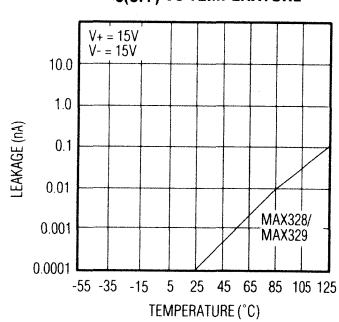
$r_{DS(ON)}$ VS ANALOG INPUT FOR DUAL SUPPLIES



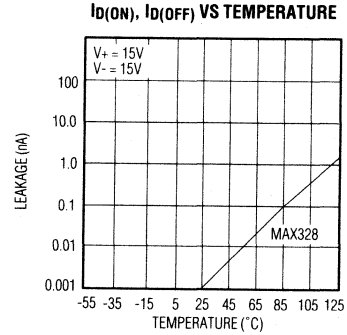
$r_{DS(ON)}$ VS ANALOG INPUT FOR SINGLE SUPPLY



$I_{S(OFF)}$ VS TEMPERATURE



$I_{D(ON)}$, $I_{D(OFF)}$ VS TEMPERATURE



Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

Application Notes

Figure 4 is a typical circuit for converting the MAX328/MAX329 into a fault-tolerant mux. In this application, the internal diodes limit the voltage at the MAX328 input to ±15.7V (±15V supplies). No external diodes need to be added with the MAX328/MAX329, unlike conventional multiplexers requiring external diodes.

The resistors, R, need to be 39kΩ or higher to limit the power dissipation in the resistor when a 120V AC fault occurs (i.e., power dissipation is $(120\text{-}16)^2/39k\Omega$ or 0.28W. This is why a 1/2W resistor is needed). The circuit withstands an indefinite fault to a 120V AC line with no damage to any component.

The guaranteed low leakage of the MAX328 is the key to this application. For the 10pA max I_S(off), the measurement error is 10pA X 39k = 0.39µV at room temperature. At 125°C, the leakages increase by a factor of 100; thus, 39µV is the high-temperature error. The commercial and industrial grades have a maximum leakage of 50pA of I_S(off) at room temperature. Therefore, 1.95µV is the room temperature error, and 195µV is the high-temperature (125°C) error.

Now, 17-bit accuracy decreases to 76µV for the least significant bit. Our 10pA model will meet this at 125°C, but not the 50pA model. Therefore, the 10pA model could be used in 16-bit systems over the military temperature range, but the 50pA model would be restricted to 100°C with adequate guardband.

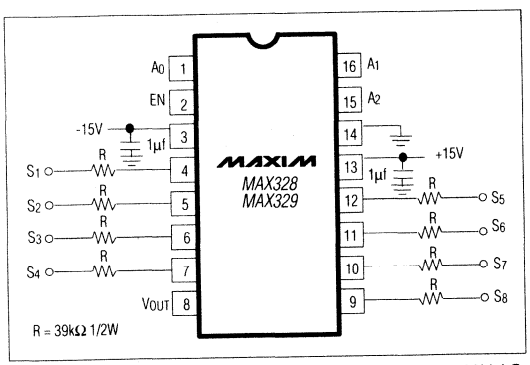


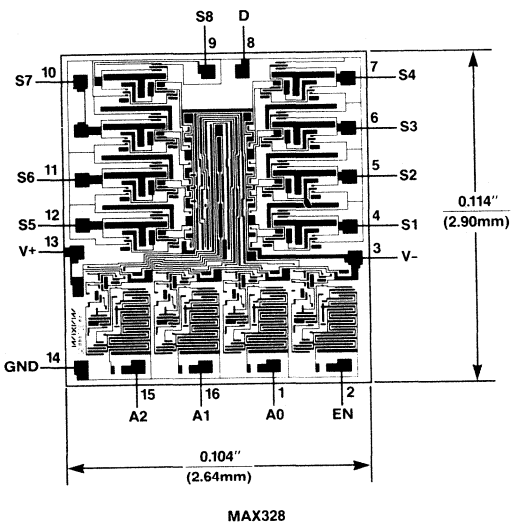
Figure 4. Fault-tolerant MUX (indefinitely withstands 120V AC fault voltages)

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX329CPE	0°C to +70°C	16 Plastic DIP
MAX329CWE	0°C to +70°C	16 Wide SO
MAX329CJE	0°C to +70°C	16 CERDIP
MAX329C/D*	0°C to +70°C	Dice
MAX329EPE	-40°C to +85°C	16 Plastic DIP
MAX329EWE	-40°C to +85°C	16 Wide SO
MAX329EJE	-40°C to +85°C	16 CERDIP
MAX329MJE	-55°C to +125°C	16 CERDIP

* Contact factory for availability. Substrate may be allowed to float or be tied to V+.

Chip Topographies



MAX328

MAXIM

Fault-Protected Analog Multiplexer

General Description

Maxim's HI-508A and MAX358 are 8 channel single-ended (1 of 8) multiplexers with fault protection. Maxim's HI-509A and MAX359 are 4 channel differential (2 of 8) multiplexers with fault protection. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly improved fault protection. If the power supplies to the Maxim fault-protected multiplexer are inadvertently turned off while input voltages are still applied, *all* channels in the multiplexer are turned off, and only a few nanoamperes of leakage current will flow into the inputs. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The Maxim series N-channel, P-channel, N-channel protection structure has two significant advantages over the simple current limiting protection scheme of the first generation fault protected multiplexers. First, the Maxim protection scheme limits fault currents to nanoamp leakage values rather than many milliamperes. This prevents damage to sensors or other sensitive signal sources. Second, the Maxim fault-protected multiplexers can withstand a *continuous* ±35V overvoltage, unlike the first generation which has a continuous overvoltage limitation of about ±10V imposed by power dissipation considerations.

All digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power supply currents have been reduced and typical power dissipation is less than 2 milliwatts.

Applications

Data Acquisition Systems

Industrial and Process Control Systems

Avionics Test Equipment

Signal Routing between Systems

Features

- **Improved 2nd Source (See "Maxim Advantage" on 3rd and 5th page)**
- **All Switches Off with Power Supplies Off**
- **On Channel Turns OFF if Overvoltage Occurs**
- **Only Nanoamperes of Input Current under All Fault Conditions**
- **Latchup-proof Construction**
- **Operates from ±4.5 to ±18V Supplies**
- **All Digital Inputs are TTL and CMOS Compatible**

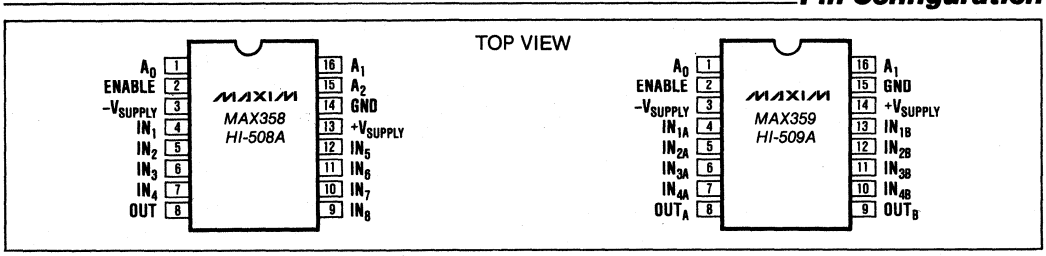
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX358CPE	0°C to +75°C	16 Lead Plastic DIP
MAX358CWE	0°C to +75°C	16 Lead Wide SO
MAX358CJE	0°C to +75°C	16 Lead CERDIP
MAX358EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX358EWE	-40°C to +85°C	16 Lead Wide SO
MAX358EJE	-40°C to +85°C	16 Lead CERDIP
MAX358MJE	-55°C to +125°C	16 Lead CERDIP
MAX358C/D**	0°C to +75°C	Dice
MAX359CPE	0°C to +75°C	16 Lead Plastic DIP
MAX359CWE	0°C to +75°C	16 Lead Wide SO
MAX359CJE	0°C to +75°C	16 Lead CERDIP
MAX359EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX359EWE	-40°C to +85°C	16 Lead Wide SO
MAX359EJE	-40°C to +85°C	16 Lead CERDIP
MAX359MJE	-55°C to +125°C	16 Lead CERDIP
MAX359C/D**	0°C to +75°C	Dice

(Ordering Information is continued on last page.)

** The substrate may be allowed to float or be tied to V^+ (JI CMOS).

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fault-Protected Analog Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins ..... +44V
V^+ ..... +22V
V^- ..... -22V
Digital Input Overvoltage:
V_{EN}, V_A { $V_{Supply}(+)$ ..... +4V
{ $V_{Supply}(-)$ ..... -4V
Analog Input Overvoltage with Multiplexer Power On:
V_S { $V_{Supply}(+)$ ..... +20V
{ $V_{Supply}(-)$ ..... -20V
Analog Input Overvoltage with Multiplexer Power Off:
V_S { $V_{Supply}(+)$ ..... +35V
{ $V_{Supply}(-)$ ..... -35V

Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (Note 1) (CERDIP) 1.28W
Operating Temperature Range:
MAX358/359M; HI-508A/509A-2, -8 ..... -55°C to +125°C
MAX358/359C; HI-508A/509A-5 ..... 0°C to +75°C
MAX358/359E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +75°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: HI-508A/509A (See facing page for MAX358/359.)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	$r_{DS(ON)}$	V_D = ±10V, I_S = 100µA V_{AL} = 0.8V, V_{AH} = 4V	+25°C Full		1.2 1.5	1.5 1.8		1.5 1.8	1.8 2.0	kΩ
OFF Input Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V V_{EN} = 0.8V (Note 2)	+25°C Full		0.03	 50		0.03	 50	nA
OFF Output Leakage Current	$I_{D(OFF)}$	V_D = ±10V, V_S = ∓10V V_{EN} = 0.8V HI-508A (Note 2) HI-509A	+25°C Full Full		0.1	 200 100		0.1	 200 100	nA
ON Channel Leakage Current	$I_{D(ON)}$	$V_{S(ALL)}$ = V_D = ±10V (Note 2) V_{AH} = V_{EN} = 4V HI-508A V_{AL} = 0.8V HI-509A	+25°C Full Full		0.1	 200 100		0.1	 200 100	nA
Analog Signal Range	V_{AN}		Full	-15		+15	-15		+15	V
Differential, OFF Output Leakage Current	I_{DIFF}	(HI-509A only)	Full			50			50	nA
FAULT										
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	V_D = 0V Analog Overvoltage = ±33V	+25°C Full		4.0	 2.0		4.0		nA µA
INPUT										
Input Low Threshold	V_{AL}	(Note 3)	Full			0.8			0.8	V
Input High Threshold	V_{AH}		Full	4.0			4.0			V
Input Leakage Current (High or Low)	I_A	V_A = 4V or 0V (Note 4)	Full			1.0			1.0	µA
DYNAMIC										
Access Time	t_A		+25°C		0.5	1.0		0.5	1.0	µs
Break-Before-Make Delay	t_{ON}-t_{OFF}	V_{EN} = +5V, V_{IN} = ±10V A_0, A_1, A_2 Strobed	+25°C	25	80		25	80		ns
Enable Delay (ON)	$t_{ON(EN)}$		+25°C Full		300	500 1000		300	 1000	ns
Enable Delay (OFF)	$t_{OFF(EN)}$		+25°C Full		300	500 1000		300	 1000	ns
Settling Time (0.1%) (0.01%)	t_{SETT}		+25°C		1.2 3.5			1.2 3.5		µs

Note 2: Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
Note 3: To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
Note 4: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Fault-Protected Analog Multiplexer

- ♦ Only Nanoamps of Leakage Under Fault Conditions
- ♦ All Switches OFF With Power Supplies Off
- ♦ Channel Turns OFF When Overvoltage Occurs
- ♦ TTL Compatible, No Pullups Required
- ♦ Significantly Reduced Power Consumption
- ♦ ±4.5V to ±18V Operation

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: MAX358/359 (See facing page for HI-508A/509A.)

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	$r_{DS(ON)}$	V_D = ±10V, I_S = 100μA V_{AL} = 0.8V, V_{AH} = 2.4V	+25°C Full		1.2 1.5	1.5 1.8		1.5 1.8	1.8 2.0	kΩ
OFF Input Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V V_{EN} = 0.8V	+25°C Full		0.03	0.5 50		0.03	1.0 50	nA
OFF Output Leakage Current	$I_{D(OFF)}$	V_D = ±10V, V_S = ∓10V V_{EN} = 0.8V MAX358 MAX359	+25°C Full Full		0.1	1.0 200 100		0.1	2.0 200 100	nA
ON Channel Leakage Current	$I_{D(ON)}$	$V_{S(ALL)}$ = V_D = ±10V (Note 2) V_{AH} = V_{EN} = 2.4V MAX358 V_{AL} = 0.8V MAX359	+25°C Full Full		0.1	2.0 200 100		0.1	5.0 200 100	nA
Analog Signal Range	V_{AN}	(Note 1)	Full	-15		+15	-15		+15	V
Differential, OFF Output Leakage Current	I_{DIFF}	MAX359 only	Full			50			50	nA
FAULT										
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	V_D = 0V (Note 2) Analog Overvoltage = ±33V	+25°C Full		4.0	 2.0		4.0		nA μA
Input Leakage Current (with Overvoltage)	$I_{S(OFF)}$	**V_{IN} = ±25V, V_O = ±10V (Note 2)**	**+25°C**			**5.0**			**10**	**μA**
Input Leakage Current (w. Power Supplies Off)	$I_{S(OFF)}$	**V_{IN} = ±25V, V_{EN} = V_O = 0V A_0 = A_1 = A_2 = 0V or 5V**	**+25°C**			**2.0**			**5.0**	**μA**
INPUT										
Input Low Threshold	V_{AL}		Full			0.8			0.8	V
Input High Threshold	V_{AH}		**Full**	**2.4**			**2.4**			**V**
Input Leakage Current (High or Low)	I_A	V_A = 4V or 0V (Note 4)	Full			1.0			1.0	μA
DYNAMIC										
Access Time	t_A	(Figure 1)	+25°C		0.5	1.0		0.5	1.0	μs
Break-Before-Make Delay (Figure 2)	t_{ON}-t_{OFF}	V_{EN} = +5V, V_{IN} = ±10V A_0, A_1, A_2 Strobed	+25°C	25	80		25	80		ns
Enable Delay (ON)	$t_{ON(EN)}$	(Figure 3)	+25°C Full		300	500 1000		300	 1000	ns
Enable Delay (OFF)	$t_{OFF(EN)}$	(Figure 3)	+25°C Full		300	500 1000		300	 1000	ns
Settling Time (0.1%) (0.01%)	t_{SETT}		+25°C		1.2 3.5			1.2 3.5		μs

Note 1: When the analog signal exceeds +13.5V or -12V the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
Note 2: The value shown is the steady state value. The transient leakage is typically 10μA. See detailed description.
Note 3: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.
Note 4: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

ELECTRICAL CHARACTERISTICS: HI-508A/509A (continued)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC (continued)										
"OFF Isolation" (Note 5)	$OFF_{(ISO)}$	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V = $7V_{RMS}$, f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	$C_{S(OFF)}$		+25°C		5			5		pF
Channel Output Capacitance	$C_{D(OFF)}$	HI-508A HI-509A	+25°C		25 12			25 12		pF
Digital Input Capacitance	C_A		+25°C		5			5		pF
Input to Output Capacitance	$C_{DS(OFF)}$		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I^+	V_{EN}, V_A = 0V or 4V	Full		0.5	2.0		0.5	2.0	mA
Negative Supply Current	I^-	V_{EN}, V_A = 0V or 4V	Full		0.02	1.0		0.02	1.0	mA

Note 5: Worst case isolation occurs on channel 4 due to proximity to the output pins.

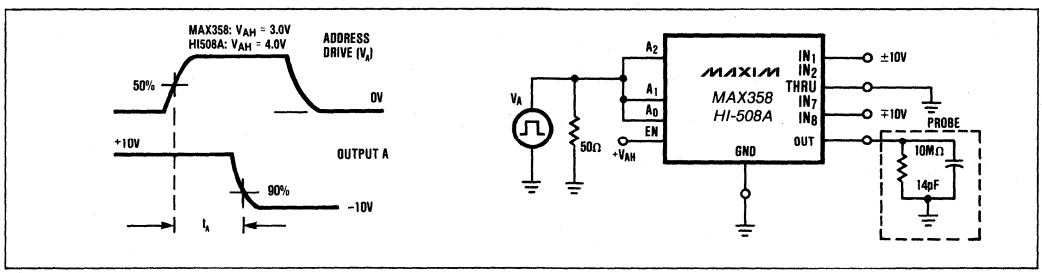


Figure 1. Access Time vs. Logic Level (High)

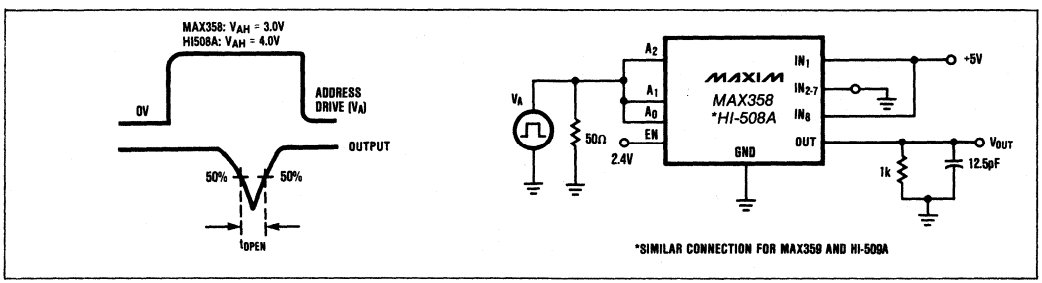


Figure 2. Break Before Make Delay (t_{OPEN})

ELECTRICAL CHARACTERISTICS: MAX358/359 (continued)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC (continued)										
"OFF Isolation"	$OFF_{(ISO)}$	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V = $7V_{RMS}$, f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	$C_{S(OFF)}$		+25°C		5			5		pF
Channel Output Capacitance	$C_{D(OFF)}$	MAX358 MAX359	+25°C		25 12			25 12		pF
Digital Input Capacitance	C_A		+25°C		5			5		pF
Input to Output Capacitance	$C_{DS(OFF)}$		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I^+	V_{EN} = 0.8V, or 2.4V All V_A = 0V or 5V	+25°C Full		0.1 0.3	0.6 0.7		0.2 0.5	1.0 1.0	mA
Negative Supply Current	I^-	V_{EN} = 0.8V or 2.4V All V_A = 0V or 5V	+25°C Full		0.01 0.02	0.1 0.2		0.01 0.02	0.1 0.1	mA
Power Supply Range for Continuous Operation	V_{OP}	(Note 5)	+25°C	±4.5		±18	±4.5		±18	V

Note 5: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

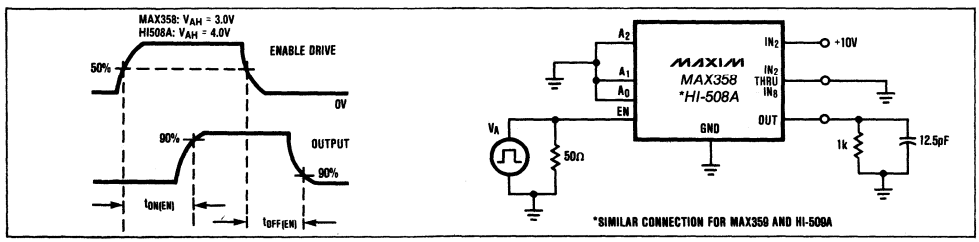


Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

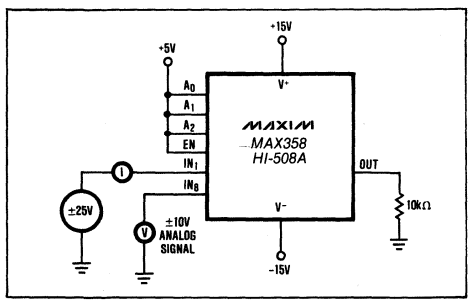


Figure 5. Input Leakage Current (Overvoltage)

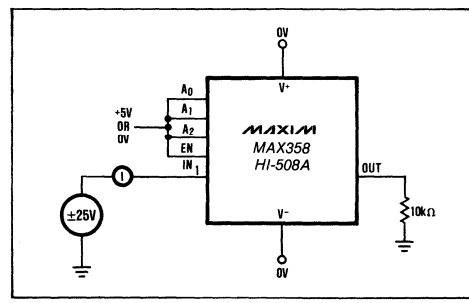
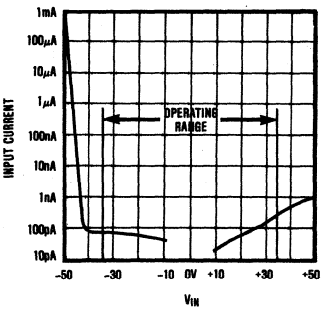


Figure 6. Input Leakage Current (with Power Supplies OFF)

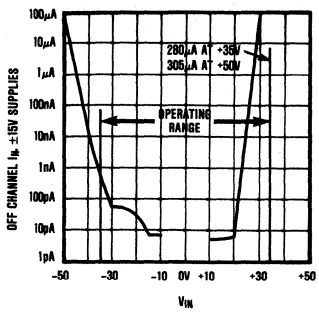
Fault-Protected Analog Multiplexer

Typical Operating Characteristics

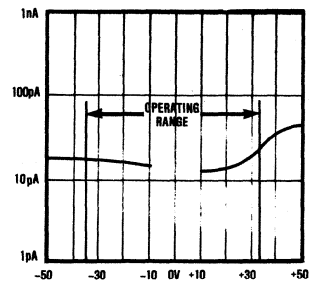
INPUT LEAKAGE VS. INPUT VOLTAGE WITH V+ = V- = 0V



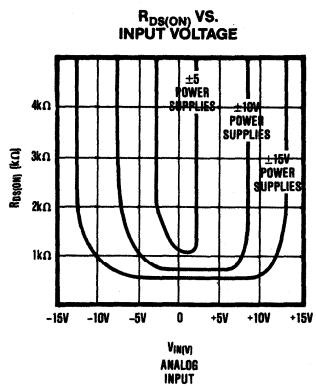
OFF CHANNEL LEAKAGE CURRENT VS. INPUT VOLTAGE WITH ±15V SUPPLIES



OUTPUT LEAKAGE VS. OFF CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$R_{DS(ON)}$ VS. INPUT VOLTAGE



TRUTH TABLE—MAX358 AND HI-508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE—MAX359 AND HI-509A

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTE: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

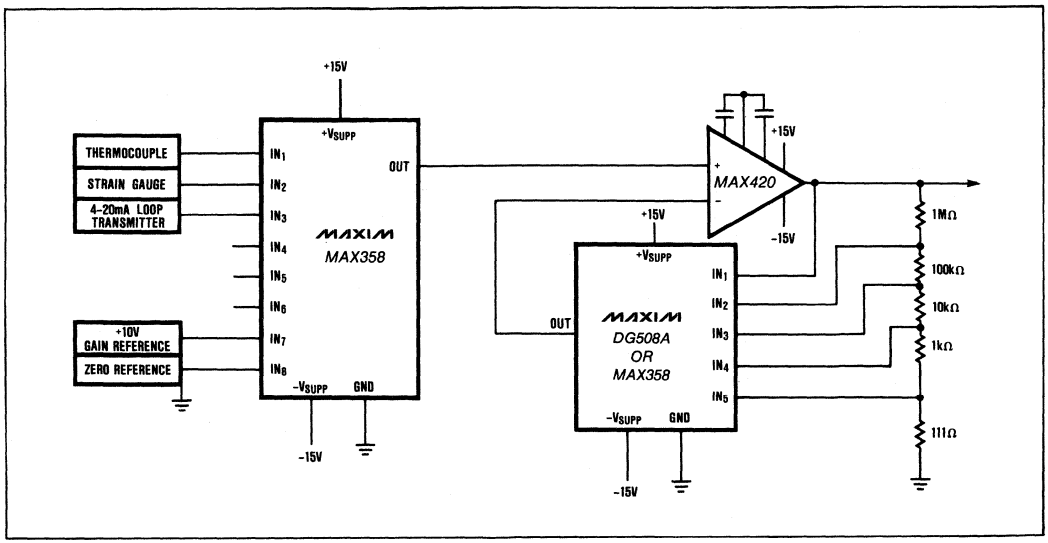


Figure 7. Typical Data Acquistion Front End

Typical Applications

Figure 7 shows a typical data acquisition system using the MAX358 multiplexer. Since the multiplexer is driving a high impedance input, its error is a function of its own resistance ($R_{DS(ON)}$) times the multiplexer leakage current ($I_{D(ON)}$) and the amplifier bias current (I_{BIAS}):

$$V_{ERR} = R_{DS(ON)} \times (I_{D(ON)} + I_{BIAS}\ (MAX420))$$
$$= 1.5k \times (2nA + 30pA)$$
$$= 3.05\mu V \text{ maximum error}$$

In most cases, this error is low enough that preamplification of input signals is not needed, even with very low level signals, such as 40μV/°C from type J thermocouples.

In systems with fewer than 8 inputs, an unused channel can be connected to the system ground reference point for software zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data acquisition system as well.

A MAX 420 precision op-amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed 5μV unadjusted offset of the MAX420 maintains high signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data acquisition system, normally a Sample/Hold and A/D. Since the gain-changing multiplexer is not connected to the external sensors, it can be either a DG508A multiplexer or the fault protected MAX358.

Input switching, however, must be done with a fault protected MAX358 multiplexer if it is to provide the level of protection and isolation required with most data acquisition inputs. Since external signal sources may continue to supply voltage when the multiplexer and system power are turned off, non-fault protected multiplexers, or even first-generation fault protected devices, will allow many milliamps of fault current to flow from outside sources into the multiplexer. The result could be damage to either the sensors or the multiplexer. A non-fault protected multiplexer will also allow input overvoltages to appear at its output, perhaps damaging Sample/Holds or A/Ds. Such input overdrives may also cause input-to-input shorts, allowing the high current output of one sensor to possibly damage another.

The MAX358 eliminates all of the above problems since it not only limits its output voltage to safe levels, with or without power applied ($+V_{SUP}$ and $-V_{SUP}$), but also turns all channels off when power is removed, drawing only sub-microamp fault currents from the inputs, and maintaining isolation between inputs for continuous overvoltages up to ±35V.

Fault-Protected Analog Multiplexer

Detailed Description

Fault Protection Circuitry

Maxim's HI-508A/509A and MAX358/359 are fully fault-protected for continuous input voltages up to ±35V, whether or not the $+V_{SUP}$ and $-V_{SUP}$ power supplies are present. These devices use a "series FET" protection scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels. This fault current is several orders of magnitude lower than the original manufacturer's HI-508A (several milliamps), which uses 1 to 2kΩ protection resistors in series with parasitic diodes connected to $+V_{SUP}$ and $-V_{SUP}$.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an OFF channel with $+V_{SUP}$ and $-V_{SUP}$ present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from -35V to +35V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages that fault current will initially be 10 or 20μA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 11 shows the condition of the ON channel with $+V_{SUP}$ and $-V_{SUP}$ present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds $+V_{SUP}$ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than $-V_{SUP}$ minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies.

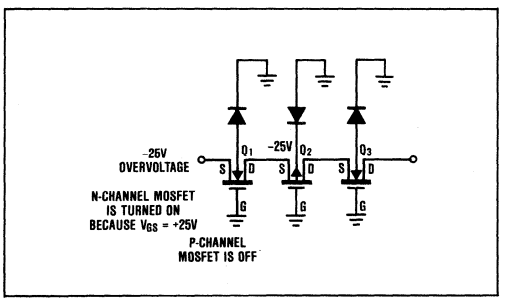


Figure 8. -25V Overvoltage with Multiplexer Power OFF

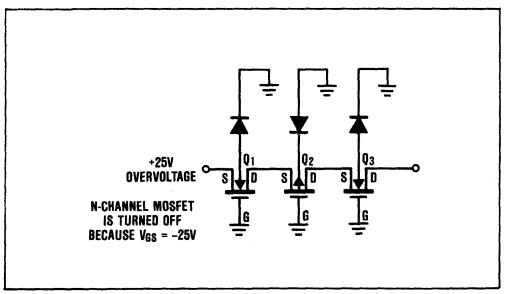


Figure 9. +25V Overvoltage with Multiplexer Power OFF

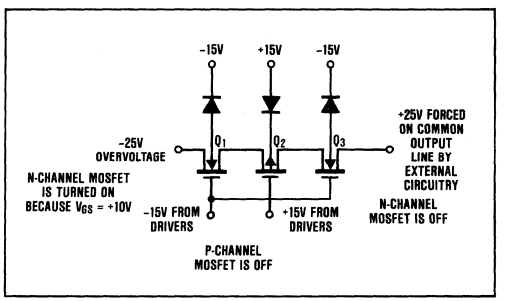


Figure 10. -25V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

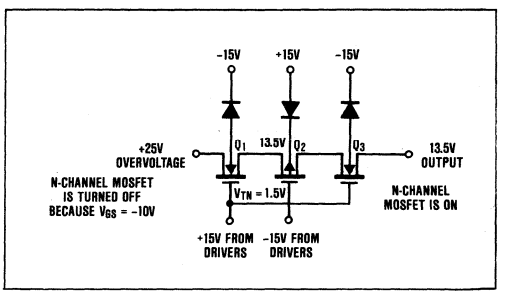


Figure 11. +25V Overvoltage Input to the ON Channel

The Typical Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated overvoltage of these devices is ±35V, the MAX358/359 typically has excellent performance up to ±40V, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX358/359 provides superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage. Note that since the channels are well matched, the differential charge injection for the MAX359/HI-509A is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break before make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as Figure 7, the dominant delay is not the switching time of the MAX358 multiplexer, but is the settling time of the following amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltages Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX358 limits the output voltage to about 1.5V below $+V_{SUP}$ and about 3V above $-V_{SUP}$. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The typical characteristics graphs show typical $R_{DS(ON)}$ for ±15V, ±10V, and ±5V power supplies. Maxim tests and guarantees the MAX358/359 for operation from ±4.5V to ±18V supplies. The switching delays are increased by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX358/9 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such at +15V and -5V. The digital threshold will remain approximately 1.6V above the Ground pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between $+V_{SUP}$ and $-V_{SUP}$. Connect $-V_{SUP}$ to 0V when operating with a +9V to +22V single supply.

The MAX358 digital threshold is relatively independent of the power supply voltages, going from a typical 1.6V when $+V_{SUP}$ is 15V to 1.5V typical with a 5V $+V_{SUP}$. This means that Maxim HI-508/509A and MAX358/359 will operate with standard TTL logic levels, even with ±5V power supplies. In all cases, the threshold of the ENable pin is the same as the other logic inputs.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the Ground pin.

The digital inputs can also be driven with CMOS logic

Table 1A. MAX358 AND HI-508A CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge
±5V	+1.7V 0V -1.7V	+100pC +70pC +45pC
±10V	+5V 0V -5V	+200pC +130pC +60pC
±15V	+10V 0V -10V	+300pC +180pC +50pC

Test Conditions: C_L = 1000pF on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2 = 0V$, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX359 AND HI-509A CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A - B
±5V	+1.7V 0V -1.7V	+105pC +73pC +48pC	+107pC +74pC +50pC	-2pC -1pC -2pC
±10V	+5V 0V -5V	+215pC +135pC +62pC	+220pC +139pC +63pC	-5pC -4pC -1pC
±15V	+10V 0V -10V	+325pC +180pC +55pC	+330pC +185pC +55pC	-5pC -5pC 0pC

Test Conditions: C_L = 1000pF on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A_1 = 0V, A_0 is toggled from 0V to 3V at a 2kHz rate.

Fault-Protected Analog Multiplexer

levels swinging from either $+V_{SUP}$ to $-V_{SUP}$ or from $+V_{SUP}$ to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1μA. The digital inputs are protected from ESD by a 30V zener diode between the input and $+V_{SUP}$, and can be driven ±6V beyond the supplies without drawing excessive current.

Operation as a Demultiplexer

The MAX358/9 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX358/9 provides both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX358 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX358 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases since the load driven by the MAX358 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasureable, since the digital pins are physically isolated from the analog section by the Ground and $-V_{SUP}$ pins. The groundplane formed by these lines is continued onto the MAX358/9 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. TYPICAL OFF ISOLATION REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: $V_{IN} = 20V_{PK-PK}$ at the tabulated frequency, $R_L = 1.5k$ between OUT and ground, EN = 0V.

$$OIRR = 20\ Log\ \frac{20V_{PK-PK}}{V_{OUT\ (PK-PK)}}$$

Table 2B. TYPICAL CROSSTALK REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
R_L = 1.5k	70dB	68dB	64dB
R_L = 10k	62dB	46dB	42dB

Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, $A_0 = A_1 = A_2$ = +5V (Channel 1 selected). $20V_{PK-PK}$ at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

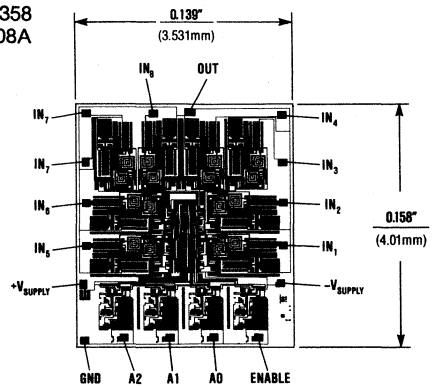
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
HI1-0508A-2	-55°C to +125°C	16 Lead CERDIP
HI1-0508A-5*	0°C to +75°C	16 Lead CERDIP
HI3-0508A-5*	0°C to +75°C	16 Lead Plastic DIP
HI1-0509A-2	-55°C to +125°C	16 Lead CERDIP
HI1-0509A-5*	0°C to +75°C	16 Lead CERDIP
HI3-0509A-5*	0°C to +75°C	16 Lead Plastic DIP

* Maxim burns in all devices at 150°C. Maxim's -5 device is therefore equivalent to the original manufacturer's -7 product.

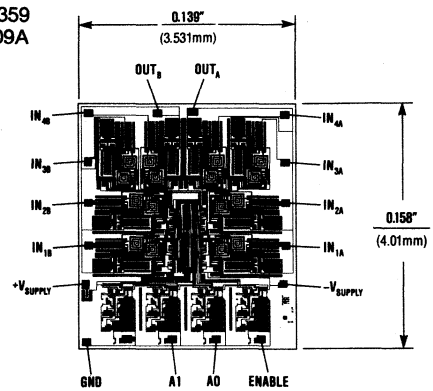
Chip Topographies

MAX358
HI-508A



Note: Connect substrate to $+V_{SUPPLY}$ or Leave It Floating

MAX359
HI-509A



Note: Connect substrate to $+V_{SUPPLY}$ or Leave It Floating

Fault-Protected Analog Multiplexer with Latch

General Description

Maxim's MAX368/369 are 8 channel single-ended (1 of 8) and 4 channel differential (2 of 8) fault-protected multiplexers with on-chip data latches. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly inproved fault protection over previous devices. If power to the multiplexers is removed while input voltages are still applied, all channels turn off, allowing only a few nanoamperes of leakage current to flow in the inputs. This not only protects the multiplexer and the circuitry connected to the output, but also protects the sensors or signal sources which drive the multiplexer inputs.

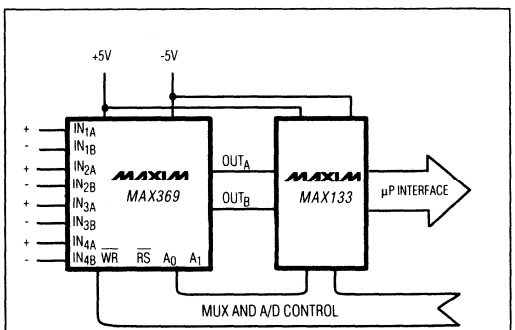
When an overvoltage signal of up to ±35V is applied to an analog input of a Maxim fault-protected multiplexer, that input channel turns off. If the overvoltage is applied to an on channel, the multiplexer output is clamped to less than its power supply voltage, thereby protecting sensitive circuitry that may be connected to the multiplexer output.

All channel selection and control inputs are fully compatible with both TTL and CMOS logic levels. In addition, break-before-make switch operation is guaranteed and typical power dissipation is less than 7 milliwatts, which makes the MAX 368/369 ideally suited for portable equipment usage.

Applications

Data Acquisition Systems
Industrial Process Control Systems
Avionics Test Equipment
Signal Routing Between Systems
Computer Controlled Analog Data Logging

Typical Operating Circuit



Input Protected Differential Input Data Acquisition System

Features

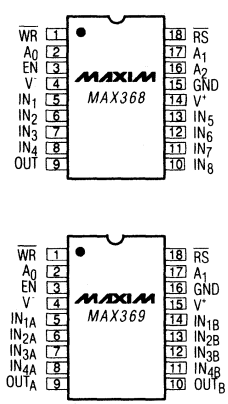
- **All Switches Off with Power Supplies Off**
- **Overvoltage Protection up to ±35V**
- **Only Nanoamperes of Input Current under All Fault Conditions**
- **Latch-Up Proof Construction**
- **Operates from ±4.5 to ±18V Supplies**
- **All Digital Inputs are TTL and CMOS Compatible**
- **Internal Data Latches for Channel Selection**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX368C/D	0°C to +70°C	Dice
MAX368CPN	0°C to +70°C	18 Lead Plastic DIP
MAX368CJN	0°C to +70°C	18 Lead CERDIP
MAX368CWN	0°C to +70°C	18 Lead Wide SO
MAX368EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX368EJN	-40°C to +85°C	18 Lead CERDIP
MAX368EWN	-40°C to +85°C	18 Lead Wide SO
MAX368MJN	-55°C to +125°C	18 Lead CERDIP
MAX369C/D	0°C to +70°C	Dice
MAX369CPN	0°C to +70°C	18 Lead Plastic DIP
MAX369CJN	0°C to +70°C	18 Lead CERDIP
MAX369CWN	0°C to +70°C	18 Lead Wide SO
MAX369EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX369EJN	-40°C to +85°C	18 Lead CERDIP
MAX369EWN	-40°C to +85°C	18 Lead Wide SO
MAX369MJN	-55°C to +125°C	18 Lead CERDIP

Pin Configurations

Top View



Fault-Protected Analog Multiplexer with Latch

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins ..... +44V
V^+ ..... +22V
V^- ..... -22V
Digital Input Overvoltage:
V_{EN}, V_A { $V_{Supply}(+)$ ..... +4V; $V_{Supply}(-)$ ..... -4V
Analog Input Overvoltage with Multiplexer Power On:
V_S { $V_{Supply}(+)$ ..... +20V; $V_{Supply}(-)$ ..... -20V
Analog Input Overvoltage with Multiplexer Power Off:
V_S { $V_{Supply}(+)$ ..... +35V; $V_{Supply}(-)$ ..... -35V

Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (Note 1) (CERDIP) 1.28W
Operating Temperature Range:
MAX368/369C ..... 0°C to +70°C
MAX368/369E ..... -40°C to +85°C
MAX368/369M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +70°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V; GND = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4V unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		TEMP *	TYP	M SUFFIX MIN	M SUFFIX MAX	E, C SUFFIX MIN	E, C SUFFIX MAX	UNITS
ANALOG SWITCH											
Analog Signal Range		V_{ANALOG}	(Note 2)		1		-15	15	-15	15	V
Drain-Source ON Resistance		$r_{DS(ON)}$	V_D = ±10V, V_{AL} = 0.8V I_S = 100µA, V_{AH} = 2.4V		1, 3 2			1500 1800		1800 2000	Ω
Greatest Change in $r_{DS(ON)}$ Between Channels		$\Delta r_{DS(ON)}$	-10V < V_S < 10V		1	10					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0.8V	V_S = ±10V V_D = ∓10V	1 2	-0.005	-1 -50	1 50	-5 -50	-5 50	nA
Drain OFF Leakage Current	MAX368	$I_{D(OFF)}$	V_{EN} = 0.8V	V_D = ±10V V_S = ∓10V	1 2	-0.015	-2 -200	2 200	-5 -200	5 200	nA
	MAX369			V_D = ±10V V_S = ∓10V	1 2	-0.008	-1 -100	1 100	-5 -100	5 100	nA
Drain ON Leakage Current	MAX368	$I_{D(ON)}$	V_S = V_D = ±10V V_{EN} = 2.4V V_{AL} = 0.8V V_{AH} = 2.4V		1 2	-0.03	-2 -200	2 200	-5 -200	5 200	nA
	MAX369				1 2	-0.015	-1 -100	1 100	-5 -100	5 100	nA
LOGIC INPUT											
Logic Input Current (Input Voltage High)		I_{AH}	V_A = 2.4V		1, 2, 3	-0.002	-1	1	-1	1	µA
			V_A = 14V		1, 2, 3	0.006	-1	1	-1	1	µA
Logic Input Current (Input Voltage Low)		I_{AL}	V_{EN} = 0 or 2.4V, V_A = 0V $\overline{RS}$ = 0V, $\overline{WR}$ = 0V		1, 2, 3	-0.002	-1	1	-1	1	µA
FAULT											
Output Leakage Current (with Overvoltage)		$I_{D(OFF)}$	V_D = 0V (Note 3) Analog Overvoltage = ±33V		1 2		-10 -2000	10 2000	-20 -2000	20 2000	nA
Input Leakage Current (with Overvoltage)		$I_{S(OFF)}$	V_{IN} = ±25V, V_D = ±10V (Note 3)		1		-5	5	-10	10	µA
Input Leakage Current (with Power Supplies Off)		$I_{D(OFF)}$	V_{IN} = ±25V, V_{EN} = V_0 = 0V A_0 = A_1 = A_2 = 0V or 5V		1		-2	2	-5	5	µA

*1 = 25°C, 2 = 125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V; GND = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP *	TYP	M SUFFIX MIN	M SUFFIX MAX	E,C SUFFIX MIN	E,C SUFFIX MAX	UNITS
DYNAMIC									
Switching Time of Multiplexer	t_{TRANS}	See Figure 2	1	0.6		1		1	µs
Break-Before-Make Interval	t_{OPEN}	See Figure 4	1	0.2					
Enable and Write Turn ON Time	$t_{ON\ (EN,\ \overline{WR})}$	See Figures 3 and 5	1	1		1.5		1.5	
Enable and Reset Turn OFF Time	$t_{OFF\ (EN,\ \overline{RS})}$	See Figures 3 and 6	1	0.4		1		1	
Charge Injection	Q	See Figure 7 and Tables 1A and 1B	1	55					pC
OFF Isolation	OIRR	V_{EN} = 0, R_L = 1kΩ, C_L = 15pF, V_{IN} = $7V_{RMS}$, f = 100kHz	1	68					dB
Logic Input Capacitance with Switch OFF	C_{IN}	f = 1MHz	1	5					pF
Input Capacitance with Switch OFF	$C_{S(OFF)}$	V_{EN} = 0, f = 140kHz, V_{IN} = 0	1	5					pF
Output Capacitance with Switch OFF, MAX368	$C_{D(OFF)}$	V_{EN} = 0, f = 140kHz, V_{OUT} = 0	1	25					
Output Capacitance with Switch OFF, MAX369	$C_{D(OFF)}$	V_{EN} = 0, f = 140kHz, V_{OUT} = 0	1	12					
$\overline{WR}$ Pulse Width	t_{WW}	See Figure 1	1, 2, 3		300		300		ns
A_X, EN Data Valid to $\overline{WR}$	t_{DW}	Set-up Time See Figure 1	1, 2, 3		180		180		
A_X, EN Data Valid after $\overline{WR}$	t_{WD}	Hold Time See Figure 1	1, 2, 3	0	10		30		
$\overline{RS}$ Pulse Width	t_{RS}	V_{IN} = 5V See Figure 1	1, 2, 3		300		500		
SUPPLY									
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V/5V	1, 2, 3			1.25 1.5		1.5 2.0	mA
Negative Supply Current	I-	V_{EN} = 2.4V, V_A = 0V/5V	1, 2, 3		-0.1 -0.2		-0.1 -0.2		

*1 = 25°C, 2 = 125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

Note 2: When the analog signal exceeds +13.5V or -12V, the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
Note 3: The value shown is the steady state value. The transient leakage is typically 10µA. See detailed description.
Note 4: Electrical Characteristics, such as ON Resistance will change when power supplies other than ±15V are used.
Note 5: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Fault-Protected Analog Multiplexer with Latch

TRUTH TABLE — MAX368

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE — MAX369

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching					
X	X	X	↑	1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

NOTE: Logic "1" : $V_{AH} \geq$ 2.4V, Logic "0" : $V_{AL} \leq$ 0.8V.

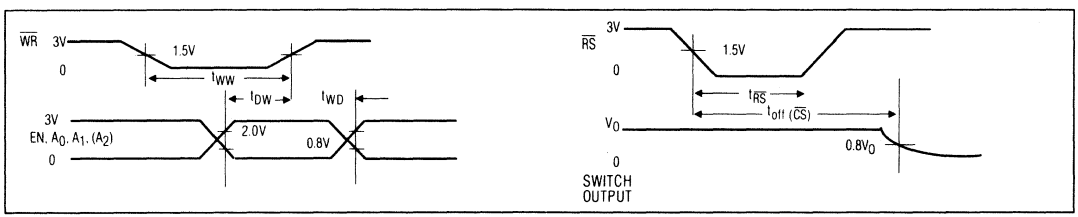


Figure 1. Typical Timing Diagrams for MAX368/369

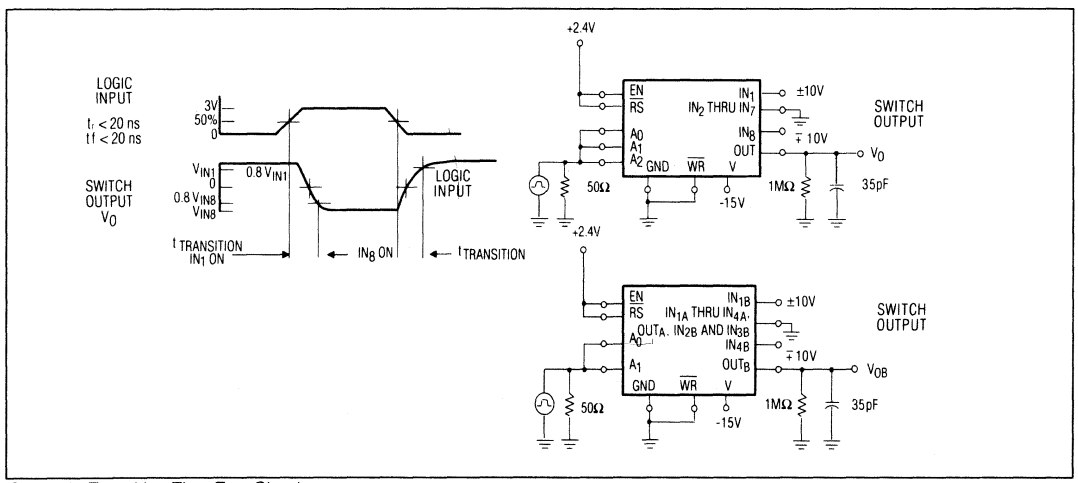


Figure 2. Transition Time Test Circuits

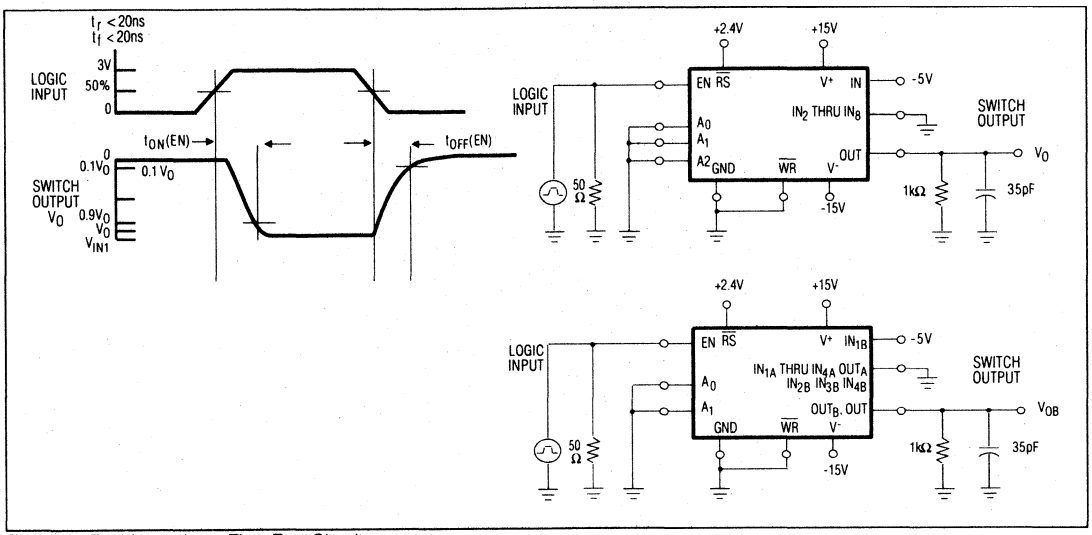


Figure 3. Enable t_{ON}/t_{OFF} Time Test Circuit

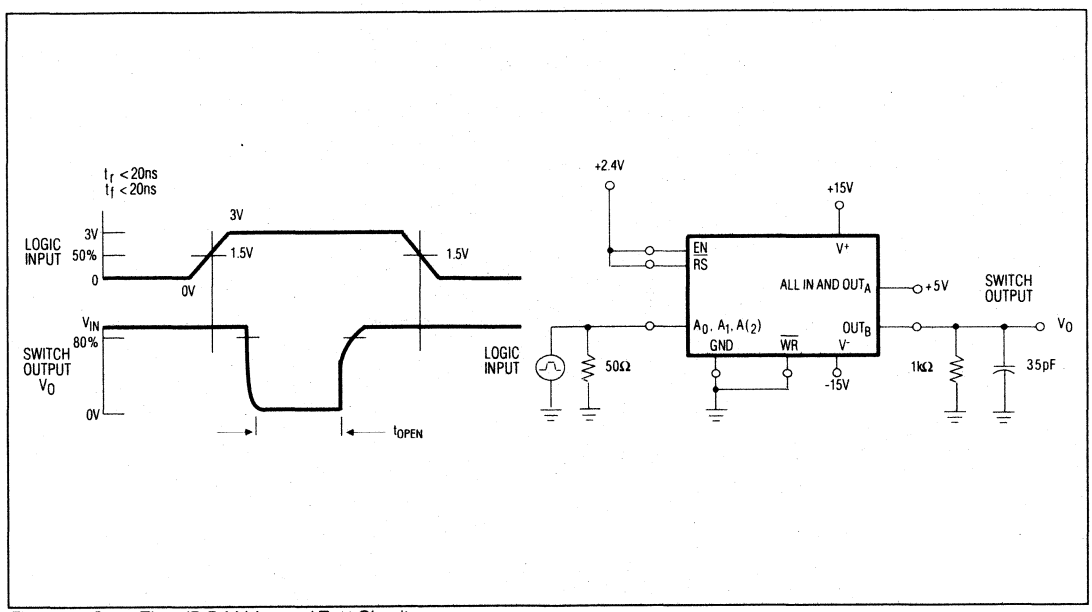


Figure 4. Open Time (B.B.M.) Interval Test Circuit

Fault-Protected Analog Multiplexer with Latch

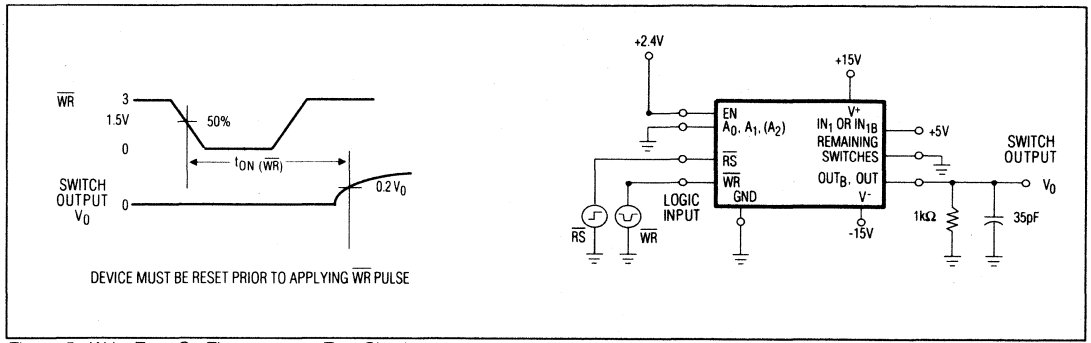


Figure 5. Write Turn-On Time $t_{ON(\overline{WR})}$ Test Circuit

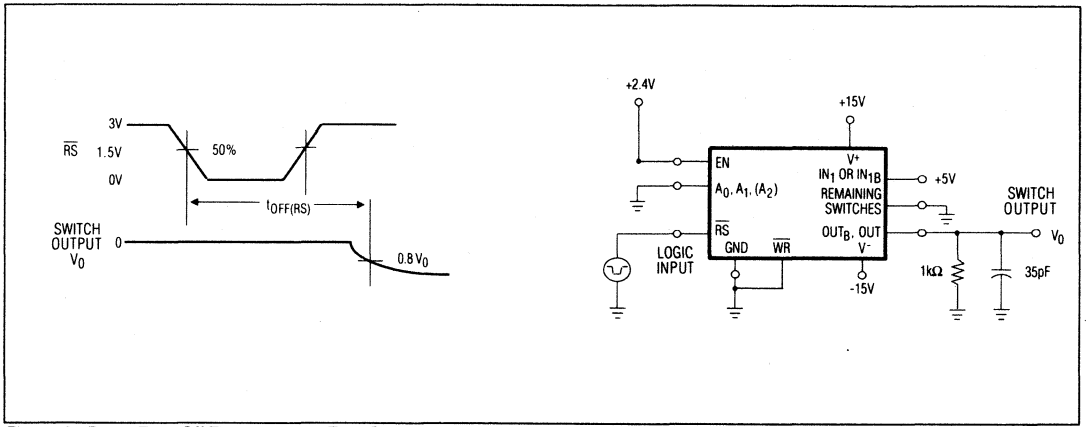


Figure 6. Reset Turn-Off Time $t_{OFF(\overline{RS})}$ Test Circuit

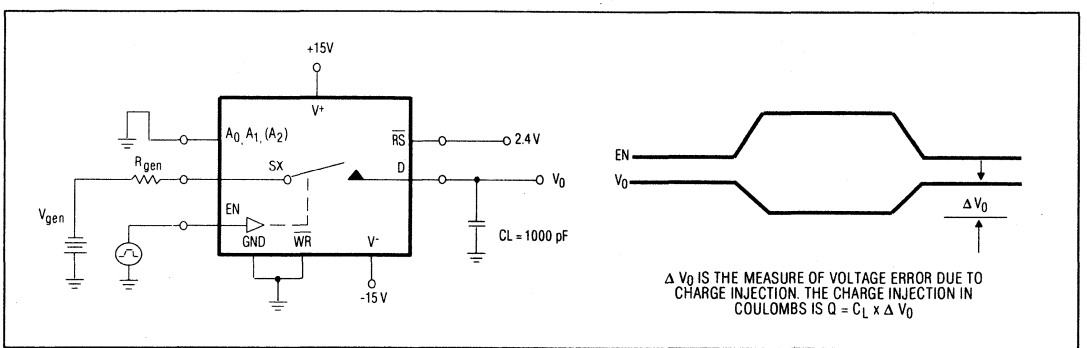


Figure 7. Charge Injection Test Circuit

Fault-Protected Analog Multiplexer with Latch

Detailed Description

Fault Protection Circuitry

Maxim's MAX368/369 are fully fault-protected for continuous input voltages up to ±35V, whether or not the $+V_{SUP}$ and $-V_{SUP}$ power supplies are present. These devices use a "series FET" protection scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all the FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any over voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an OFF channel with $+V_{SUP}$ and $-V_{SUP}$ present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from -35V to +35V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages the fault current will initially be 10 or 20µA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 11 shows the condition of the ON channel with $+V_{SUP}$ and $-V_{SUP}$ present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds $+V_{SUP}$ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than $-V_{SUP}$ minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies

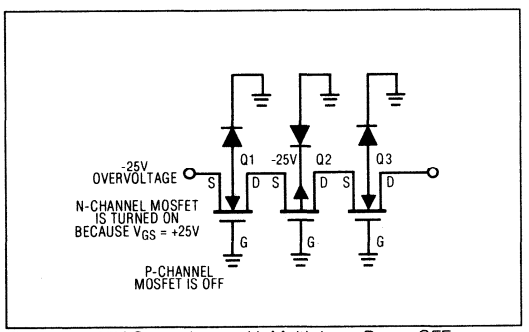


Figure 8. -25V Overvoltage with Multiplexer Power OFF

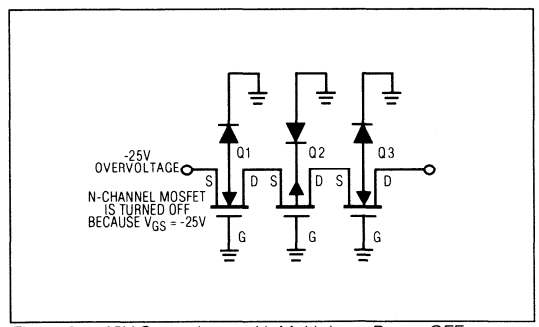


Figure 9. +25V Overvoltage with Multiplexer Power OFF

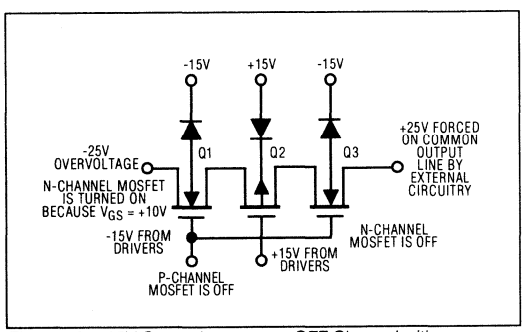


Figure 10. -25V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

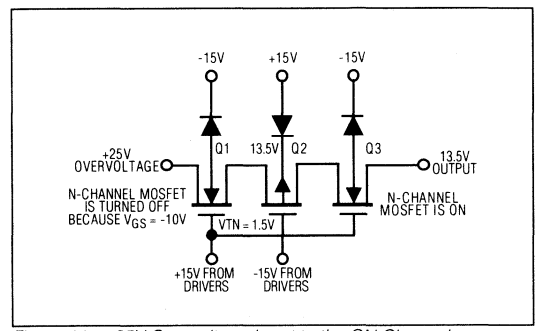


Figure 11. +25V Overvoltage Input to the ON Channel

Fault-Protected Analog Multiplexer with Latch

The Typical Operating Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated overvoltage of these devices is ±35V, the MAX368/369 typically has excellent performance up to ±40V, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX368/369 provides superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Digital Control Circuitry

The internal structure of the MAX368/369 includes translators for the A_0, A_1, A_2, EN, $\overline{RS}$, and WR digital inputs, latches, a decode section for channel selection (see Truth Tables on the fourth page of this data sheet). The gate structure consists of series N-channel/ P-channel/ N-channel MOSFETs (see Figure 12). This combination produces a very rugged, fault tolerant multiplexer with address latch capability, and does so with extremely low power dissipation.

Write ($\overline{WR}$), and Reset ($\overline{RS}$) strobes are provided for interfacing with microprocessor bus lines (Figure 13), alleviating the need for the microprocessor to provide constant address inputs to the MUX in order to hold on to a particular channel.

When the write strobe is in the low state (less than 0.8V), and the reset strobe is in the high state (greater than 2.4V), the MUXs are in the transparent mode; this means that the MUXs act similar to non-latching MUXs such as the MAX358/359 or the HI-508A/509A.

When the write input goes to the high state (>2.4V), the previous BCD address input will be latched and held in that state indefinitely. To pull the MUX out of this state, either the write input ($\overline{WR}$) must be taken low (0.8V), back to the transparent state, or the Reset ($\overline{RS}$) input taken low, turning off all channels.

The function of the Reset input is to allow for turning off all channels when the $\overline{RS}$ input is low (<0.8V); this has the dual function of resetting channel selection back to the channel 1 mode.

The MAX368/369 is designed to work with single as well as dual supplies, and good performance can be expected in the 9V to 22V single supply range. For example, with a single +15V power supply, analog signals in the range of +3.3V to +12V can be switched normally, and overvoltages up to ±35V can still be tolerated. If negative signals, around 0V are expected, a negative supply is needed. However, only -5V is needed to normally switch signals in the -2V to +12V range (-5V, +15V supplies). No current is drawn from the negative supply, so Maxim's MAX635 D/C to D/C converter does the job very nicely.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more MAX368s are cascaded to build 16-line and larger analog signal input multiplexers.

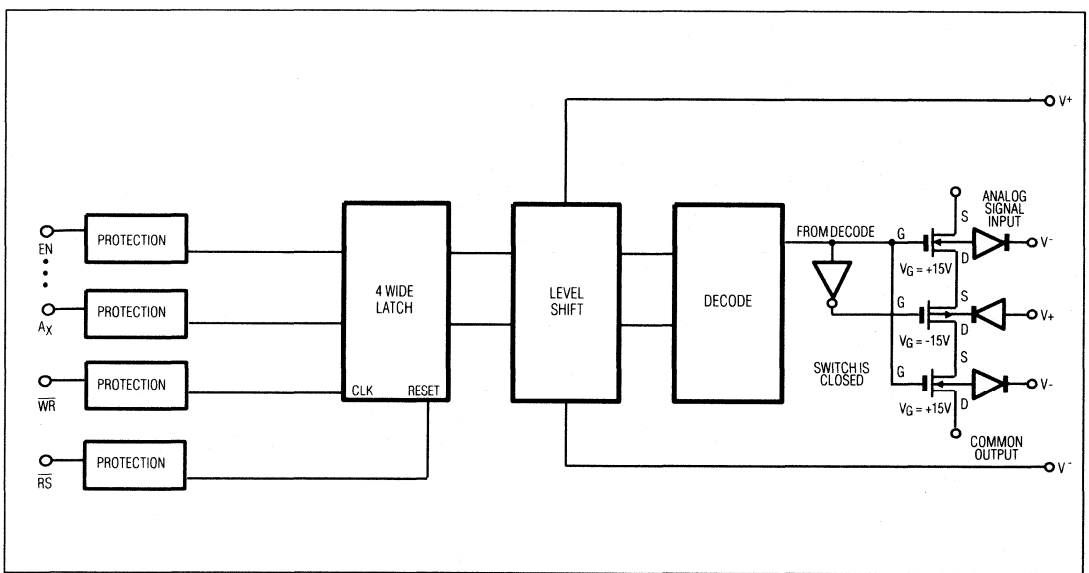
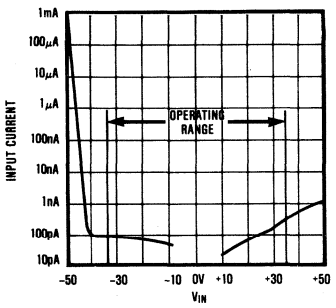


Figure 12. Simplified Internal Structure

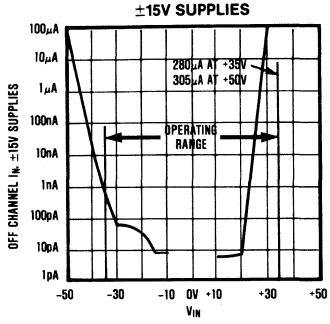
Fault-Protected Analog Multiplexer with Latch

Typical Operating Characteristics

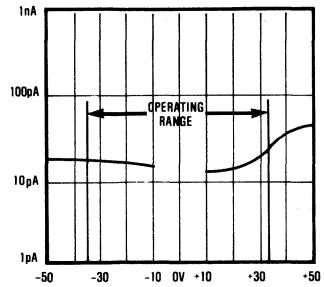
INPUT LEAKAGE VS. INPUT VOLTAGE WITH $V^+ = V^- = 0V$



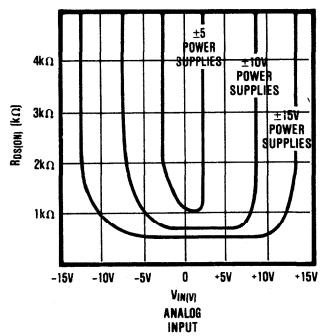
OFF CHANNEL LEAKAGE CURRENT VS. INPUT VOLTAGE WITH ±15V SUPPLIES



OUTPUT LEAKAGE VS. OFF CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$R_{DS(ON)}$ VS. INPUT VOLTAGE



Applications

Operation with Supply Voltages Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX368/369 limits the output voltage to about 1.5V below $+V_{SUP}$ and about 3V above $-V_{SUP}$. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The Typical Operating Characteristics graphs show typical $R_{DS(ON)}$ for ±15V, ±10V, and ±5V power supplies. Maxim guarantees the MAX368/369 for operation from ±4.5V to ±18V supplies. The switching delays increase by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX368/369 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold will remain approximately 1.6V above the GROUND pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between $+V_{SUP}$ and $-V_{SUP}$. Connect $-V_{SUP}$ to 0V when operating with a +9V to +22V single supply.

The MAX368/369 digital threshold is relatively independent of the power supply voltages, going from a typical 1.6V when $+V_{SUP}$ is 15V to 1.5V typical with a 5V $+V_{SUP}$. This means that Maxim's MAX368/369 will operate with standard TTL logic levels, even with ±5V power supplies. In all cases, the threshold of the Enable pin is the same as the other logic inputs.

Operation as a Demultiplexer

The MAX368/369 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX368/369 provide both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Fault-Protected Analog Multiplexer with Latch

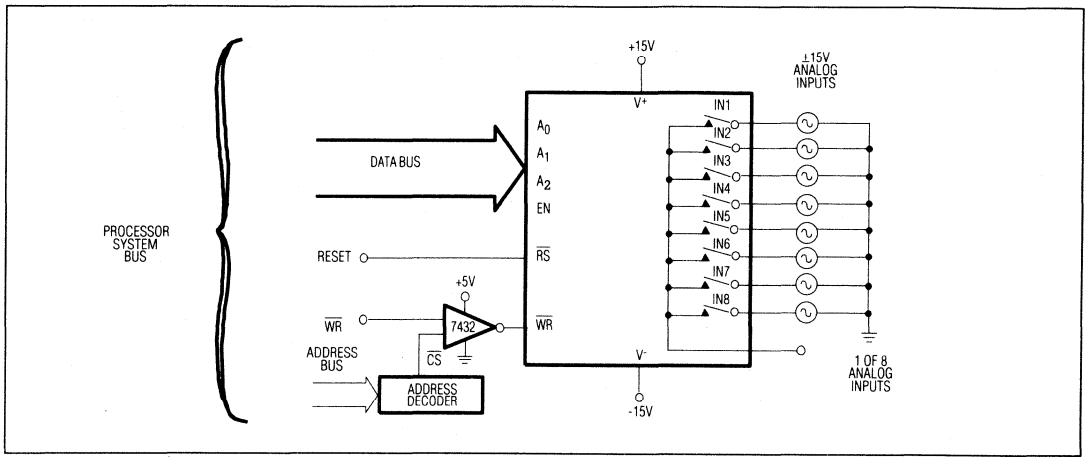


Figure 13. Bus Interface

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage for the MAX368 and MAX369. Note that since the channels are well matched, the differential charge injection for the MAX368/369 is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break-before-make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as that shown in Figure 13, the dominant delay is not the switching time of the MAX368/MAX369 multiplexer but is the settling time of the following amplifier and sample/hold. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output approximately doubles the settling time for 0.01% accuracy settling.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of approximately -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the GROUND pin.

Table 1A. MAX368 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge
±5V	+1.7V 0V -1.7V	+100pC +70pC +45pC
±10V	+5V 0V -5V	+200pC +130pC +60pC
±15V	+10V 0V -10V	+300pC +180pC +50pC

Test Conditions: C_L = 1000pF on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2$ = 0V, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX369 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A - B
±5V	+1.7V 0V -1.7V	+105pC +73pC +48pC	+107pC +48pC +50pC	-2pC -1pC -2pC
±10V	+5V 0V -5V	+215pC +135pC +62pC	+220pC +139pC +63pC	-5pC -4pC -1pC
±15V	+10V 0V -10V	+325pC +180pC +55pC	+330pC +185pC +55pC	-5pC -5pC 0pC

Test Conditions: C_L = 1000pF on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A_1 = 0V, A_0 is toggled from 0V to 3V at a 2kHz rate.

The digital inputs can also be driven with CMOS logic levels swinging from either +V_{SUP} to –V_{SUP} or from +V_{SUP} to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1µA. The digital inputs are protected from ESD by a 30V zener diode between the input and +V_{SUP}, and can be driven ±6V beyond the supplies without drawing excessive current.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies, the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX368/369 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX368/369 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases, since the load driven by the MAX368/369 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled.

When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GROUND and –V_{SUP} pins. The groundplane formed by these lines is continued onto the MAX368/369 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. TYPICAL OFF ISOLATION REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: V_{IN} = 20V_{PK-PK} at the tabulated frequency, R_L = 1.5k between OUT and ground, EN = 0V.

$$OIRR = 20\ Log\ \frac{20\ V_{PK-PK}}{V_{OUT\ (PK-PK)}}$$

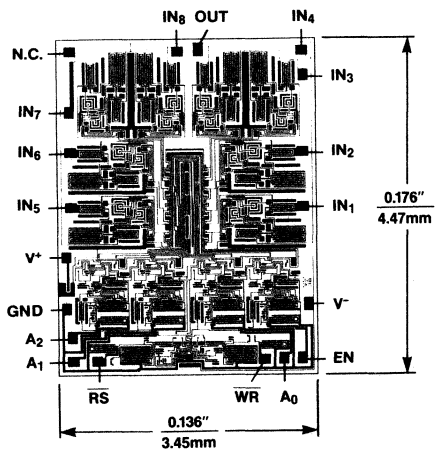
Table 2B. TYPICAL CROSSTALK REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
R_L = 1.5k	70dB	68dB	64dB
R_L = 10k	62dB	46dB	42dB

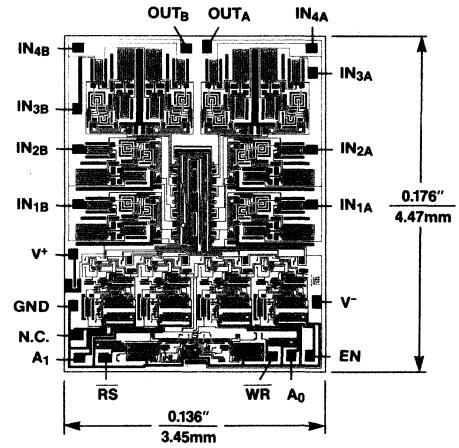
Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, A_0 = A_1 = A_2 =0V (Channel 1 selected). 20V_{PK-PK} at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Chip Topographies

MAX368



MAX369



MAXIM

High Voltage, Fault-Protected Analog Multiplexers

General Description

Maxim's MAX378 is an 8 channel single-ended (1 of 8) multiplexer with fault protection, and the MAX379 is a 4 channel differential (2 of 8) multiplexer with fault protection. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significant fault protection. If the power supplies to the fault-protected multiplexers are inadvertently turned off while input voltages are still applied, *all* channels in the multiplexers are turned off, and only a few nanoamperes of leakage current will flow into the inputs. This protects not only the multiplexers and the circuitry driven by the multiplexers, but also protects the sensors or signal sources which drive the multiplexers.

The series N-channel, P-channel, N-channel protection structure has two significant advantages over the simple current limiting protection scheme of the industry's first generation fault-protected multiplexers. First, the Maxim protection scheme limits fault currents to nanoamp leakage values rather than many milliamperes. This prevents damage to sensors or other sensitive signal sources. Second, the MAX378/379 fault-protected multiplexers can withstand a *continuous* ±60V input, unlike the first generation which had a continuous ±35V input limitation imposed by power dissipation considerations.

All digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power dissipation is less than 2 milliwatts.

Applications

Data Acquisition Systems

Industrial and Process Control Systems

Avionics Test Equipment

Signal routing between Systems

Features

- **Fault Input Voltage ±75V with Power Supplies Off**
- **Fault Input Voltage ±60V with ±15V Power Supplies**
- **All Switches Off with Power Supplies Off**
- **On Channel Turns OFF if Overvoltage Occurs on Input or Output**
- **Only Nanoamperes of Input Current Under All Fault Conditions**
- **No Increase in Supply Currents Due to Fault Conditions**
- **Latchup-proof Construction**
- **Operates From ±4.5V to ±18V Supplies**
- **All Digital Inputs are TTL and CMOS Compatible**
- **Low-Power Monolithic CMOS Design**

Ordering Information

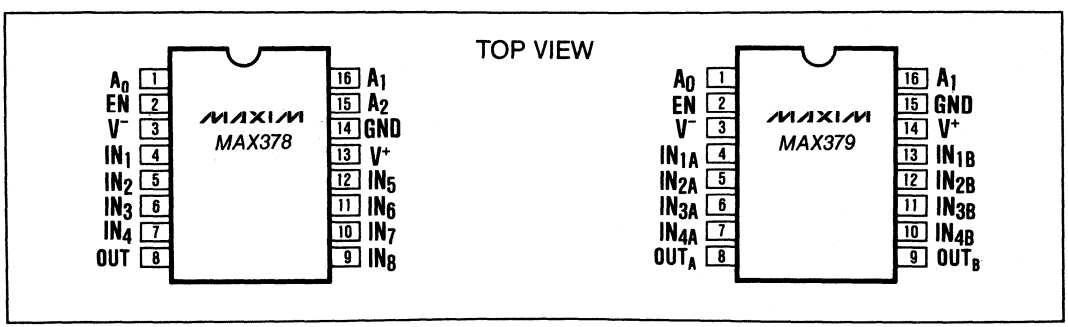
PART	TEMP. RANGE	PACKAGE
MAX378CPE	0°C to +70°C	16 Lead Plastic DIP
MAX378CWE	0°C to +70°C	16 Lead Wide SO
MAX378CJE	0°C to +70°C	16 Lead CERDIP
MAX378EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX378EWE	-40°C to +85°C	16 Lead Wide SO
MAX378EJE	-40°C to +85°C	16 Lead CERDIP
MAX378MJE	-55°C to +125°C	16 Lead CERDIP
MAX378MLP*	-55°C to +125°C	20 Lead LCC
MAX378C/D**	0°C to +70°C	Dice
MAX379CPE	0°C to +70°C	16 Lead Plastic DIP
MAX379CWE	0°C to +70°C	16 Lead Wide SO
MAX379CJE	0°C to +70°C	16 Lead CERDIP

Ordering Information continued on page 10.

* Contact Factory for availability.

** The substrate may be allowed to float or be tied to V^+ (JI CMOS).

Pin Configurations



High Voltage, Fault-Protected Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins ..... +44V
V^+ to Ground ..... +22V
V^- to Ground ..... -22V
Digital Input Overvoltage:
V_{EN}, V_A { V^+ ..... +4V; V^- ..... -4V
Analog Input with Multiplexer Power On ..... ±65V
{ Recommended Power Supplies } V^+ ..... +15V; V^- ..... -15V
Analog Input with Multiplexer Power Off ..... ±80V

Continuous Current, IN or OUT 20mA
Peak Current, IN or OUT
(Pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (Note 1) (CERDIP) 1.28W
Operating Temperature Range:
MAX378/379M ..... -55°C to +125°C
MAX378/379C ..... 0°C to +70°C
MAX378/379E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +75°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +70°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	$r_{DS(ON)}$	V_{OUT} = ±10V, I_{IN} = 100µA V_{AL} = 0.8V, V_{AH} = 2.4V	+25°C Full		2.0 3.0	3.0 4.0		2.0 3.0	3.5 4.0	kΩ
OFF Input Leakage Current	$I_{IN(OFF)}$	V_{IN} = ± 10V, V_{OUT} = ∓10V V_{EN} = 0.8V (Note 6)	+25°C Full	-0.5 -50	0.03	0.5 50	-1.0 -50	0.03	1.0 50	nA
OFF Output Leakage Current	$I_{OUT(OFF)}$	V_{OUT} = ±10V, V_{IN} = ∓10V V_{EN} = 0.8V MAX378 (Note 6) MAX379	+25°C Full Full	-1.0 -200 -100	0.1	1.0 200 100	-2.0 -200 -100	0.1	2.0 200 100	nA
ON Channel Leakage Current	$I_{OUT(ON)}$	$V_{IN(ALL)}$ = V_{OUT} = ±10V (Note 5) V_{AH} = V_{EN} = 2.4V MAX378 V_{AL} = 0.8V MAX379	+25°C Full Full	-2.0 -200 -100	0.1	2.0 200 100	-5.0 -200 -100	0.1	5.0 200 100	nA
Analog Signal Range	V_{AN}	(Note 2)	Full	-15		+15	-15		+15	V
Differential, OFF Output Leakage Current	I_{DIFF}	MAX379 only (Note 6)	Full	-50		50	-50		50	nA
FAULT										
Output Leakage Current (with Input Overvoltage)	$I_{OUT(OFF)}$	V_{OUT} = 0V (Note 3) V_{IN} = ±60V	+25°C Full		20	10		20	20	nA µA
Input Leakage Current (with Overvoltage)	$I_{IN(OFF)}$	V_{IN} = ±60V, V_O = ±10V (Note 3)	+25°C			25			40	µA
Input Leakage Current (with Power Supplies Off)	$I_{IN(OFF)}$	V_{IN} = ±75V, V_{EN} = V_O = 0V A_0 = A_1 = A_2 = 0V or 5V	+25°C			10			20	µA
CONTROL										
Input Low Threshold	V_{AL}	(Note 4)	Full			0.8			0.8	V
Input High Threshold	V_{AH}	(Note 4)	Full	2.4			2.4			V
Input Leakage Current (High or Low)	I_A	V_A = 5V or 0V (Note 5)	Full	-1.0		1.0	-1.0		1.0	µA

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +15V, V^- = -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +70°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC										
Access Time	t_A	(Figure 1)	+25°C		0.5	1.0		0.5	1.0	µs
Break-Before-Make Delay (Figure 2)	t_{ON}-t_{OFF}	V_{EN} = +5V, V_{IN} = ±10V A_0, A_1, A_2 Strobed	+25°C	25	200		25	200		ns
Enable Delay (ON)	$t_{ON(EN)}$	(Figure 3)	+25°C Full		400	750 1000		400	1000 1500	ns
Enable Delay (OFF)	$t_{OFF(EN)}$	(Figure 3)	+25°C Full		300	500 1000		300	 1000	ns
Settling Time (0.1%) (0.01%)	t_{SETT}		+25°C		1.2 3.5			1.2 3.5		µs
"OFF Isolation"	$OFF_{(ISO)}$	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V = $7V_{RMS}$, f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	$C_{IN(OFF)}$		+25°C		5			5		pF
Channel Output Capacitance	$C_{OUT(OFF)}$	MAX378 MAX379	+25°C		25 12			25 12		pF
Digital Input Capacitance	C_A		+25°C		5			5		pF
Input to Output Capacitance	$C_{DS(OFF)}$		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I^+	V_{EN} = 0.8V, or 2.4V All V_A = 0V or 5V	+25°C Full		0.1 0.3	0.6 0.7		0.2 0.5	1.0 1.0	mA
Negative Supply Current	I^-	V_{EN} = 0.8V or 2.4V All V_A = 0V or 5V	+25°C Full		0.01 0.02	0.1 0.2		0.01 0.02	0.1 0.1	mA
Power Supply Range for Continuous Operation	V_{OP}	(Note 7)	+25°C	±4.5		±18	±4.5		±18	V

Note 2: When the analog signal exceeds +13.5V or -12V the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
Note 3: The value shown is the steady state value. The transient leakage is typically 50µA. See detailed description.
Note 4: Guaranteed by other static parameters.
Note 5: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.
Note 6: Leakage currents not tested at T_A = cold temp.
Note 7: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

High Voltage, Fault-Protected Analog Multiplexers

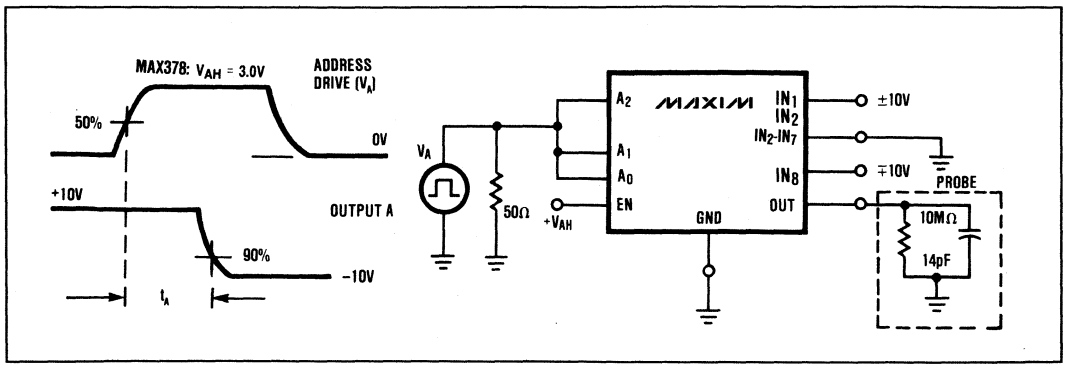


Figure 1. Access Time vs. Logic Level (High)

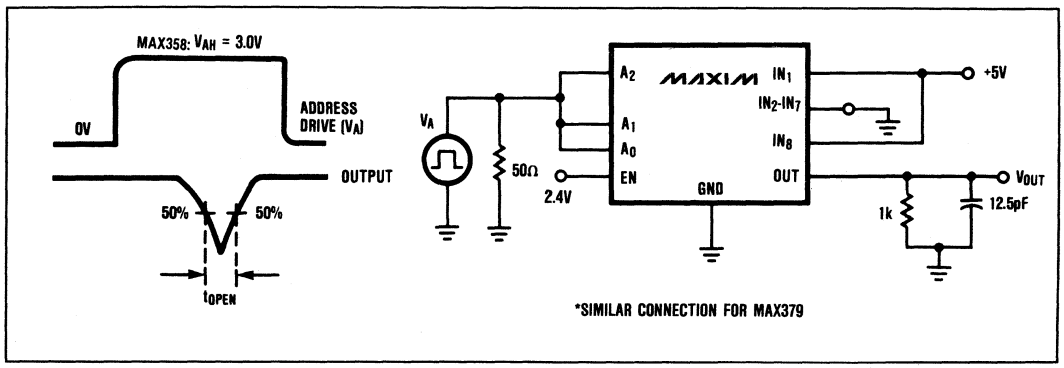


Figure 2. Break-Before-Make Delay (t_{OPEN})

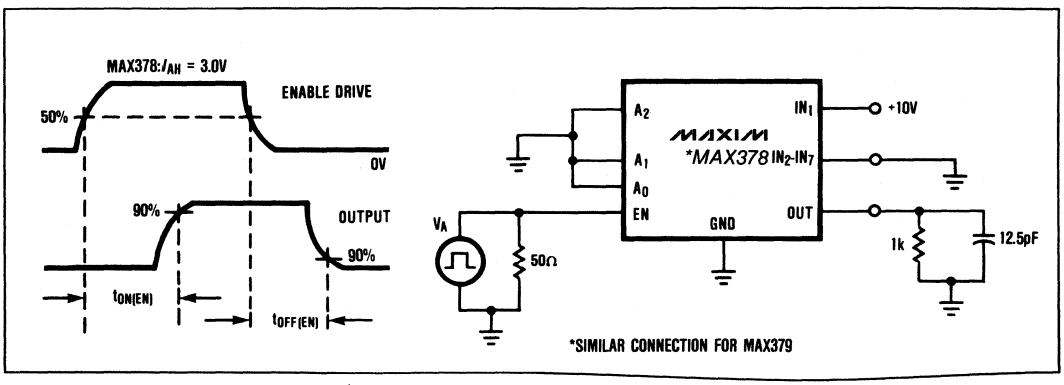


Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

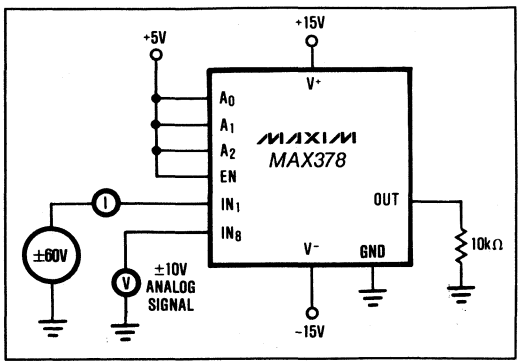


Figure 4. Input Leakage Current (Overvoltage)

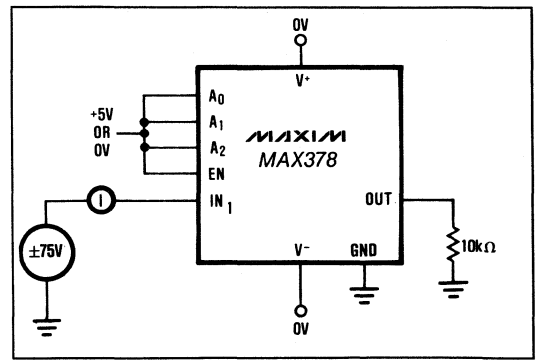
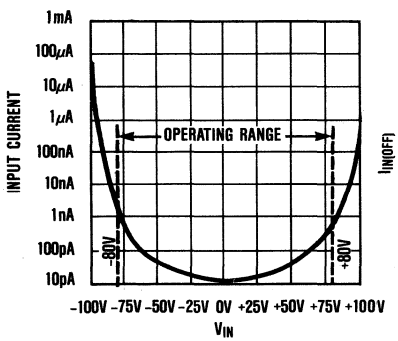


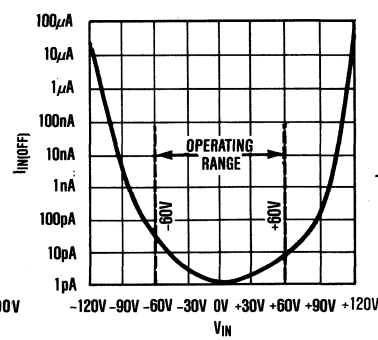
Figure 5. Input Leakage Current (with Power Supplies OFF)

Typical Operating Characteristics

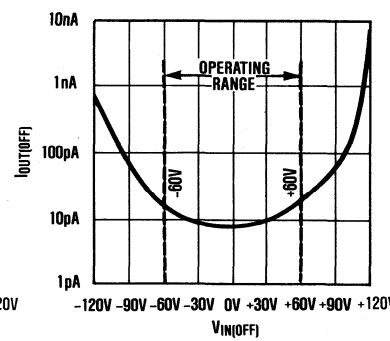
INPUT LEAKAGE vs INPUT VOLTAGE WITH $V^+ = V^- = 0V$



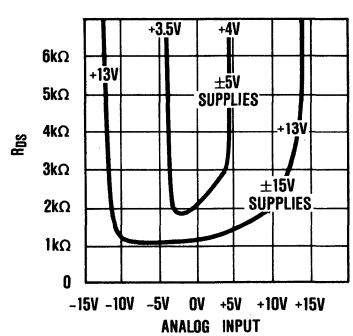
OFF CHANNEL LEAKAGE CURRENT vs INPUT VOLTAGE WITH ±15V SUPPLIES



OUTPUT LEAKAGE vs OFF CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$R_{DS(ON)}$ vs ANALOG INPUT VOLTAGE



NOTE: Typical $R_{DS(ON)}$ match @ +10V Analog in (±15V supplies) = 2% for lowest to highest $R_{DS(ON)}$ channel; @ -10V Analog in, match = 3%.

High Voltage, Fault-Protected Analog Multiplexers

TRUTH TABLE—MAX378

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE—MAX379

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Note: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

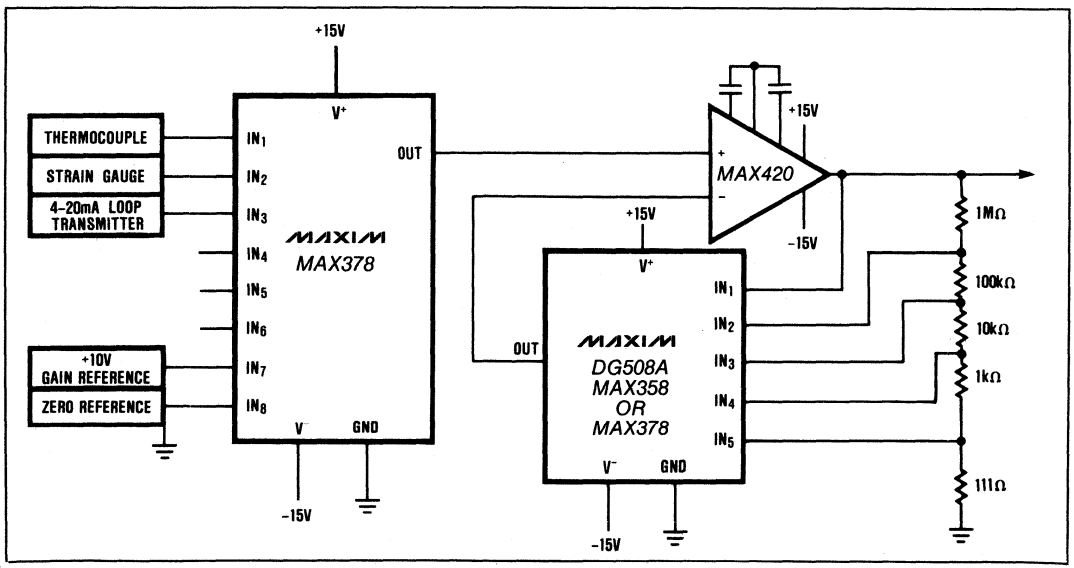


Figure 6. Typical Data Acquisition Front End

Typical Applications

Figure 6 shows a typical data acquisition system using the MAX378 multiplexer. Since the multiplexer is driving a high impedance input, its error is a function of its own resistance ($R_{DS(ON)}$) times the multiplexer leakage current ($I_{OUT(ON)}$) and the ampliifer bias current (I_{BIAS}):

$$V_{ERR} = R_{DS(ON)} \times (I_{OUT(ON)} + I_{BIAS}\ (MAX420))$$
$$= 2.0k \times (2nA + 30pA)$$
$$= 18.0\mu V \text{ maximum error}$$

In most cases, this error is low enough that preamplification of input signals is not needed, even with very low level signals, such as 40μV/°C from type J thermocouples.

In systems with fewer than 8 inputs, an unuse . channel can be connected to the system ground reference point for software zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data acquisition system as well.

A MAX420 precision op amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed 5μV unadjusted offset of the MAX420 maintains high signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data acquisition system, normally a Sample/Hold and A/D. Since the gain-changing multiplexer is not

connected to the external sensors, it can be either a DG508A multiplexer or the fault protected MAX358 or MAX378.

Input switching, however, must be done with a fault-protected MAX378 multiplexer to provide the level of protection and isolation required with most data acquisition inputs. Since external signal sources may continue to supply voltage when the multiplexer and system power are turned off, non-fault protected multiplexers, or even first-generation fault protected devices, will allow many milliamps of fault current to flow from outside sources into the multiplexer. The result could be damage to either the sensors or the multiplexer. A non-fault protected multiplexer will also allow input overvoltages to appear at its output, perhaps damaging Sample/Holds or A/Ds. Such input overdrives may also cause input-to-input shorts, allowing the high current output of one sensor to possibly damage another.

The MAX378 eliminates all of the above problems since it not only limits its output voltage to safe levels, with or without power applied (V^+ and V^-), but also turns all channels off when power is removed, drawing only sub-microamp fault currents from the inputs, and maintaining isolation between inputs for continuous input levels up to ±75V with power supplies off.

Detailed Description

Fault Protection Circuitry

MAX378/379 are fully fault-protected for continuous input voltages up to ±60V, whether or not the V^+ and V^- power supplies are present. These devices use a "series FET" switching scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels.

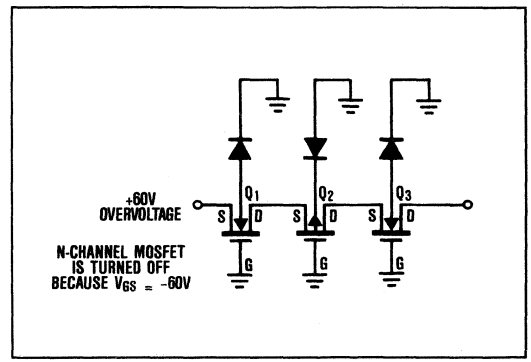


Figure 8. +60V Overvoltage with Multiplexer Power OFF

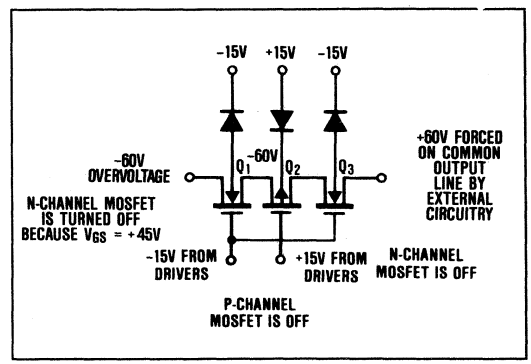


Figure 9. -60V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

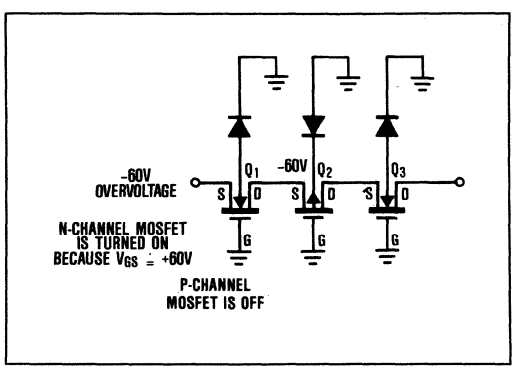


Figure 7. -60V Overvoltage with Multiplexer Power OFF

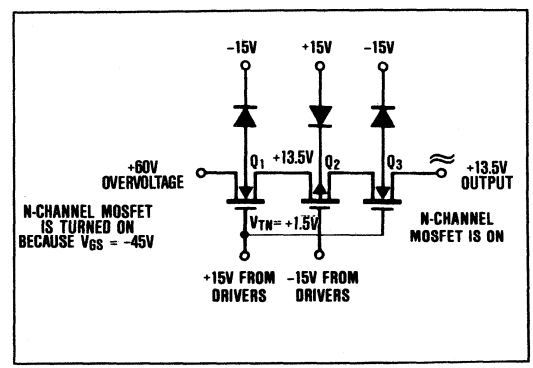


Figure 10. +60V Overvoltage Input to the ON Channel

High Voltage, Fault-Protected Analog Multiplexers

Figures 7 and 8 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -60V input, N-channel FET Q1 is turned on by the +60V gate-to-source voltage. The P-channel device (Q2), however, has +60V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +60V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Figure 9 shows the condition of an OFF channel with V^+ and V^- present. As with Figures 7 and 8, either an N-channel or a P-channel device will be off for any input voltage from -60V to +60V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages that fault current will initially be 40 or 50μA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 10 shows the condition of the ON channel with V^+ and V^- present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds V^+ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than V^- minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies.

The Typical Operating Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated input of these devices is ±65V, the MAX378/379 typically have excellent performance up to ±75V, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX378/379 provide superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage. Note that since the channels are well matched, the differential charge injection for the MAX379 is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break-before-make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as Figure 6, the dominant delay is not the switching time of the MAX378 multiplexer, but is the settling time of the following amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltage Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX378 limits the output voltage to about 1.5V below V^+ and about 3V above V^-. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The Typical Operating Characteristics graphs show typical $R_{DS(ON)}$ for ±15V , ±10V, and ±5V power supplies. Maxim tests and guarantees the MAX378/379 for operation from ±4.5V to ±18V supplies. The switching delays are increased by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX378/379 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold will remain approximately 1.6V above the Ground pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between V^+ and V^-. Connect V^- to 0V when operating with a +9V to +22V single supply.

This means that the Maxim MAX378/379 will operate with standard TTL logic levels, even with ±5V power supplies. In all cases, the threshold of the ENable pin is the same as the other logic inputs.

Table 1A. MAX378 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge
±5V	+1.7V	+100pC
	0V	+70pC
	-1.7V	+45pC
±10V	+5V	+200pC
	0V	+130pC
	-5V	+60pC
±15V	+10V	+500pC
	0V	+180pC
	-10V	+50pC

Test Conditions: C_L = 1000pF on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2 = 0V$, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX379 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A-B
±5V	+1.7V	+105pC	+107pC	-2pC
	0V	+73pC	+74pC	-1pC
	-1.7V	+48pC	+50pC	-2pC
±10V	+5V	+215pC	+220pC	-5pC
	0V	+135pC	+139pC	-4pC
	-5V	+62pC	+63pC	-1pC
±15V	+10V	+525pC	+530pC	-5pC
	0V	+180pC	+185pC	-5pC
	-10V	+55pC	+55pC	0pC

Test Conditions: C_L = 1000pF on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A_1 = 0V, A_0 is toggled from 0V to 3V at a 2kHz rate.

Digital Interface Levels

The typical digital threshold of both the address lines and the ENable pin is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the Ground pin.

The digital inputs can also be driven with CMOS logic levels swinging from either V^+ to V^- or from V^+ to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1μA. The digital inputs are protected from ESD by a 30V zener diode between the input and V^+, and can be driven ±4V beyond the supplies without drawing excessive current.

Operation as a Demultiplexer

The MAX378/379 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX378/379 provide both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX378 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX378 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases since the load driven by the MAX378 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the Ground and V^- pins. The groundplane formed by these lines is continued onto the MAX378/9 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. Typical Off Isolation Rejection Ratio

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: V_{IN} = $20V_{PK-PK}$ at the tabulated frequency, R_L = 1.5k between OUT and Ground, EN = 0V.

$$OIRR = 20\ Log\ \frac{20V_{PK-PK}}{V_{OUT\ (PK-PK)}}$$

Table 2B. Typical Crosstalk Rejection Ratio

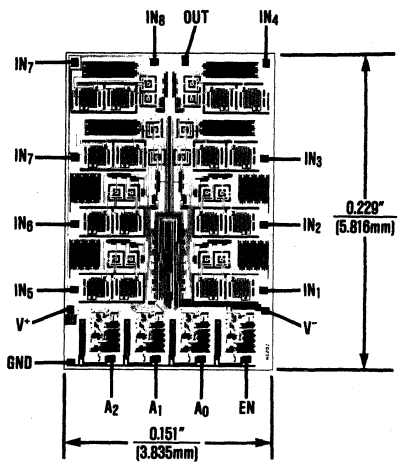
Frequency	100kHz	500kHz	1MHz
F_L = 1.5k	70dB	68dB	64dB
R_L = 10k	62dB	46dB	42dB

Test Conditions: Specified R_L connected from OUT to Ground, EN = +5V, A_0 = A_1 = A_2 = +5V (Channel 1 selected). $20V_{PK-PK}$ at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

High Voltage, Fault-Protected Analog Multiplexers

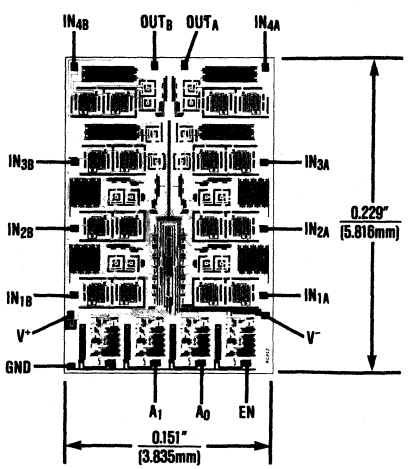
Chip Topographies

MAX378



NOTE: Connect substrate to V+ or leave it floating.

MAX379



NOTE: Connect substrate to V+ or leave it floating.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX379EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX379EWE	-40°C to +85°C	16 Lead Wide SO
MAX379EJE	-40°C to +85°C	16 Lead CERDIP
MAX379MJE	-55°C to +125°C	16 Lead CERDIP
MAX379MLP*	-55°C to +125°C	20 Lead LCC
MAX379C/D**	0°C to +70°C	Dice

* Contact Factory for availability.

** The substrate may be allowed to float or be tied to V+ (JI CMOS).

ADVANCE INFORMATION

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MAXIM

Dual High-Speed Analog Switches

General Description

The MXDG401/403/405 are dual high-speed analog switches. Both the MXDG401 and MXDG405 are normally closed, (SPST, NC) and (DPST, NC), respectively. The MXDG403 has one normally-open and one normally-closed pole (DPST). All three parts offer low on resistance (35Ω max) over the analog range, fast switching (100ns max), and low power dissipation (0.035mW max). Logic inputs are TTL compatible.

The MXDG401/403/405 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

- ♦ **35Ω Max $r_{DS(ON)}$**
- ♦ **100ns Max Switching**
- ♦ **0.035mW Max Power Dissipation**
- ♦ **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- ♦ **+30V Peak-to-Peak Switch-Off Blocking Capacity**

Ordering Information

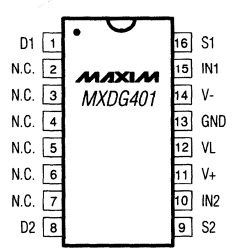
PART	TEMP. RANGE	PIN-PACKAGE
MXDG401C/D	0°C to +70°C	Dice*
MXDG401DJ	-40°C to +85°C	16 Plastic DIP
MXDG401DY	-40°C to +85°C	16 Narrow SO
MXDG401DK	-40°C to +85°C	16 CERDIP
MXDG401AZ	-55°C to +125°C	16 LCC**
MXDG401AK	-55°C to +125°C	16 CERDIP**
MXDG403C/D	0°C to +70°C	Dice*
MXDG403DJ	-40°C to +85°C	16 Plastic DIP
MXDG403DY	-40°C to +85°C	16 Narrow SO
MXDG403DK	-40°C to +85°C	16 CERDIP
MXDG403AZ	-55°C to +125°C	16 LCC**
MXDG403AK	-55°C to +125°C	16 CERDIP**
MXDG405C/D	0°C to +70°C	Dice*
MXDG405DJ	-40°C to +85°C	16 Plastic DIP
MXDG405DY	-40°C to +85°C	16 Narrow SO
MXDG405DK	-40°C to +85°C	16 CERDIP
MXDG405AZ	-55°C to +125°C	16 LCC**
MXDG405AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*

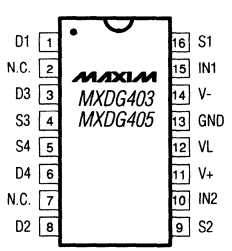
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations

TOP VIEW



DIP/SO



DIP/SO

ADVANCE INFORMATION

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MAXIM

Quad SPST Precision Analog Switches

General Description

The MXDG411/412/413 are quad single-pole-single-throw (SPST) precision analog switches. The MXDG411 is normally open (SPST, NO), while the MXDG412 is normally closed (SPST, NC). The MXDG413 has two normally-open and two normally-closed switches. All three parts offer low on resistance (35Ω max) over the analog range, fast switching (145ns max), and low power dissipation (0.035mW max). Logic inputs are TTL compatible.

The MXDG411/412/413 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

- ♦ **35Ω Max $r_{DS(ON)}$**
- ♦ **145ns Max Switching**
- ♦ **0.035mW Max Power Dissipation**
- ♦ **CMOS Logic Compatible**
- ♦ **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- ♦ **+30V Peak-to-Peak Switch-Off Blocking Capacity**

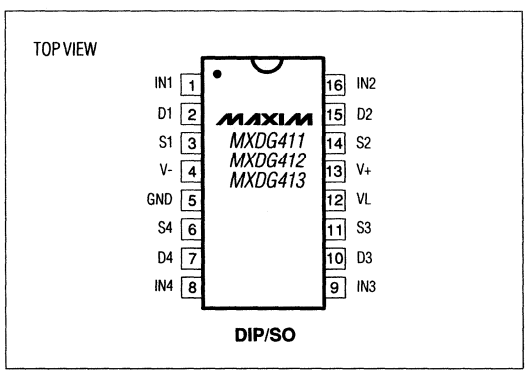
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXDG411C/D	0°C to +70°C	Dice*
MXDG411DJ	-40°C to +85°C	16 Plastic DIP
MXDG411DY	-40°C to +85°C	16 Narrow SO
MXDG411DK	-40°C to +85°C	16 CERDIP
MXDG411AK	-55°C to +125°C	16 CERDIP**
MXDG412C/D	0°C to +70°C	Dice*
MXDG412DJ	-40°C to +85°C	16 Plastic DIP
MXDG412DY	-40°C to +85°C	16 Narrow SO
MXDG412DK	-40°C to +85°C	16 CERDIP
MXDG412AK	-55°C to +125°C	16 CERDIP**
MXDG413C/D	0°C to +70°C	Dice*
MXDG413DJ	-40°C to +85°C	16 Plastic DIP
MXDG413DY	-40°C to +85°C	16 Narrow SO
MXDG413DK	-40°C to +85°C	16 CERDIP
MXDG413AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



ADVANCE INFORMATION

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MAXIM

Precision MiniDIP Analog Switches

General Description

The MXDG417/418/419 are precision miniDIP analog switches. The MXDG417 is normally open (SPST, NO), while the MXDG418 is normally closed (SPST, NC). The MXDG419 has one normally-open and one normally-closed pole (DPST). All three parts offer low on resistance (35Ω max) over the analog range, fast switching (145ns max), and low power dissipation (0.035mW max). Logic inputs are TTL compatible.

The MXDG417/418/419 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

- ♦ **35Ω Max $r_{DS(ON)}$**
- ♦ **145ns Max Switching**
- ♦ **0.035mW Max Power Dissipation**
- ♦ **CMOS Logic Compatible**
- ♦ **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- ♦ **+30V Peak-to-Peak Switch-Off Blocking Capacity**

Ordering Information

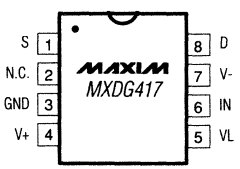
PART	TEMP. RANGE	PIN-PACKAGE
MXDG417C/D	0°C to +70°C	Dice*
MXDG417DJ	-40°C to +85°C	8 Plastic DIP
MXDG417DY	-40°C to +85°C	8 SO
MXDG417DK	-40°C to +85°C	8 CERDIP
MXDG417AK	-55°C to +125°C	8 CERDIP**
MXDG418C/D	0°C to +70°C	Dice*
MXDG418DJ	-40°C to +85°C	8 Plastic DIP
MXDG418DY	-40°C to +85°C	8 SO
MXDG418DK	-40°C to +85°C	8 CERDIP
MXDG418AK	-55°C to +125°C	8 CERDIP**
MXDG419C/D	0°C to +70°C	Dice*
MXDG419DJ	-40°C to +85°C	8 Plastic DIP
MXDG419DY	-40°C to +85°C	8 SO
MXDG419DK	-40°C to +85°C	8 CERDIP
MXDG419AK	-55°C to +125°C	8 CERDIP**

* *Contact factory for dice specifications.*

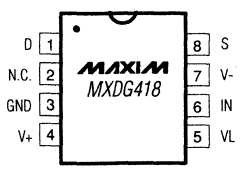
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations

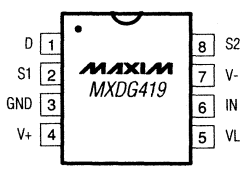
TOP VIEW



DIP/SO



DIP/SO



DIP/SO

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MAXIM

Dual CMOS Analog Switches

General Description

The MXDG421/423/425 are dual monolithic analog switches. The MXDG421 is normally closed (SPST, NC), while the MXDG423 (SPDT) and MXDG425 (DPST) have two normally-closed and two normally-open poles. These devices feature latchable logic inputs that simplify interfacing with microprocessors. All three switches offer low on resistance (35Ω max) over the analog range, fast switching (200ns max), and low power dissipation (0.035mW max). Logic inputs are TTL compatible.

The MXDG421/423/425 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

- **35Ω Max $r_{DS(ON)}$**
- **200ns Max Switching**
- **0.035mW Max Power Dissipation**
- **CMOS Logic Compatible**
- **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- **+30V Peak-to-Peak Switch-Off Blocking Capacity**

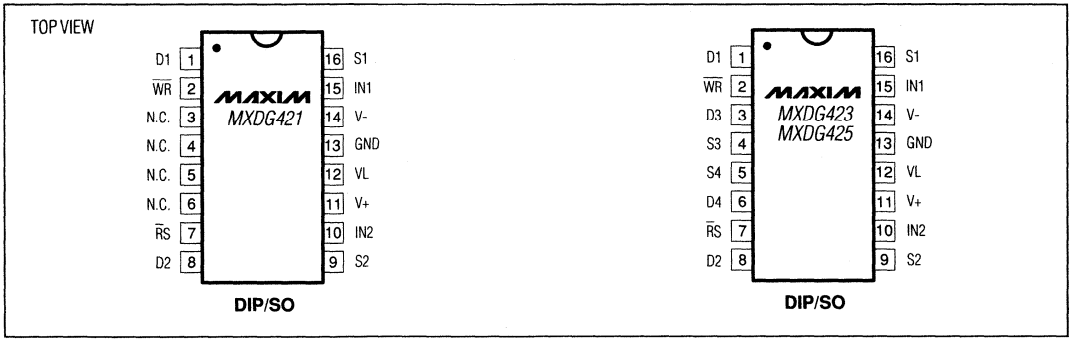
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXDG421C/D	0°C to +70°C	Dice*
MXDG421DJ	-40°C to +85°C	16 Plastic DIP
MXDG421DY	-40°C to +85°C	16 Narrow SO
MXDG421DK	-40°C to +85°C	16 CERDIP
MXDG421AK	-55°C to +125°C	16 CERDIP**
MXDG423C/D	0°C to +70°C	Dice*
MXDG423DJ	-40°C to +85°C	16 Plastic DIP
MXDG423DY	-40°C to +85°C	16 Narrow SO
MXDG423DK	-40°C to +85°C	16 CERDIP
MXDG423AK	-55°C to +125°C	16 CERDIP**
MXDG425C/D	0°C to +70°C	Dice*
MXDG425DJ	-40°C to +85°C	16 Plastic DIP
MXDG425DY	-40°C to +85°C	16 Narrow SO
MXDG425DK	-40°C to +85°C	16 CERDIP
MXDG425AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



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MAXIM

Quad SPST Analog Switches

General Description

The MXDG441/MXDG442 are quad single-pole-single-throw (SPST) analog switches. The MXDG441 is normally open (SPST, NO), while the MXDG442 is normally closed (SPST, NC). Both parts offer low on resistance (80Ω max) over the analog range, fast switching (120ns max), and low power dissipation (1.6mW max). Logic inputs are TTL compatible.

The MXDG441/MXDG442 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

- **80Ω Max $r_{DS(ON)}$**
- **120ns Max Switching**
- **1.6mW Max Power Dissipation**
- **CMOS Logic Compatible**
- **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- **+30V Peak-to-Peak Switch-Off Blocking Capacity**

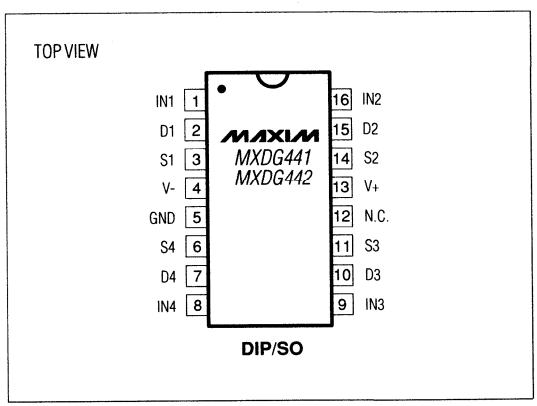
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXDG441C/D	0°C to +70°C	Dice*
MXDG441DJ	-40°C to +85°C	16 Plastic DIP
MXDG441DY	-40°C to +85°C	16 Narrow SO
MXDG441DK	-40°C to +85°C	16 CERDIP
MXDG441AK	-55°C to +125°C	16 CERDIP**
MXDG442C/D	0°C to +70°C	Dice*
MXDG442DJ	-40°C to +85°C	16 Plastic DIP
MXDG442DY	-40°C to +85°C	16 Narrow SO
MXDG442DK	-40°C to +85°C	16 CERDIP
MXDG442AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



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MAXIM

Quad SPST Analog Switches

General Description

The MXDG444/MXDG445 are quad single-pole-single-throw (SPST) analog switches. The MXDG444 is normally open (SPST, NO), while the MXDG445 is normally closed (SPST, NC). Both parts offer low on resistance (85Ω max) over the analog range, fast switching (120ns max), and low power dissipation (0.035mW max). Logic inputs are TTL compatible.

The MXDG444/MXDG445 are designed with a +44V maximum breakdown voltage rating that allows +30V peak-to-peak switch-off blocking capacity. These switches can be used with a single positive supply (+5V to +30V) or split supplies (±5V to ±20V) while retaining CMOS logic input compatibility and fast switching.

Applications

Sample-and-Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-Up Displays
Military Radios
Battery-Operated Systems

Features

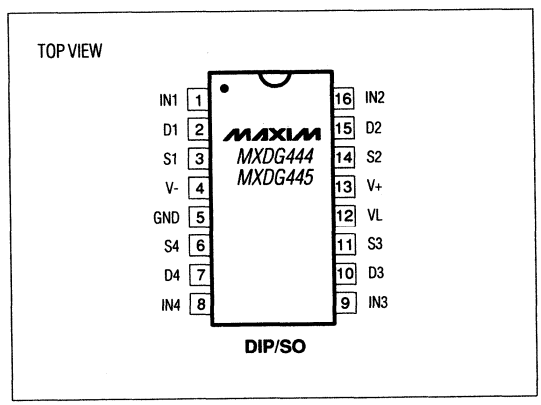
- **85Ω Max $r_{DS(ON)}$**
- **120ns Max Switching**
- **0.035mW Max Power Dissipation**
- **CMOS Logic Compatible**
- **Operation from Single (+5V to +30V) or Bipolar (±5V to ±20V) Supplies**
- **+30V Peak-to-Peak Switch-Off Blocking Capacity**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXDG444C/D	0°C to +70°C	Dice*
MXDG444DJ	-40°C to +85°C	16 Plastic DIP
MXDG444DY	-40°C to +85°C	16 Narrow SO
MXDG444DK	-40°C to +85°C	16 CERDIP
MXDG444AK	-55°C to +125°C	16 CERDIP**
MXDG445C/D	0°C to +70°C	Dice*
MXDG445DJ	-40°C to +85°C	16 Plastic DIP
MXDG445DY	-40°C to +85°C	16 Narrow SO
MXDG445DK	-40°C to +85°C	16 CERDIP
MXDG445AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



MAXIM

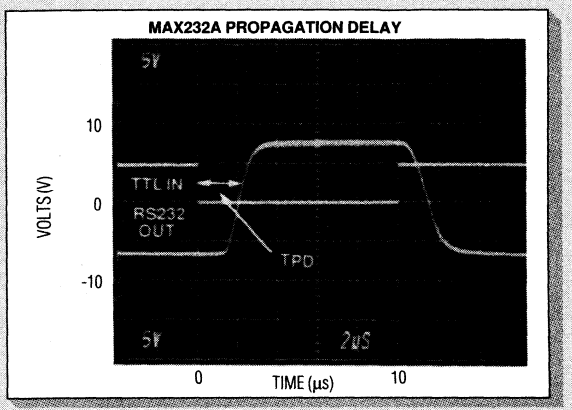
Interface Products

New RS-232 Transceiver Doubles Speed of Existing +5V RS-232 Devices!

Guaranteed Data Rate is 116kbits/sec

Maxim's new MAX232A dual RS-232 transceiver operates on +5V and maintains full compatibility with EIA-232D and CCITT V.28 standards while providing the highest data rates available from any +5V powered RS-232 device; 116kbits/sec guaranteed. And, these limits are guaranteed while driving real loads (2500pF and 3kΩ).

Systems can be smaller and less costly because the MAX232A operates with only 0.1µF charge-pump capacitors, rather than the 10µF capacitors as required with older transceivers. The MAX232A outputs assume a high-impedance state that draws no current from the data lines when the transceiver is turned off.

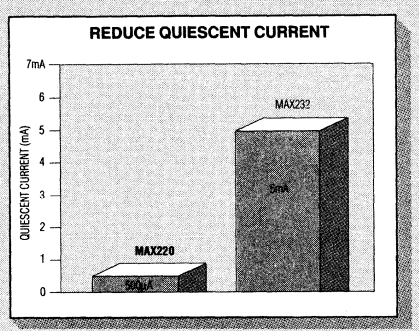


The MAX232A improves propagation delay and symmetry.

RS-232 at 1/10th the Power!

Quiescent Current is Only 500µA

The new MAX220, with the industry-standard MAX232 pinout, meets all the requirements of EIA-232D while dramatically reducing power consumption. The dual transceiver typically draws only 500µA vs. 5mA for CMOS-equivalent transceivers and 14mA for bipolar equivalents. The 2mA maximum supply current for the MAX220 is 10 times lower than bipolar RS-232 transceivers. The reduction in power consumption makes the MAX220 ideal for hand-held instruments and other portable applications.



The MAX220 saves over 22mW of power.

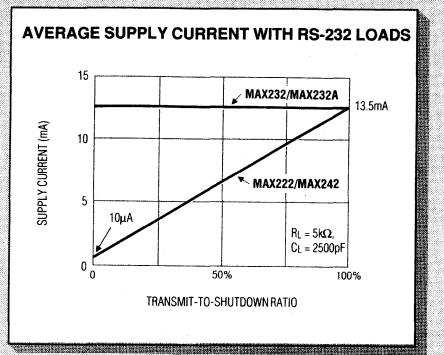
When powered down (V_{CC} = 0V), the MAX220 outputs turn off and draw negligible current from the data lines. Moreover, the MAX220 is guaranteed to operate at data rates up to 20kbits/sec while maintaining full compatibility with EIA-232D and CCITT V.28 standards.

Dual Transceivers Conserve 67mW of Power In Shutdown Mode

New MAX222 and MAX242 Draw Only 10µA Max

The MAX222 and MAX242, operating with space-saving 0.1µF external charge-pump capacitors, are guaranteed for data rates up to 116kbits/sec. These dual transceivers (two drivers and two receivers on each chip) feature a shutdown mode that disables the device and turns off all driver and receiver outputs. Using the shutdown mode, the MAX222 and MAX242 save up to 67mW of power when not receiving or transmitting data by reducing loaded supply current from 13.5mA during normal operation to 10µA in the shutdown mode.

The MAX222 and MAX242 are identical except one pin places the MAX222's drivers and receivers into the shutdown mode. The MAX242 provides separate three-state controls for the driver and receiver outputs, allowing bused (party-line) configurations. And, the MAX242 receivers remain on in the shutdown mode to receive incoming data.



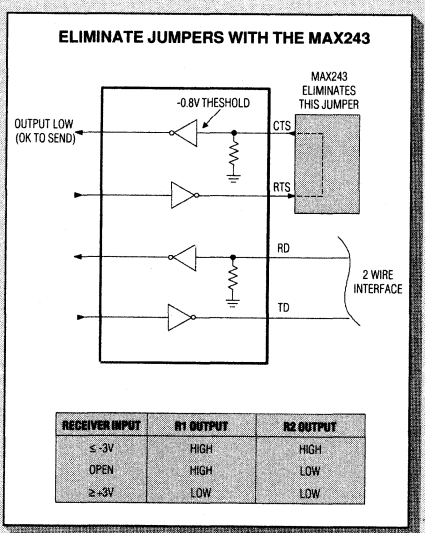
The MAX222 and MAX242 save power in the shutdown mode.

RS-232 Transceiver Simplifies Cabling

Switch between Xon/Xoff and CTS/RTS flow control without changing cables

The MAX243 lets you swap between 2-wire (Xon/Xoff) and 4-wire (CTS/RTS) interfaces without changing cables or adding jumpers. Because one of the two receiver-input thresholds is negative (-0.8V) instead of positive (+1.4V), CTS/RTS flow-control lines can float without interrupting communications.

The receiver output goes high only if its input is actively driven negative. If the input is floating or not driven, the output defaults to the low "OK to send" state. In normal applications, the negative-threshold receiver connects to the data line (TD or RD), and the other 1.4V threshold receiver connects to the control line (DTR, DTS, CTS, RTS). The MAX243 operates with space saving 0.1µF external charge-pump capacitors, and is guaranteed for data rates up to 116kbits/sec.



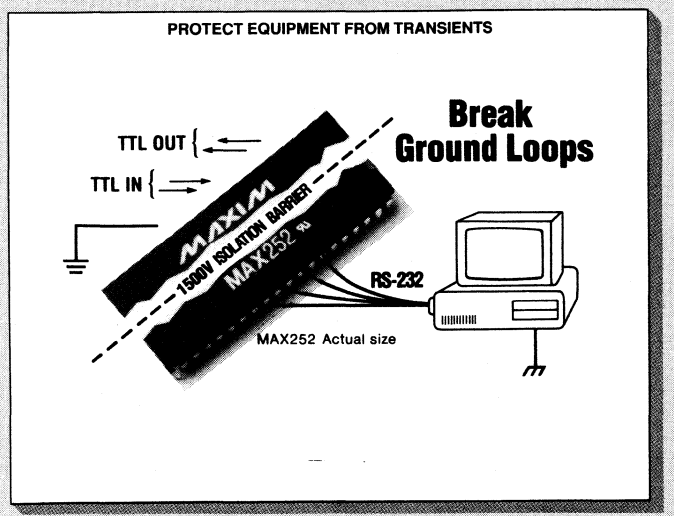
RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

The MAX243 detects open line conditions while operating as a typical RS-232 receiver during normal operation.

Break Ground Loops

Complete Solution in a Standard 40-Pin DIP Package Needs No External Components

Do you need to transmit RS-232 data where very high transient voltages, differential ground potentials, or noise is encountered? The MAX252A and MAX252B are dual, +5V powered RS-232 transceivers that are designed for environments where noise and ground loops are present. The UL recognized MAX252A withstands up to 1500V_{rms} for 1 second, 1260V_{rms} for 1 minute, or 130V_{rms} continuously. The MAX252B, designed to break ground loops, withstands 500V_{rms} for 1 minute or 600V_{rms} for one second. The MAX252 contains all the components necessary for an isolated RS-232 interface in a standard, 40-pin, plastic DIP package including optocouplers, capacitors, and a transformer.



Whether you need to break ground loops or protect your equipment from destructive transients, the MAX252 solves your interface isolation problems.

The MAX252 can operate at a guaranteed 9600bits/sec while meeting EIA-232D and CCITT V.28 specifications. The MAX252 will typically operate at data rates up to 20kbits/sec. A shutdown mode disables the device and lowers power consumption to 50µW when the RS-232 port is not in use. And shutdown places the driver outputs in a high impedance state that draws no current from the data lines.

2

★ FUTURE PRODUCTS ★

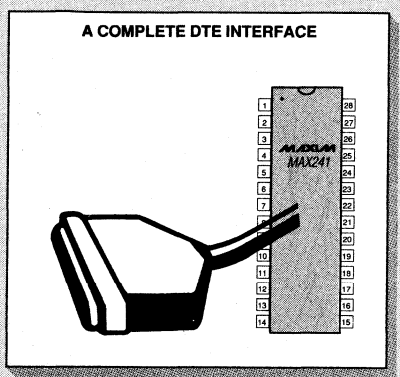
Two IBM PC Serial Ports on a Single Chip

The new MAX249 contains 6 RS-232 drivers and 10 RS-232 receivers to provide two complete DTE (Data Terminal Equipment) RS-232 serial ports on one chip to save board space in space critical applications. The MAX249 meets all EIA-232D specifications and is guaranteed to operate at data rates up to 64kbits/sec. The MAX249 is available in a 44 pin PLCC package and uses space saving 1.0µF external charge pump capacitors.

Nine different operating modes determine the combination of RS-232 drivers and RS-232 receivers that are enabled at any one time. Separate transmitter enable inputs control two sets of three transmitters and separate receiver enable inputs control two sets of five receivers. Thus, an unused serial port (3 drivers and 5 receivers) can be shutdown to save power while the other serial port continues to transmit and receive data. The receivers remain active during shutdown at data rates up to 20kbits/sec. Supply current falls to 25µA when all drivers and receivers are disabled.

A Complete PC Serial Port On One Chip!

MAX241 has 4 RS-232 Drivers and 5 RS-232 Receivers



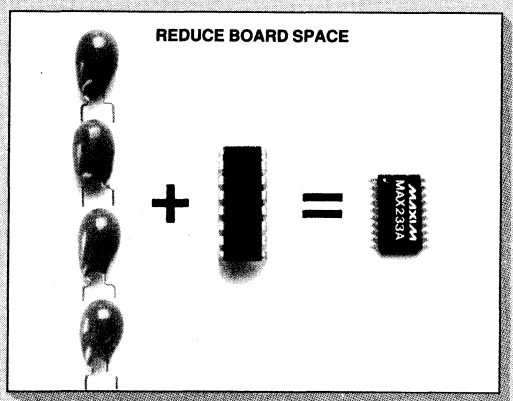
The MAX241 connects to a complete serial port.

The MAX241 is a single PC serial RS-232 interface port on one chip that reduces board space in personal computers. The MAX241 has 4 RS-232 drivers and 5 RS-232 receivers on one 28-pin small-outline chip to provide a complete RS-232 DTE (Data Terminal Equipment) port plus a spare RS-232 driver. Therefore, all RS-232 data transmission and handshaking is taken care of on one chip. Plus, the MAX241 operates at data rates in excess of 20kbit/sec while meeting all EIA-232D specifications.

The MAX241 includes a shutdown and receiver enable mode. Receiver outputs turn off, and transmitter outputs are disabled during shutdown mode. In this mode, supply current drops to 10µA extending battery life in laptop computer applications. The MAX241's enable control activates the receiver TTL/CMOS outputs when it is at a low level, or places the outputs into a high impedance state. The RS-232 transmitters are unaffected by the receiver enable status.

+5V Powered Dual RS-232 Transceiver With No External Components!

New MAX233A Guarantees 116kbits/sec Data Rate



The MAX233A in a small outline package saves space and eliminates 4 charge pump capacitors.

Maxim's new MAX233A is a dual RS-232 transceiver that operates on a single +5V supply. The transceiver saves board space by integrating all the charge-pump capacitors required for a +5V-operation RS-232 transceiver within a 20-pin DIP package. A 20-pin small-outline package version will be available in July 1991 to save even more space.

The MAX233A meets EIA-232D and CCITT V.28 standards while operating at data rates as high as 116kbits/sec. The device typically operates to 200kbits/sec, extending the usable rate well beyond 20kbits/sec as guaranteed by the RS-232 standard.

The MAX233A consumes 10mA maximum quiescent current. When V_{CC} = 0V, the output drivers assume a high-impedance state that draws no current from the data lines.

Part Number	Power Supply (V)	# of RS232 Drivers	# of RS232 Receivers	# of Ext. Caps	Nom. Cap. (µF)	Shutdown & 3-State	Supply I(mA) max	(kb/sec) max	Features	Price 1000-up† ($)
MAX220	+5	2	2	4	10	NO	2	20	Ultra low power, industry standard pinout	2.65
MAX222	+5	2	2	4	0.1	YES	10	116	MAX232A with shutdown	2.65
MAX230	+5	5	0	4	4.7	YES	10	20	5 drivers with shutdown	3.44
MAX231	+5 and +7.5 to +13.2	2	2	2	4.7	NO	1/5	20	Standard +5/+12V or battery supplies; same functions as MAX232	2.04
MAX232	+5	2	2	4	4.7	NO	10	20	Industry standard	1.91
MAX232A	+5	2	2	4	0.1	NO	10	116	Higher slew rate, small caps	2.65
MAX233	+5	2	2	0	-	NO	10	20	No external caps	3.56
MAX233A	+5	2	2	0	4.7	NO	10	116	No external caps, high slew rate	4.21
MAX234	+5	4	0	4	4.7	NO	10	20	Replaces 1488	3.10
MAX235	+5	5	5	0	-	YES	10	20	No external caps	7.20
MAX236	+5	4	3	4	4.7	YES	10	20	Shutdown, three-state	4.18
MAX237	+5	5	3	4	4.7	NO	10	20	Complements IBM PC serial port	4.18
MAX238	+5	4	4	4	4.7	NO	10	20	Replaces 1488 and 1489	4.18
MAX239	+5 and +7.5 to +13.2	3	5	2	4.7	NO	1/15	20	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port	4.18
MAX240	+5	5	5	4	4.7	YES	10	20	DIP or flatpak package	5.10
MAX241	+5	4	5	4	4.7	YES	10	20	Complete IBM PC serial port	4.73
MAX242	+5	2	2	4	0.1	YES	10	116	Separate shutdown and enable	2.65
MAX243	+5	2	2	4	0.1	NO	10	116	Open line detection simplifies cabling	2.65
MAX244	+5	8	10	4	1.0	NO	25	20	High slew rate	††
MAX245	+5	8	10	0	-	YES	25	20	High slew rate, int. caps, two shutdown modes	††
MAX246	+5	8	10	0	-	YES	25	20	High slew rate, int. caps, three shutdown modes	††
MAX247	+5	8	9	0	-	YES	25	20	High slew rate, int. caps, nine operating modes	††
MAX248	+5	8	8	4	1.0	YES	25	20	High slew rate, selective half-chip enables	††
MAX249	+5	6	10	4	1.0	YES	25	20	MAX248 with 2 complete IBM PC serial ports	††
RS232 ISOLATION PRODUCTS										
MAX250	+5	2	2		-	YES	-	20	Isolated RS232 chipset	3.20
MAX251	+5	2	2		-	YES	-	20	Isolated RS232 chipset	3.20
MAX252A	+5	2	2	0	-	YES	90	9.6	UL Recognized, 1500V isolation	50.00
MAX252B	+5	2	2	0	-	YES	90	9.6	Economical 500V isolation	29.50

Note:
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products-contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

What The EIA-232D Specs Don't Tell You

What Is The Maximum Cable Length?

When the RS-232C standard was rewritten as EIA-232D, the specification pertaining to maximum cable length was changed from "50 feet" to "2500 picofarads." This change from feet of cable to picofarads of load capacitance recognizes a shortcoming in RS-232C: not only does the older spec ignore the effects of cable capacitance; it contains a 50ft distance limit often ignored by designers.

The new EIA-232D specification considers cable length indirectly, through the effect of load capacitance, but it doesn't specify a maximum length. Because the capacitance of inexpensive cable can range from 12pF/ft for a single twisted pair to 30pF/ft for low-noise, shielded, multiple-twisted-pair cable, some confusion still prevails.

Cable capacitance matters because EIA-232D transmissions are AC signals. First, higher capacitance demands higher peak currents from the transmitter, resulting in higher average supply current for a given data rate (Figure 1). Second, the cable impedance forms an AC divider with the transmitter's output impedance. Higher cable capacitance lowers the divider's shunt component, which in turn reduces signal amplitude at the receiver end of the cable (Figure 2). This signal loss becomes a problem when the receiver-end voltage falls below the specified 5V minimum input level.

Third, cable capacitance limits the slew rate available from a given transmitter (Figure 3), and slew rate determines the transition time between the +3V and -3V signal levels. Transition time then constrains the maximum data rate according to specifications in the RS-232C, EIA-232D and CCITT V.28 standards (Table 1). Every EIA-232D transmitter from Maxim is therefore tested with the maximum 2500pF specified load capacitance, to ensure compliance with the maximum data rate specified for that device.

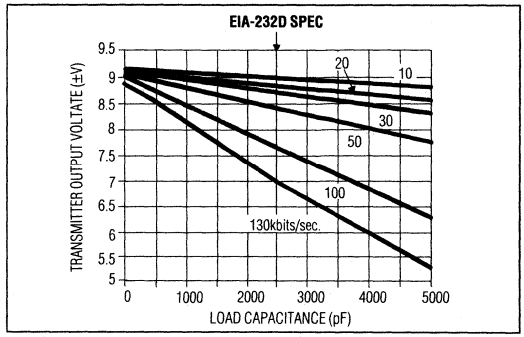


Figure 2. MAX220 Output Voltage vs. Output Load Capacitance, 2 Transmitters Driven

The simplest way to calculate the maximum allowable cable length for a Maxim EIA-232D transceiver is to divide its 2500pF load specification by the capacitance per foot specified for your EIA-232D cable. Then, for cable lengths up to that limit, you can be assured that the transceiver will operate properly and provide its maximum specified data rate.

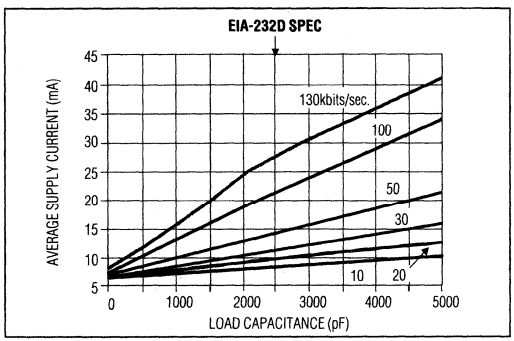


Figure 1. MAX220 Supply Current vs. Output Load Capacitance, 2 Transmitters Driven

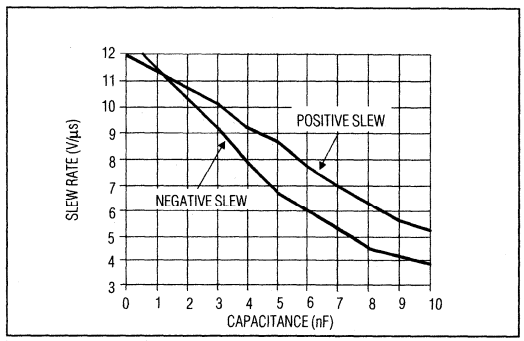


Figure 3. Slew Rate vs. Output Capacitance (MAX220/232A/233A/242/243)

What The EIA-232D Specs Don't Tell You

Figure 4 shows how the data rate may be extended past the limits of RS-232. Longer cable adds to line capacitance, lengthening the signal transition time (tT) and thereby limiting the data rate. But you can implement cable lengths and data rates well beyond the limits implied by the EIA-232D specification.

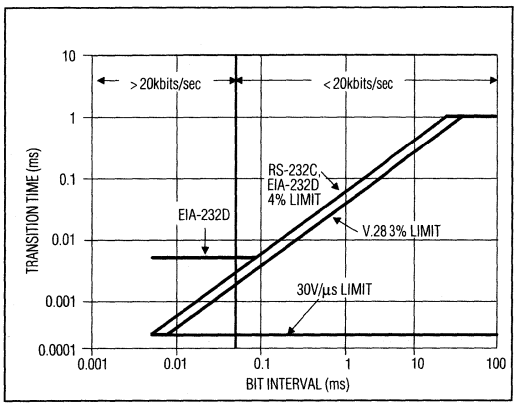


Figure 4. Maximum Transition Time vs. Bit Interval

Why Use Low-Power EIA-232D Components?

Many types of portable equipment communicate over EIA-232D lines, from bar-code readers to underwater data loggers. Minimal power consumption is a common goal in these designs, particularly in portable equipment that must sustain a long battery life. Low power consumption in EIA-232D transceivers is important because dissipation in these circuits becomes a growing percentage of the total as you reduce the operating current in a CMOS system.

When Should You Activate The Shutdown Mode?

First, how often is the EIA-232D link active? If the answer is "continuously" then it's best to choose a transceiver with the lowest possible quiescent current. The MAX220, with low 0.5mA quiescent current is ideal for low-power applications. Supply current for a given device varies with the capacitive load (Figure 1) and the data rate. Low current remains important if the operation is intermittent, but in that case you should also shut the chip down when it's not in use. The MAX222 and MAX242, for instance, draw only 1µA in the shutdown mode.

Shutdown helps the system conserve power (Figure 5). Although the MAX222 and MAX242 draw the same current as the MAX232A/233A/243 (13.4mA for the conditions listed) for continuous operation, they consume less average power if shut down for any duty cycle at all. The lower-power MAX220, which cannot be shut down, has an advantage over the MAX222 and MAX242 only when it transmits data more than two-thirds of the time. (This comparison is restricted to data rates below the MAX220's limit of 40 kbits/sec.) The optimum choice for power consumption thus depends on the application and on the ratio of transmitting time to shutdown time.

What EIA-232D Applications Require Line Isolation?

In telecomm systems, the service provider incorporates line isolation to protect the network against unorthodox connnections made by users. Similarly, the EIA-232D connections from patient-monitoring equipment to data loggers and supervisory computers must be isolated to protect the patient from failures in the hardware.

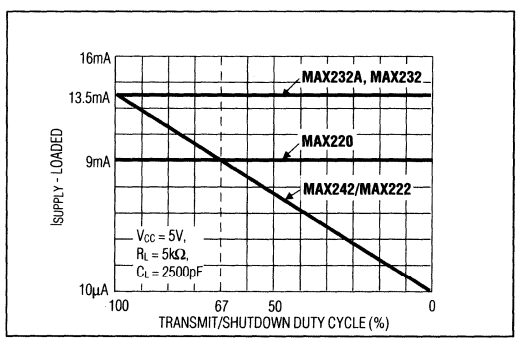


Figure 5. To conserve power, use the MAX220 when transmitting data more than 2/3 of the time. Use the MAX222/MAX242 with shutdown when transmitting less than 2/3 of the time.

What The EIA-232D Specs Don't Tell You

Isolation not only provides safety, it can also improve a system's electrical performance. EIA-232D links between a computer in one building and terminals in other buildings, for example, can exhibit ground-current noise if the buildings' earth-ground connections have different potentials (and they often do). Isolation with a rating of only 100V can solve this problem. In severe industrial environments, however, you may need a full UL-rated isolation barrier of 1500V or more.

The task of transmitting digital data while maintaining an electrical barrier is usually performed by transformers and opto-isolators. The transformer supplies power to the other side of the barrier while the opto-couplers handle data transmission across the barrier. As an alternative, the transmission technique can involve small capacitors, acoustic devices, or even radio communications. An alternative to transformers for power transmission is the use of independent power supplies on either side of the barrier.

It may appear straightforward to implement line isolation by combining standard EIA-232D transmitter and receiver chips with standard opto-isolators, but this approach has two drawbacks: Because the LEDs in opto-isolators (especially high-speed ones) require more current than normal logic circuits can provide, you must connect the outputs in parallel or add buffer ICs to get adequate drive current. Second, the isolated power supply will be fairly large because standard EIA-232D chips require supply voltages of ±12V as well as +5V.

These power and signal-transfer problems are overcome by the MAX250/MAX251 chip set. The two ICs include circuitry for two EIA-232D transmitters and two receivers, circuitry for generating isolated power-supply voltages from the main (non-isolated) +5V supply, and interface circuitry for driving and receiving signals from the external opto-isolators. You need supply only the isolators, a 1:1 transformer and a few passive components to complete an isolated dual-transceiver EIA-232D port (Figure 6a).

You can achieve any reasonable isolation voltage by a careful choice of the isolation components (opto-isolators and transformer). Inexpensive 4N26 optos, for example, when operated in the diode-to-diode mode (with base tied to emitter), can support transmission rates to 19.2kbits/sec. Higher speed opto-couplers such as the 6N136 are good for data rates to 90kbits/sec. You can either wind the transformer according to specifications taken from the MAX250/251 data sheet, or obtain it ready-made from the manufacturer, also listed in the data sheet.

The MAX252 (Figure 6b), packs all the circuitry of Figure 6a in a module with the size and appearance of a standard 40-pin DIP for ICs. The UL-recognized device includes two ICs, a transformer, four capacitors, four opto- isolators, and a 1500V isolation barrier.

What improvements Have Been Made in RS-232 Data Transmission?

Numerous changes in the RS-232 standard (now called EIA-232D) have been prompted by the experience of users. This process continues, and IC manufacturers are responding as the component requirements change. Here are some of the recent developments:

Operation On a Single +5V Supply

On-chip DC-DC converters generate 10V for the transmitter output drivers. This feature eliminates the need for 12V supplies, often included in a system solely for the EIA-232D circuits.

Transmitters and Receivers On One Chip

Combining transmitters and receivers on one chip provides a significant space savings over the separate IC approach, especially in surface-mount applications.

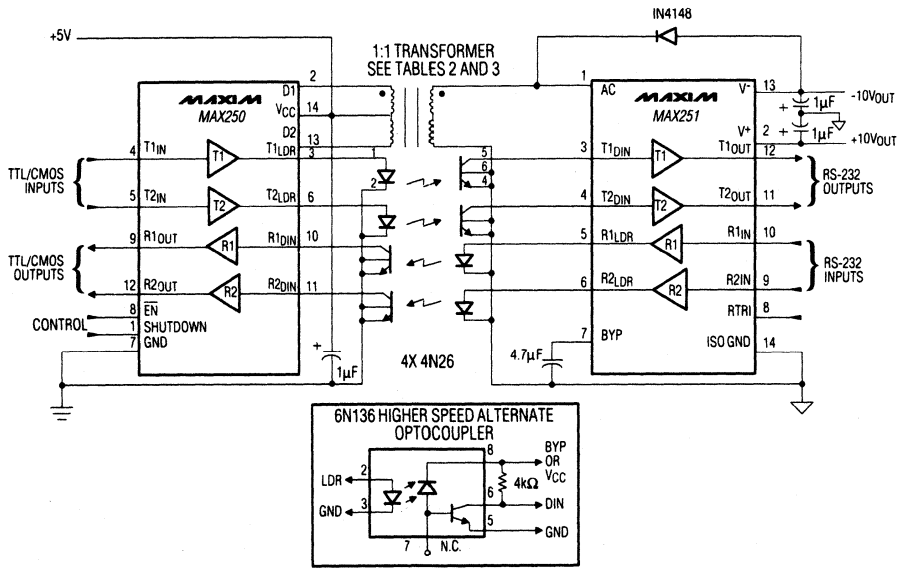
Higher Data Rates

Maxim ICs (MAX222/232A/233A/242/243) guarantee an RS-232 data rate of 116kbits/sec. compared with the EIA limit of 20kbits/sec. (Though most popular, EIA-232D is the slowest of the current standards for serial-data transmission, as shown in Table 2).

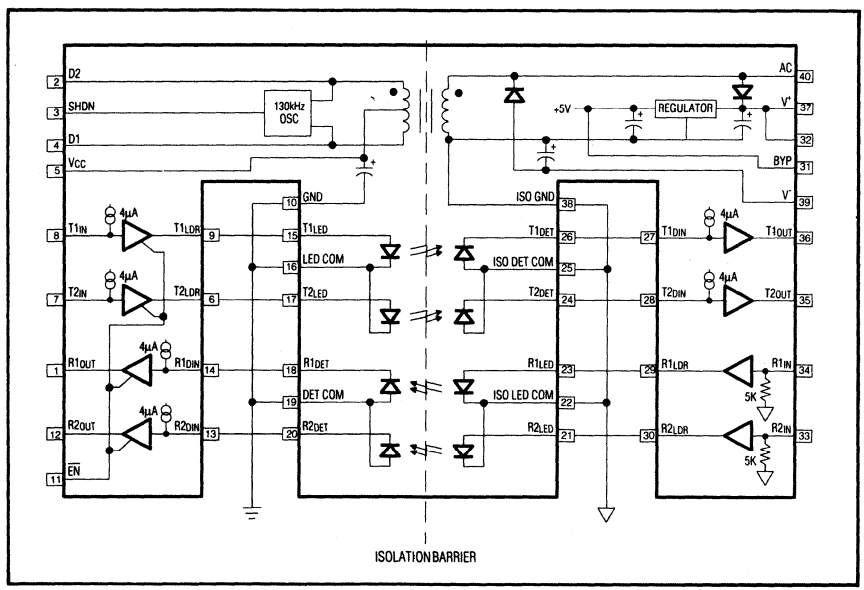
Other New Features for EIA-232D Devices

Chip Enable controls the receiver outputs, and Shutdown reduces the supply current to 1µA in the MAX222/242. By placing the transmitter outputs in a high-impedance state, Shutdown allows the chip to share lines with other RS-232 transmitters. The MAX222 perform Shutdown and Chip Enable with one pin; The MAX242 offers separate pins for Chip Enable and Shutdown.

What The EIA-232D Specs Don't Tell You



6a



6b

MAX252 BLOCK DIAGRAM

Figure 6. Isolated EIA-232D Interface

What The EIA-232D Specs Don't Tell You

TABLE 1. COMPARISON OF TRANSITION TIMES

	RS-232C	EIA-232D	CCITT V.28
Slew Rate, Maximum	30 V/µs	30 V/µs	30 V/µs
Transition Time, t_T, Maximum			
<40 bits/sec.	1ms	1ms	—
<30bits/sec. (V.28 only)	—	—	1ms
40bits/sec. < t_T < 8kbits/sec.	4% of a unit interval	4% of a unit interval	3% of a unit interval
> 8kbits/sec.	4% of a unit inverval	5µs	3% of a unit interval

TABLE 2. COMPARISON OF STANDARDS

	EIA-232D	EIA-423A	EIA-422A	RS-485
Mode of Operation	Single Ended	Single Ended	Differential	Differential
Allowed # of Tx and Rx per Data Line	1 Tx, 1 Rx	1 Tx, 1 Rx	1 Tx, 10 Rx	32 Tx, 32Rx
Cable Length, Maximum	Load-Dependent	4kft	4kft	4kft
Data Rate, Maximum	20kbits/sec.	100kbits/sec.	10Mbits/sec.	10Mbits/sec.
Driver Output Range, Loaded (0V Offset):				
Minimum	±5V	±3.6V	±2V	±1.5V
Maximum	±15V	±5.4V	±5V	±5V
Driver Short-Circuit Current, Maximum	500mA	150mA	150mA	250mA
TX Load Impedance	3kΩ to 7kΩ	450Ω	100Ω	54Ω
Instantaneous Slew Rate	< 30V/µs	—	—	—
Rx Input Sensitivity	±3V	±200mV	±200mV	±200mV
Rx Input Resistance, Minimum	3kΩ to 7kΩ	4kΩ	4kΩ	12kΩ
Rx Input Range	±25V	±12V	±7V	-7V to +12V

19-289, Rev.1; 7/91

APPLICATION NOTE FOLLOWS DATA SHEETS

MAXIM

High-Speed +5V-Powered RS-232 Drivers/Receivers

General Description

The MAX220/222/232A/233A/242/243 are ideal for EIA-232D and V.28/V.24 interfaces, particularly where ±12V supplies are not available. Each device contains two drivers and receivers and operates from a single +5V power supply. Driver slew rates and data rates are guaranteed up to 116kbits/sec (except MAX220), and most devices operate with only 0.1µF charge-pump capacitors.

MAX220: A low-power, pin-compatible upgrade of the MAX232, with a typical supply current of only 0.5mA.

MAX222: Includes a $\overline{\text{SHUTDOWN}}$ ($\overline{\text{SHDN}}$) input that disables the device and places all driver and receiver outputs into a high-impedance state. When shut down, supply current is only 10µA.

MAX232A/MAX233A: Pin-compatible upgrades of the MAX232/MAX233. Driver outputs maintain high impedance with power off.

MAX243: Identical to the MAX232A, except the MAX243 has a negative input threshold on one receiver that eliminates the jumpers on CTS and RTS; jumpers are normally required when switching from two-line to four-line interfaces.

MAX242: Identical to the MAX222 with the addition of separate three-state controls for driver and receiver outputs, allowing bused configurations. When drivers are disabled, supply current falls to 10µA.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

- ♦ **116kbits/sec Guaranteed Data Rate (except MAX220)**
- ♦ **Three-State Outputs (MAX222/MAX242)**
- ♦ **0.5mA Typ Supply Current (MAX220)**
- ♦ **High-Impedance Outputs with Power Off**
- ♦ **10µA Max Shutdown Current (MAX222/MAX242)**
- ♦ **Exceed All EIA-232D and V.28 Specifications**
- ♦ **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic Dip
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic Dip
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP
MAX222CPN	0°C to +70°C	18 Plastic Dip
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic Dip
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP

Ordering information continued on page 11

** Contact factory for dice specifications.*

Selection Table

Part Number	Max kbits/sec	External Capacitors (µF)	Max Supply Current (mA)	Shutdown & Three-State	Features
MAX220	20	4.7/10	2	No	Lowest Power
MAX222	116	0.1	10	Yes	$\overline{\text{SHDN}}$
MAX232A	116	0.1	10	No	High Speed
MAX233A	116	None	10	No	Internal Caps
MAX242	116	0.1	10	Yes	$\overline{\text{EN}}$, $\overline{\text{SHDN}}$
MAX243	116	0.1	10	No	Open-Line Detect

High-Speed +5V-Powered RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} -0.3V)
R_{IN} ..... ±30V
T_{OUT} (Note 1) ..... ±15V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} +0.3V)
Driver/Receiver Output Short Circuited to GND ... Continuous
Continuous Total Power Dissipation (T_A = +70°C)
16-Pin Plastic Dip (derate 7.41mW/°C above +70°C) .. 407mW
18-Pin Plastic Dip (derate 8.00mW/°C above +70°C) .. 440mW
20-Pin Plastic Dip (derate 8.00mW/°C above +70°C) ... 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) .. 478mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 525mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 525mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 550mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 579mW
Operating Temperature Ranges:
MAX2 _ _ AC _ _ , MAX2 _ _ C _ _ ..... 0°C to +70°C
MAX2 _ _ AE _ _ , MAX2 _ _ E _ _ ..... -40°C to +85°C
MAX2 _ _ AM _ _ , MAX2 _ _ M _ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	$\overline{SHDN}$ = V_{CC}			5	40	µA
	$\overline{SHDN}$ = 0V			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	Except MAX220, normal operation			200	116	kbits/sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	Except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	Except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	Except MAX243, V_{CC} = 5V, no hyst. in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} -0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA
$\overline{EN}$ Input Threshold Low				1.4	0.8	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

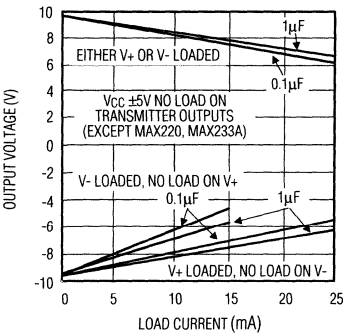
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Threshold High			2.0	1.4		V
POWER SUPPLY						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5-10	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both outputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current					±1	µA
$\overline{SHDN}$ Threshold Low				1.4	0.8	V
$\overline{SHDN}$ Threshold High			2.0	1.4		V
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	Except MAX220	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX222/242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX222/242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (Includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT}-t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR}-t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.
Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when the $R2_{IN}$ is ≥ 0V or is floating.

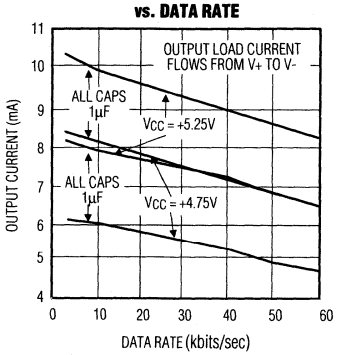
High-Speed +5V-Powered RS-232 Drivers/Receivers

Typical Operating Characteristics

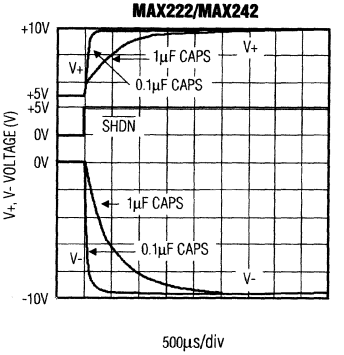
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



ON-TIME EXITING SHUTDOWN – MAX222/MAX242



Detailed Description

The MAX220-MAX243 contain three sections: dual charge-pump DC-DC voltage converter, RS-232 drivers, and RS-232 receivers.

Dual Charge-Pump Voltage Converter

All devices convert +5V to ±10V with two stages of charge-pump voltage conversion. In the first stage, pump capacitor C1 doubles VCC to +10V, which is stored on the V+ filter capacitor, C3. In the second stage, pump capacitor C2 inverts +10V to -10V, which is stored on the V- filter capacitor, C4. The equivalent circuit of the dual charge pump is shown in Figure 12.

A small amount of power can be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry. The amount that can be drawn is shown in the *Output Voltage vs. Load Current* and *Available Output Current vs. Data Rate* graphs in the *Typical Operating Characterisitics* Section. The second graph shows that the available current varies inversely with data rate. If more than ±10V power is required, the MAX680 charge-pump voltage converter or the MAX743 DC-DC converter are recommended.

When using the shutdown feature of the MAX222 and MAX242, avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to VCC. This is because V+ is internally connected to VCC in shutdown mode.

When power is drawn from the V+ or V- pins, except for the MAX220, the value of C1-C4 should be increased to at least 1µF, but not more than 10µF. The time required to return to active operation after shutdown is proportional to the charge-pump capacitor value.

RS-232 Drivers

With +5V VCC, the typical driver-output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet the EIA-232D/V.28 specification which calls for ±5V minimum output levels under worst-case conditions. These include a minimum 3kΩ load ,VCC = 4.5V, and maximum operating temperature. The open-circuit output voltage swing ranges from V+ - 1.3V to V- + 0.5V.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to VCC are included on chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. In the MAX222 and MAX242, the pull-ups are disabled in shutdown to minimize current drain. When shut down, driver outputs are turned off.

As required by the EIA-232D and V.28 specifications, driver-output slew rate is limited to 30V/µs. Typical slew rates are 24V/µs unloaded and 12V/µs loaded with 3kΩ and 2500pF. These slew rates allow bit rates of over 116kbits/sec.

RS-232 Receivers

The RS-232 receiver-input signal range of ±5V to ±15V is translated to 5V TTL/CMOS output logic levels. Since the EIA-232D/V.28 specifications define a voltage level greater than +3V as a logic 0, the receivers invert. And since the input thresholds are set at 0.8V and 2.4V (except MAX243 $R2_{IN}$), receivers respond to EIA-232D/V.28 as well as TTL level inputs.

Receivers' inputs are protected against input overvoltage up to ±30V and provide input terminating resistors with 5kΩ nominal values. The receivers implement type 1 interpretation of fault conditions (~7 of V.28, ~2.5 of EIA-232D).

RS-232 receivers' inputs hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions, even with slow-moving input signals with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Shutdown - MAX222/MAX242

On the MAX222, all receivers are disabled during shutdown. On the MAX242, both receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX242 also has a receiver output enable input ($\overline{EN}$) that allows receiver output control independent of $\overline{SHDN}$. With the MAX222, $\overline{SHDN}$ also disables the receiver outputs.

MAX243-Negative Threshold

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the MAX232 family implement the optional cable fault protection as specified by EIA-232D specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Applications Information

Figures 5 through 11 show typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device. RS-232 receivers and drivers invert on all devices.

Driver outputs ($T1_{OUT}$, $T2_{OUT}$) on all devices enter a high-impedance state when V_{CC} powers down. Also, when the $\overline{SHDN}$ input of the MAX222 or MAX242 is low, the devices turn off and the driver outputs again go into a high-impedance state. In the MAX222, $\overline{SHDN}$ also disables receiver logic outputs ($R1_{OUT}$, $R2_{OUT}$); however, when the MAX242 is shut down, its receivers continue to function in a reduced power mode.

MAX242 receiver outputs are placed in a high-impedance state by the $\overline{EN}$ input independent of $\overline{SHDN}$. $\overline{EN}$ enables the receiver TTL/CMOS outputs ($R1_{OUT}$, $R2_{OUT}$) when low and places the outputs into a high-impedance state when high.

When active (no shutdown), the MAX242 receiver propagation delay is approximately 600ns. When shut down, the delay increases to approximately 2.5µs for a high-to-low input transition. To minimize power consumption, the internal driver pull-up resistors disconnect from V_{CC} in the shutdown mode.

High-Speed +5V-Powered RS-232 Drivers/Receivers

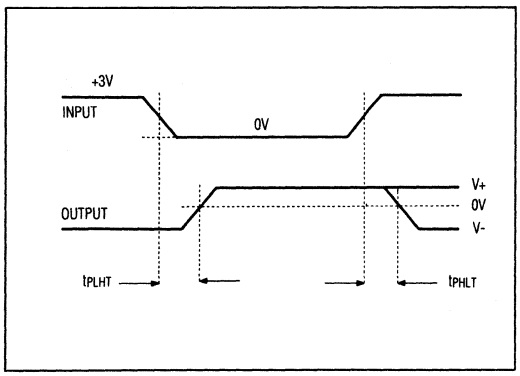


Figure 1. Transmitter Propagation Delay Timing

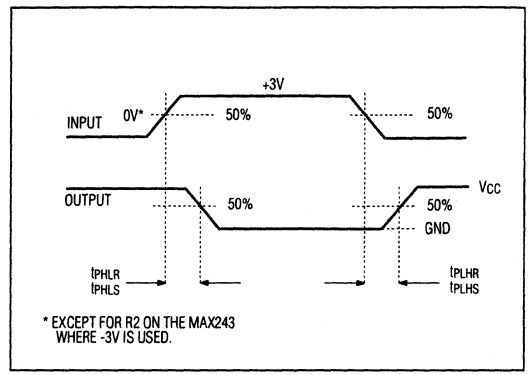


Figure 2. Receiver Propagation Delay Timing

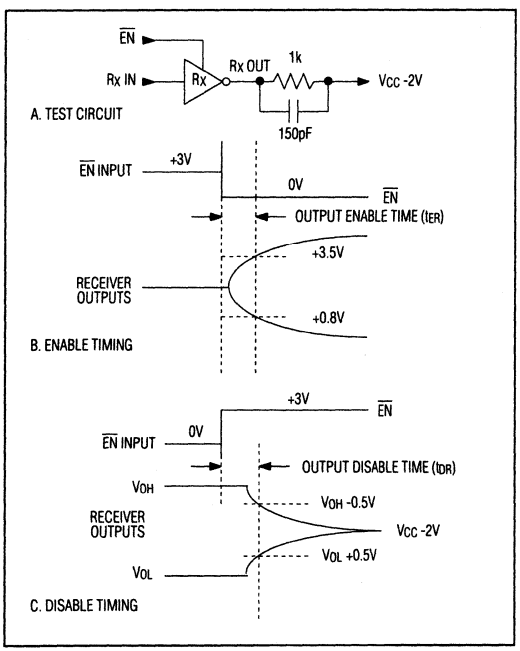


Figure 3. Receiver-Output Enable and Disable Timing

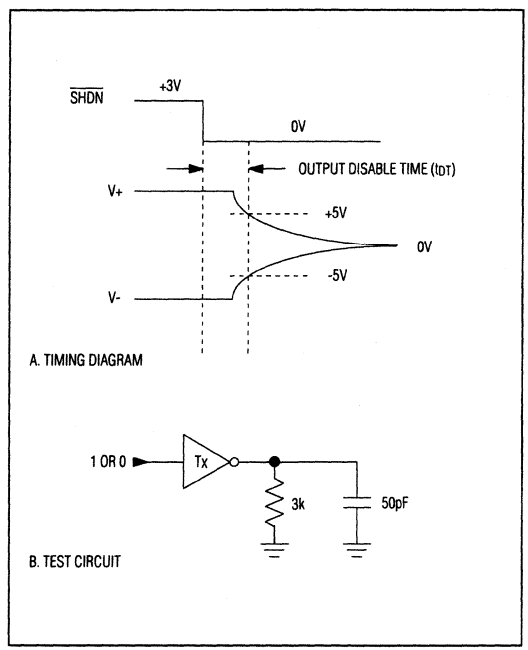


Figure 4. Transmitter-Output Disable Timing

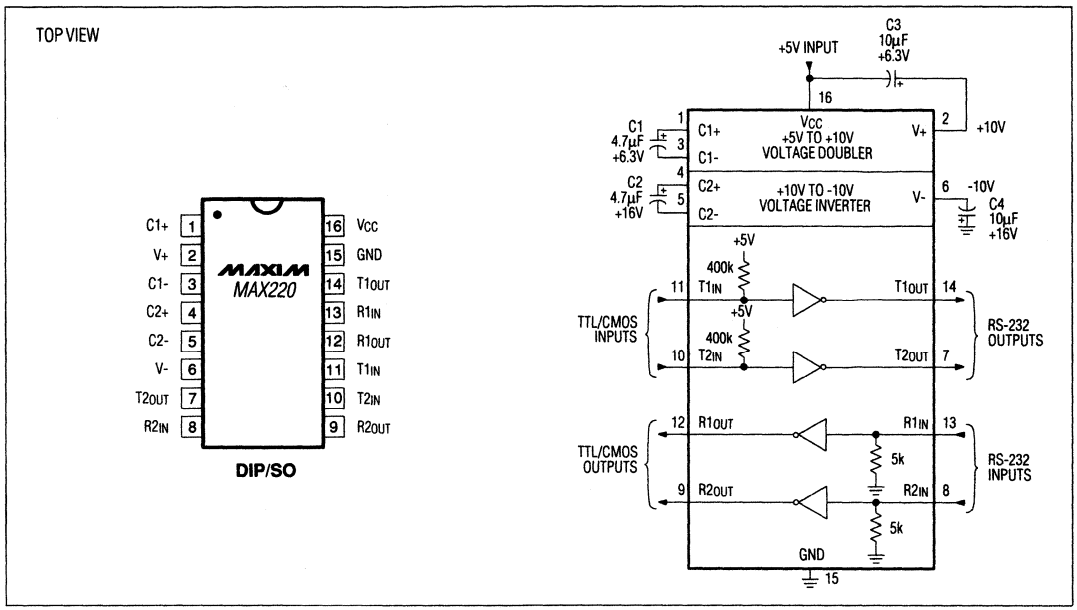


Figure 5. MAX220 Typical Operating Circuit

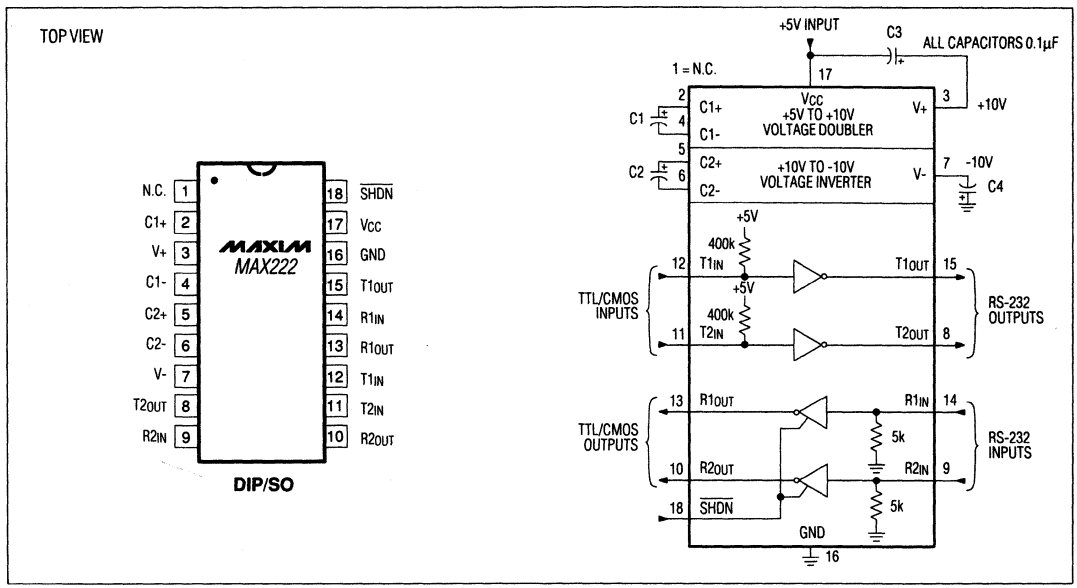


Figure 6. MAX222 Typical Operating Circuit

High-Speed +5V-Powered RS-232 Drivers/Receivers

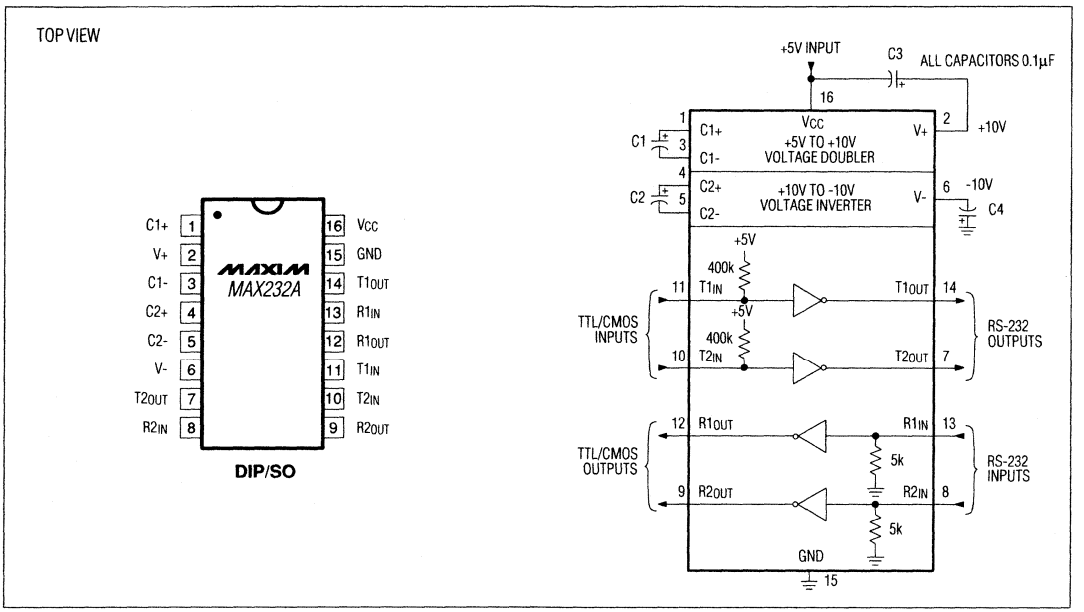


Figure 7. MAX232A Typical Operating Circuit

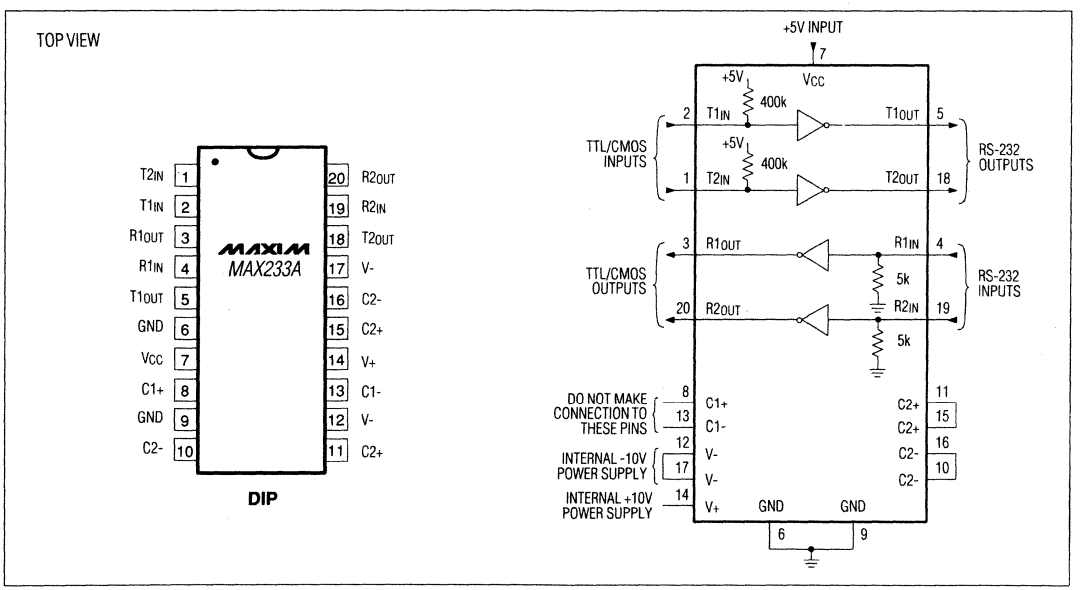


Figure 8. MAX233A Typical Operating Circuit (DIP Package Only)

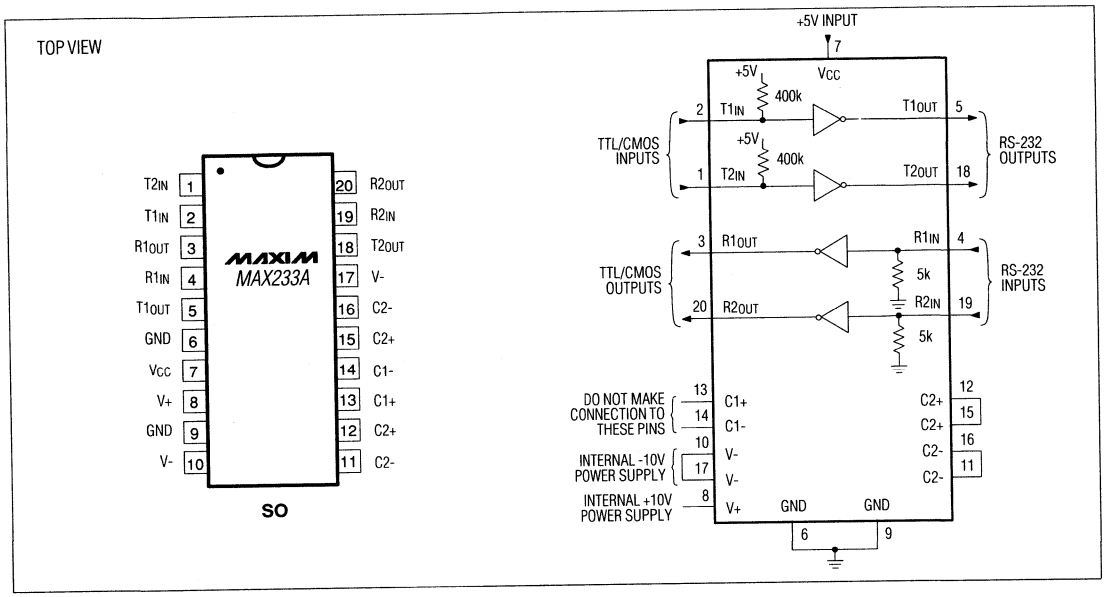


Figure 9. MAX233A Typical Operating Circuit (SOIC Package Only)

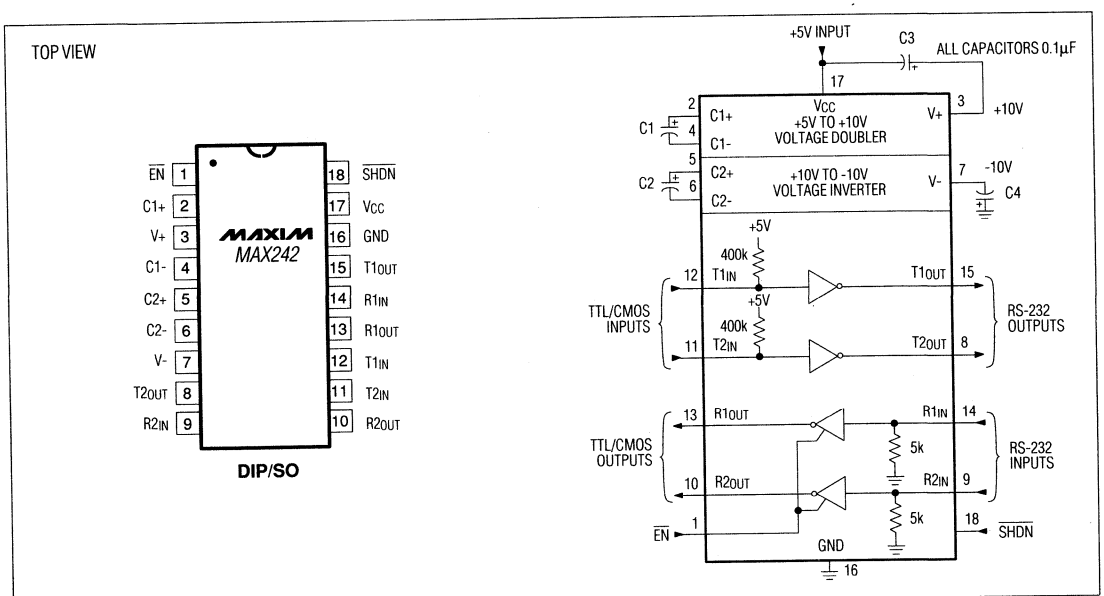
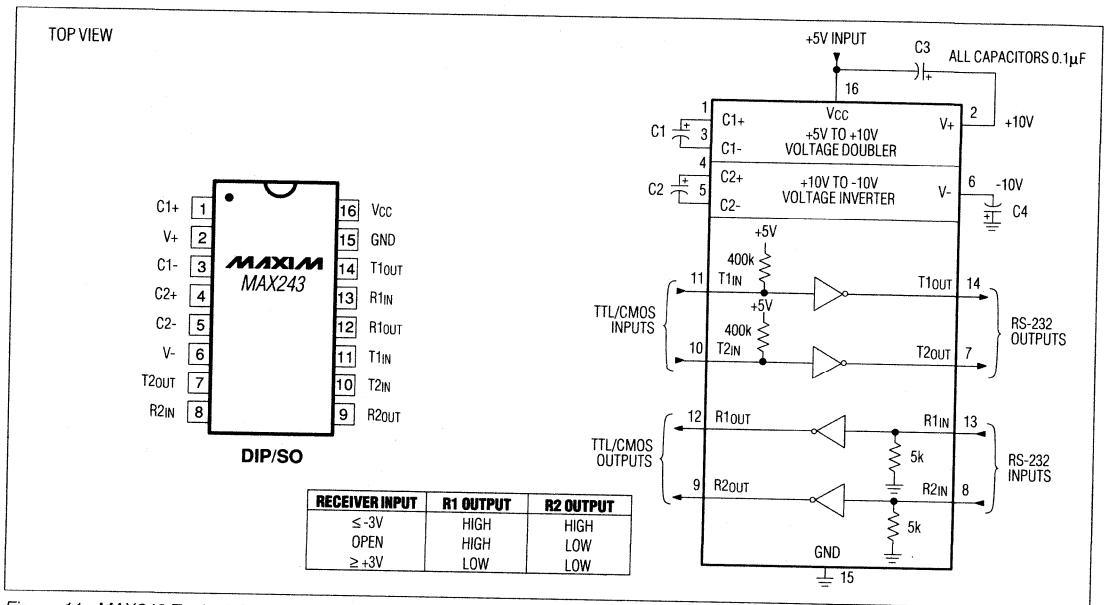


Figure 10. MAX242 Typical Operating Circuit

High-Speed +5V-Powered RS-232 Drivers/Receivers



RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

Figure 11. MAX243 Typical Operating Circuit

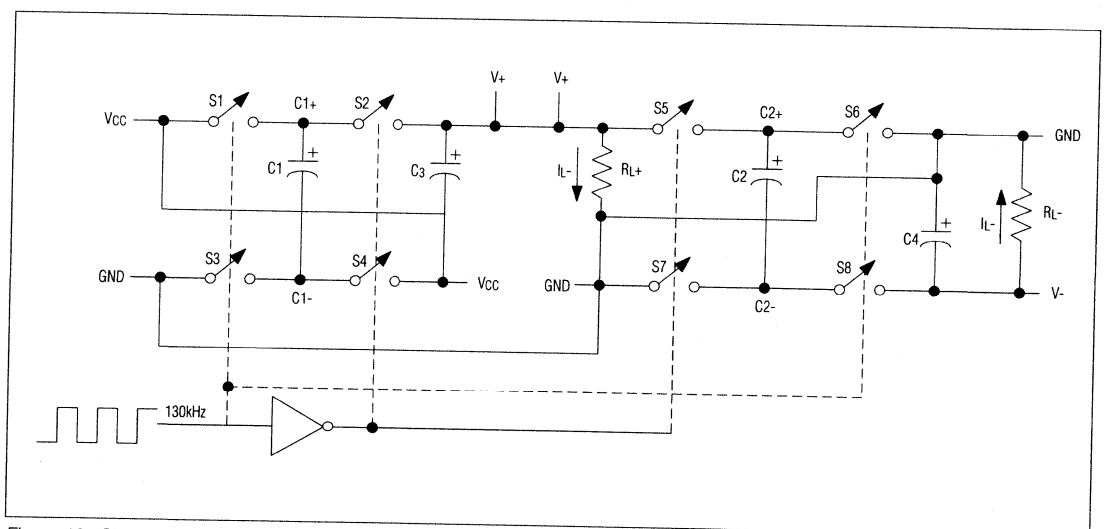


Figure 12. Charge Pump

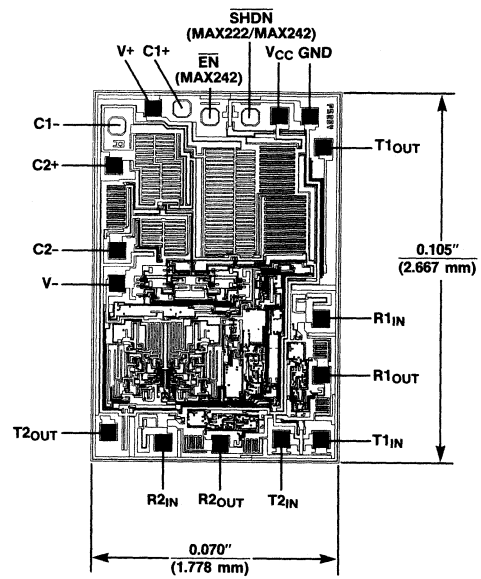
High-Speed +5V-Powered RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX232ACPE	0°C to +70°C	16 Plastic Dip
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic Dip
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AEJE	-40°C to +85°C	16 CERDIP
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX233ACPP	0°C to +70°C	20 Plastic Dip
MAX233AEPP	-40°C to +85°C	20 Plastic Dip
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX242CPN	0°C to +70°C	18 Plastic Dip
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic Dip
MAX242EWN	-40°C to +85°C	18 Wide SO
MAX242EJN	-40°C to +85°C	18 CERDIP
MAX242MJN	-55°C to +125°C	18 CERDIP
MAX243CPE	0°C to +70°C	16 Plastic Dip
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX243C/D	0°C to +70°C	Dice*
MAX243EPE	-40°C to +85°C	16 Plastic Dip
MAX243ESE	-40°C to +85°C	16 Narrow SO
MAX243EJE	-40°C to +85°C	16 CERDIP
MAX243MJE	-55°C to +125°C	16 CERDIP

* *Contact factory for dice specifications.*

Chip Topography



MAXIM

+5V Powered RS-232 Drivers/Receivers

General Description

Maxim's family of line drivers/receivers are intended for all RS-232 and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available. The MAX230, MAX236, MAX240 and MAX241 are particularly useful in battery powered systems since their low power shutdown mode reduces power dissipation to less than 5μW. The MAX233 and MAX235 use no external components and are recommended for applications where printed circuit board space is critical.

All members of the family except the MAX231 and MAX239 need only a single +5V supply for operation. The RS-232 drivers/receivers have on-board charge pump voltage converters which convert the +5V input power to the ±10V needed to generate the RS-232 output levels. The MAX231 and MAX239, designed to operate from +5V and +12V, contain a +12V to -12V charge pump voltage converter.

Since nearly all RS-232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. The wide variety of RS-232 applications require differing numbers of drivers and receivers. Maxim offers a wide selection of RS-232 driver/receiver combinations in order to minimize the package count (see table below).

Both the receivers and the line drivers (transmitters) meet all EIA RS-232C and CCITT V.28 specifications.

Features

- **Operates from Single 5V Power Supply (+5V and +12V — MAX231 and MAX239)**
- **Meets All RS-232C and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **Onboard DC-DC Converters**
- **±9V Output Swing with +5V Supply**
- **Low Power Shutdown — <1μA (typ)**
- **3-State TTL/CMOS Receiver Outputs**
- **±30V Receiver Input Levels**

Applications

Computers
Peripherals
Modems
Printers
Instruments

Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Components	Low Power Shutdown /TTL 3-State	No. of Pins
MAX230	+5V	5	0	4 capacitors	Yes/No	20
MAX231	+5V and +7.5V to 13.2V	2	2	2 capacitors	No/No	14
MAX232	+5V	2	2	4 capacitors	No/No	16
MAX233	+5V	2	2	None	No/No	20
MAX234	+5V	4	0	4 capacitors	No/No	16
MAX235	+5V	5	5	None	Yes/Yes	24
MAX236	+5V	4	3	4 capacitors	Yes/Yes	24
MAX237	+5V	5	3	4 capacitors	No/No	24
MAX238	+5V	4	4	4 capacitors	No/No	24
MAX239	+5V and +7.5V to 13.2V	3	5	2 capacitors	No/Yes	24
MAX240	+5V	5	5	4 capacitors	Yes/Yes	44 (Flatpak)
MAX241	+5V	4	5	4 capacitors	Yes/Yes	28 (Small Outline)

*Patent Pending

+5V Powered RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V^+ ..... (V_{CC} - 0.3V) to +14V
V^- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3 to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V^+ + 0.3V) to (V^- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short Circuit Duration
T_{OUT} ..... continuous
Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline (SO) 375mW
(derate 7mW/°C above +70°C)
Lead Temperature (soldering 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

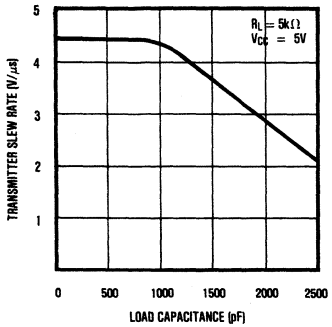
(MAX232, 234, 236, 237, 238, 240, 241 V_{CC} = 5V ±10%; MAX233, 235 V_{CC} = 5V ±5% C1-C4 = 1.0µF; MAX231, 239 V_{CC} = 5V ±10%, V^+ = 7.5V to 13.2V; T_A = Operating Temperature Range, Figures 3-14, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All Transmitter Outputs loaded with 3kΩ to Ground		±5	±9		V
V_{CC} Power Supply Current	No load, T_A = +25°C MAX232-MAX233			5	10	mA
	MAX230, MAX234-238, MAX240-MAX241			7	15	
	MAX231, MAX239			0.4	1	
V^+ Power Supply Current	No load, MAX231 and MAX239 only	MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	Figure 1, T_A = +25°C			1	10	µA
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, Shutdown				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	$\overline{EN}$, Shutdown		2.4			
Logic Pullup Current	T_{IN} = 0V			15	200	µA
RS-232 Input Voltage Operating Range			-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V, T_A = +25°C (MAX231, 239 V^+ = 0V)		0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V, T_A = +25°C (MAX231, 239 V^+ = 12V)			1.7	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233, I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = 1.0mA		3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, MAX241			400		ns
Output Disable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, MAX241			250		ns
Propagation Delay	RS-232 to TTL			0.5		µs
Instantaneous Slew Rate	C_L = 10pF, R_L = 3-7kΩ, T_A = +25°C (Note 1)				30	V/µs
Transition Region Slew Rate	R_L = 3kΩ, C_L = 2500pF, Measured from +3V to -3V or -3V to +3V			3		V/µs
Output Resistance	V_{CC} = V^+ = V^- = 0V, V_{OUT} = ±2V		300			Ω
RS-232 Output Short Circuit Current				±10		mA

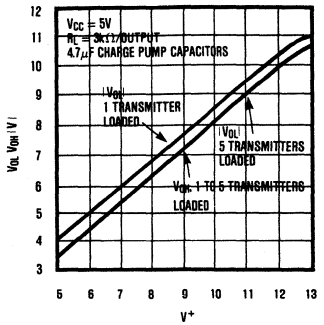
Note 1: Sample tested

Typical Operating Characteristics

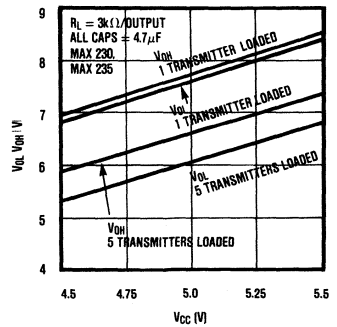
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



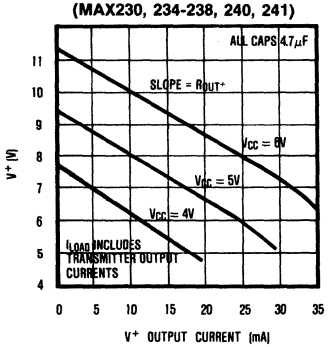
MAX239 TRANSMITTER OUTPUT VOLTAGE vs. V+ VOLTAGE



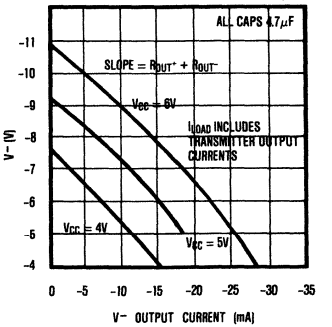
TRANSMITTER OUTPUT VOLTAGE vs. V_{CC} VOLTAGE



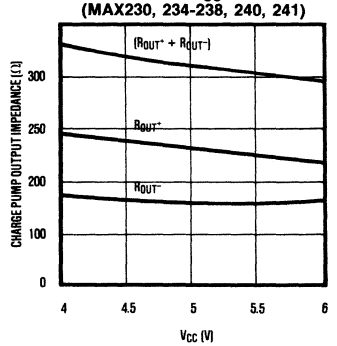
V+ SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



V- SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



CHARGE PUMP OUTPUT IMPEDANCE vs. V_{CC} (MAX230, 234-238, 240, 241)



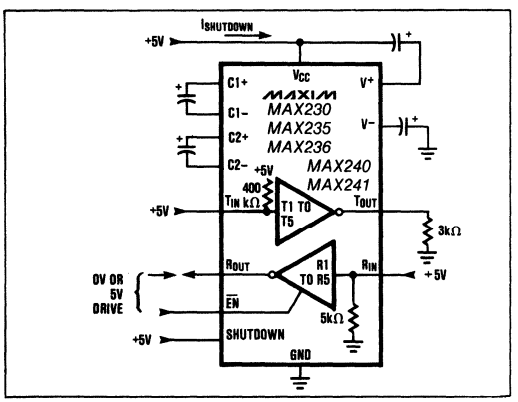


Figure 1. Shutdown Current Test Circuit

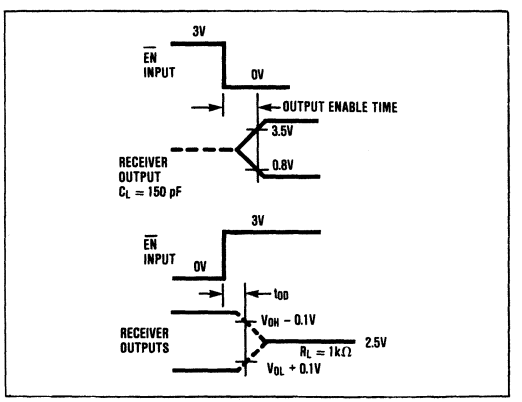
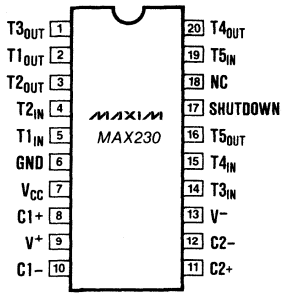


Figure 2. Receiver Output Enable and Disable Timing

+5V Powered RS-232 Drivers/Receivers



20 Lead Small Outline
also available.

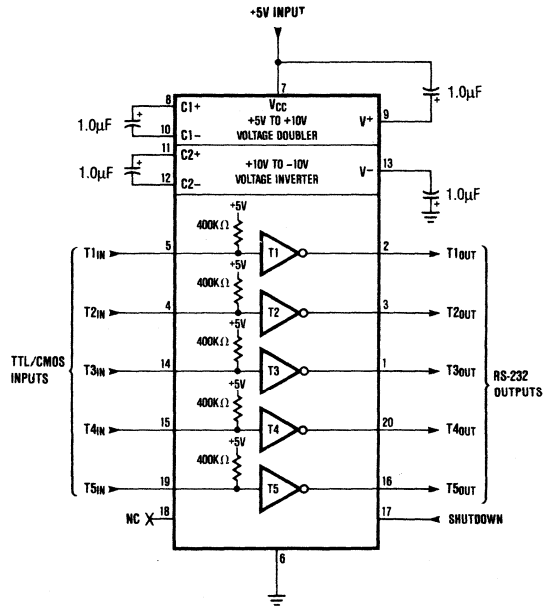
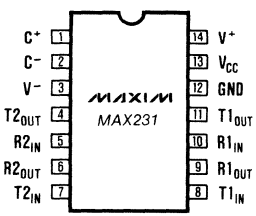
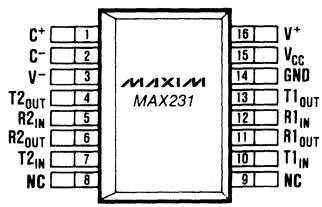


Figure 3. MAX230 Typical Operating Circuit



14 Lead Plastic DIP



16 Lead Small Outline

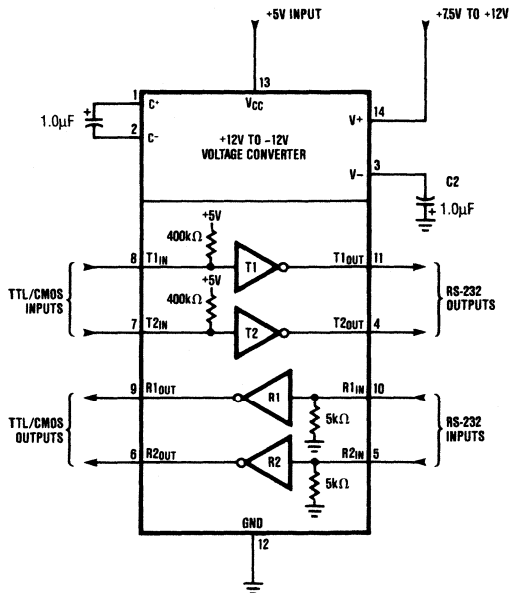
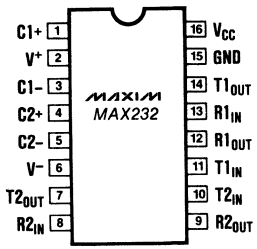


Figure 4. MAX231 Typical Operating Circuit



16 Lead Small Outline
also available.

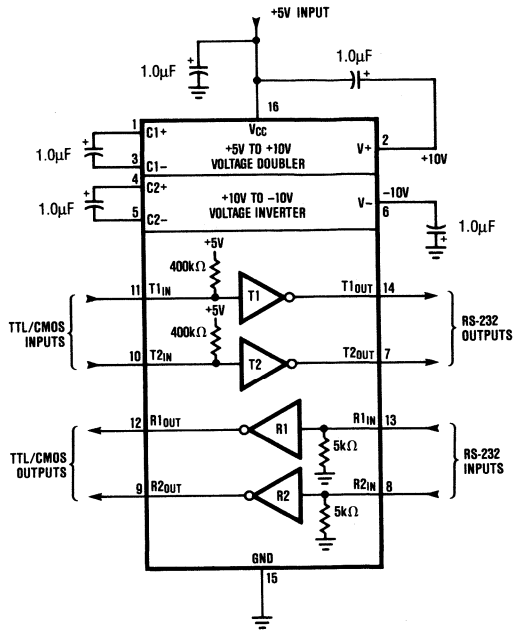
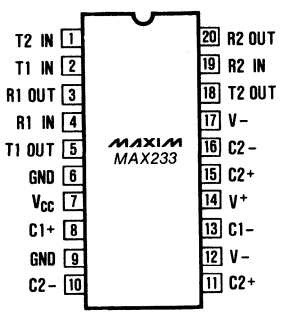


Figure 5. MAX232 Typical Operating Circuit



Small Outline Not Available

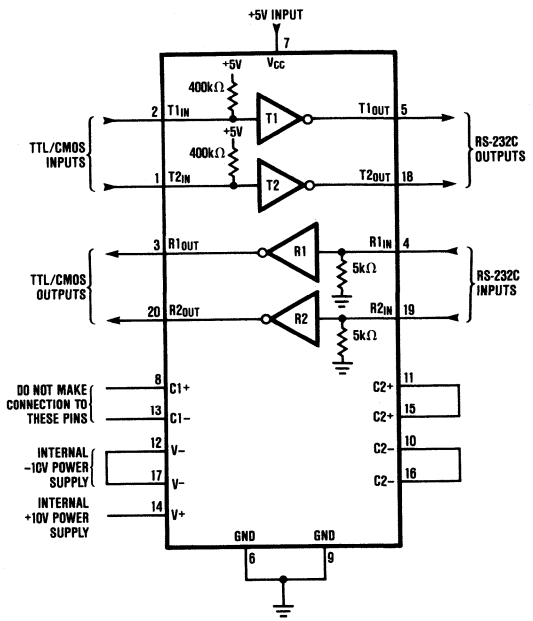
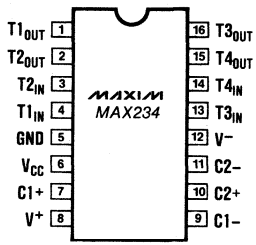


Figure 6. MAX233 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers



16 Lead Small Outline
also available.

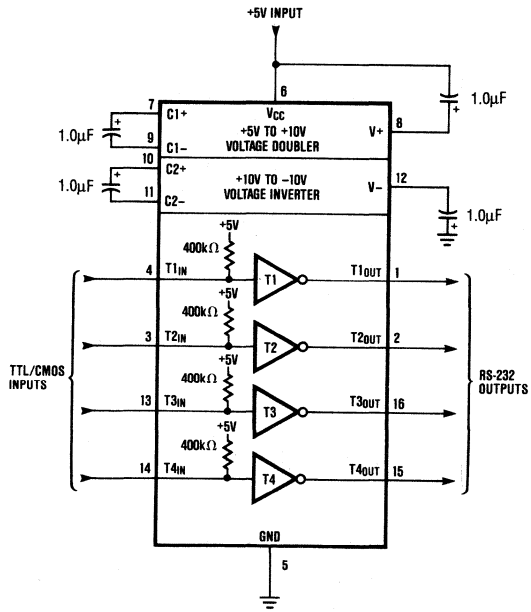
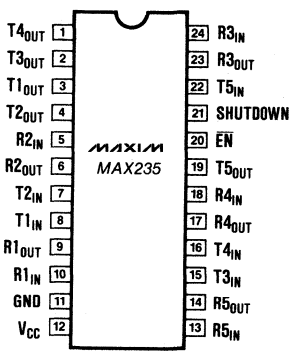


Figure 7. MAX234 Typical Operating Circuit



0.600" Wide Package Only

Small Outline Not Available

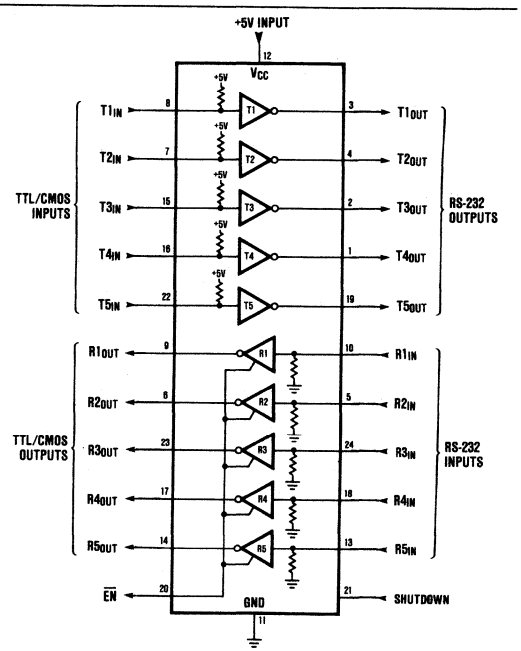
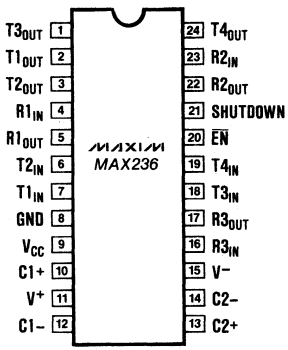


Figure 8. MAX235 Typical Operating Circuit



24 Lead Small Outline
also available.

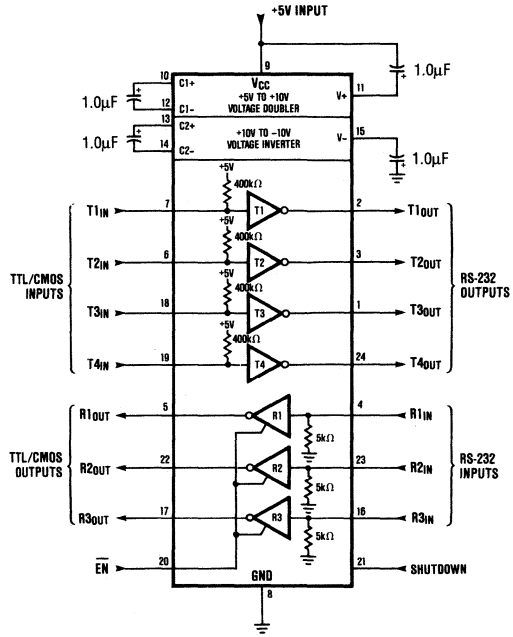
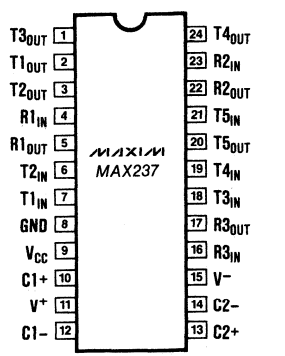


Figure 9. MAX236 Typical Operating Circuit



24 Lead Small Outline
also available.

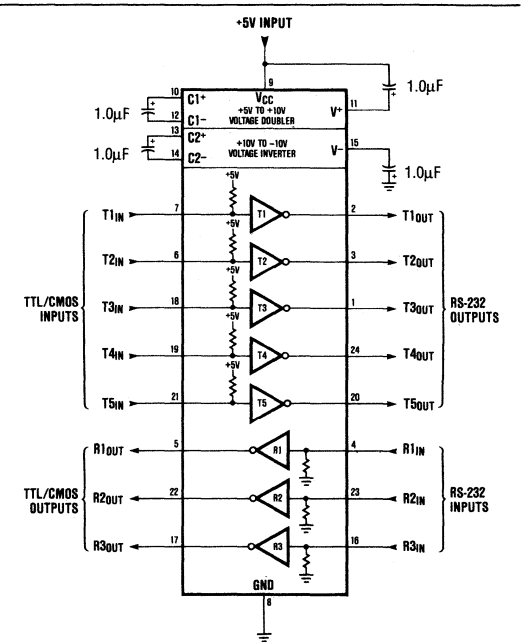
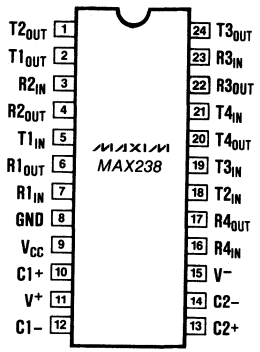


Figure 10. MAX237 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers



24 Lead Small Outline
also available.

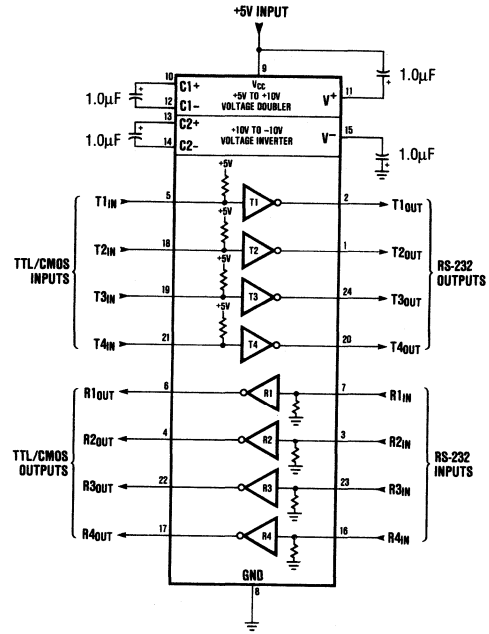
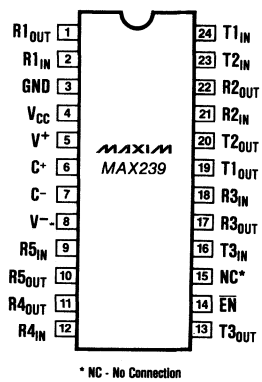


Figure 11. MAX238 Typical Operating Circuit



24 Lead Small Outline
also available.

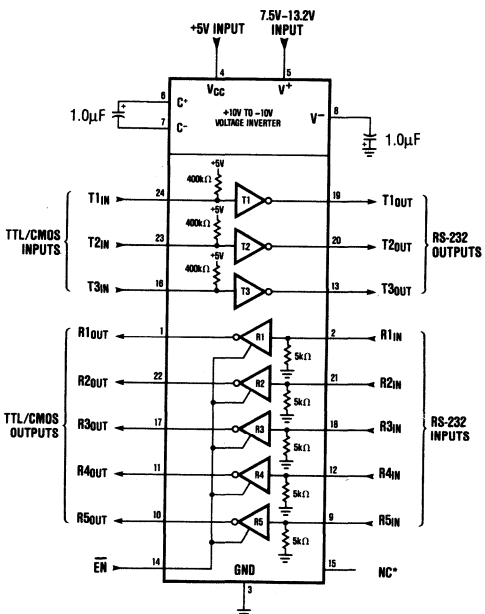
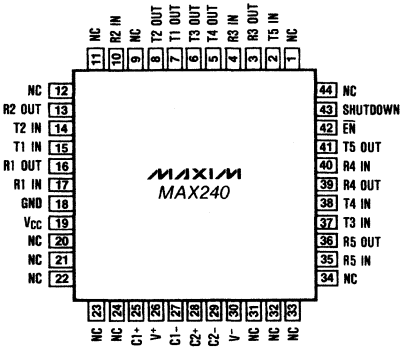


Figure 12. MAX239 Typical Operating Circuit



44 Lead Plastic Flatpak Only

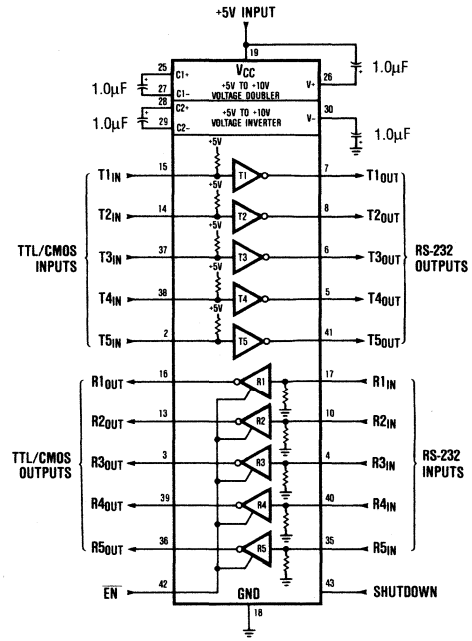
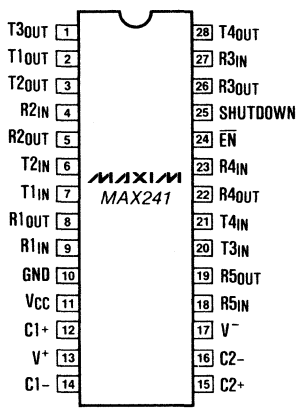


Figure 13. MAX240 Typical Operating Circuit.



28 Lead Wide Small Outline Only

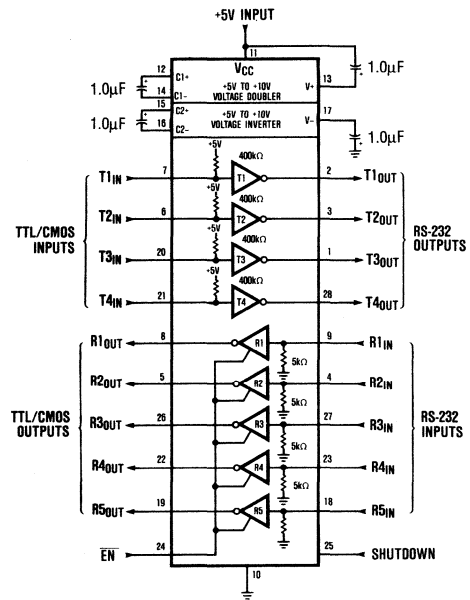


Figure 14. MAX241 Typical Operating Circuit.

+5V Powered RS-232 Drivers/Receivers

Typical Applications

Figures 3 through 14 show typical applications. The capacitor values are non-critical. Reducing the capacitors C1 and C2 to 1μF will slightly increase the impedance of the charge pump, lowering the RS-232 driver output voltages by about 100mV. Lower values of C3 and C4 increase the ripple on the V^+ and V^- outputs.

If the power supply input to the device has a very fast rate-of-rise (as would occur if a PCB were to be plugged into a card cage with power already on), use the simple RC filter shown in Figure 15. This bypass network is not needed if the V_{CC} rate-of-rise is below 1V/μs.

All receivers and drivers are inverting. The $\overline{EN}$able control of the MAX235, MAX236, MAX239, MAX240 and MAX241 enables the receiver TTL/CMOS outputs when it is at a low level, and places the TTL/CMOS outputs of the receivers into a high impedance state when it is a high level.

When the Shutdown control of the MAX230, MAX235, MAX236, MAX240 and MAX241 is at a logic 1 the charge pump is turned off, the receiver outputs are put into the high impedance state, V^+ is pulled down to V_{CC}, V^- is pulled up to ground, and the transmitter outputs are disabled. The supply current drops to less than 10μA.

Detailed Description

The following sections provide supplementary information for those designers with non-standard applications and for those with interest in the internal operation of the devices.

The devices consist of 3 sections: the transmitters, the receivers, and the charge pump DC-DC voltage converter.

+5V to ±10V Dual Charge Pump Voltage Converter

All but the MAX231 and MAX239 convert +5V to ±10V. This conversion is performed by two charge pump voltage converters. The first uses capacitor C1 to double the +5V to +10V, storing the +10V on the V^+ output filter capacitor, C3. The second charge pump voltage converter uses capacitor C2 to invert the +10V to -10V, storing the -10V on the V^- output filter capacitor, C4. The equivalent circuit of the charge pump section is shown in Figure 16.

A small amount of power may be drawn from the V^+ and V^- outputs to power external circuitry. Two Typical Operating Characteristics graphs show typical output voltage versus load current for the MAX230, 234-238, and 241. Transmitter output current is included in these plots. The MAX231-233, which are not shown in the graphs, supply less output current, and are limited to 1 or 2mA of excess output load current.

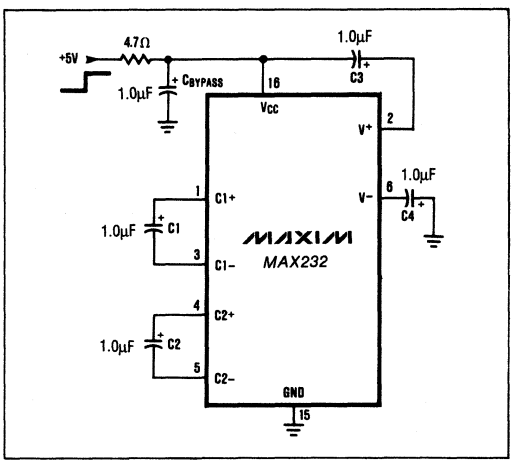


Figure 15. Protection from High $\frac{dV}{dT}$

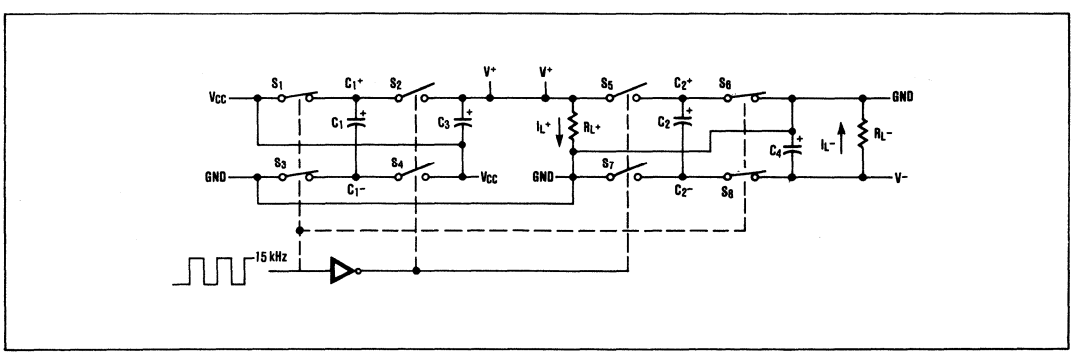


Figure 16. Charge Pump Diagram.

For applications needing only the +5V to ±10V charge pump voltage converter, the MAX680 is available.

The capacitor values for C1 through C4 are noncritical. At the 30kHz (MAX231-MAX233, 60kHz otherwise) typical switching frequency of the voltage converter, a 1µF capacitor has approximately 10Ω impedance and replacing the 4.7µF and 10µF capacitors shown in the typical applications with 1µF for C1 and C2 will increase the output impedance of the V^+ output by about 10Ω and the output imepedance of V^- by about 20Ω. Lowering the value of C3 and C4 increases the ripple on the V^+ and V^- outputs. Where operation to the upper temperature limit is not required, or V_{CC} will not go below 4.75V, C1 and C2 can be 1µF, and C3 and C4 can be 1µF per output channel (1µF if one transmitter is used, 5µF if five transmitters are used).

There are parasitic diodes which become forward biased if V^+ goes below V_{CC} or V^- goes above ground. When in the shutdown mode (MAX230, MAX235, MAX236, MAX240 and MAX241 only), V^+ is internally connected to V_{CC} by a 1kΩ pulldown, and V^- is internally connected to ground via a 1kΩ pullup.

The MAX233 and MAX235 contain all charge pump components, including the capacitors, and operate with NO external components.

The MAX231 and MAX239 include only the V^+ to V^- charge pump, and are intended for applications which have a +5V supply and either a +12V ± 10% supply or a 7.5V to 13.2V battery voltage. When operating with V^+ greater than 8.0V, both capacitors can be 1µF.

Driver (Transmitter) Section

The transmitters or line drivers are inverting level translators which convert the CMOS or TTL input levels to RS-232 or V.28 voltage levels. With +5V V_{CC}, the typical output voltage swing is ±9V when loaded with the nominal 5kΩ input resistance of an RS-232 receiver. The output swing is guaranteed to meet the RS-232/V.28 specification of ±5V minimum output swing under the worst case conditions of all transmitters driving the 3kΩ minimum allowable load impedance, V_{CC} = 4.5V, and maximum operating ambient temperature. The open circuit output voltage swing is from (V^+ - 0.6V) to V^-.

The input thresholds are both CMOS and TTL compatible, with a logic threshold of about 25% of V_{CC}. The inputs of unused drivers sections can be left unconnected; an internal 400kΩ input pullup resistor to V_{CC} will pull the inputs high, forcing the unused transmitter outputs low. The input pullup resistors source about 12µA, and the driver inputs should be driven high or open circuited to minimize power supply current in the shutdown mode.

When in the low power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ. As required by the RS232 and V.28, the slew rate is limited to less than 30V/µs. This limits the maximum usable baud rate to 19,200 baud.

Receiver Section

All but the MAX230 and MAX234 contain RS-232/V.28 receivers. These receivers convert the ±5V to ±15V RS-232 signals to 5V TTL/CMOS outputs. Since the RS-232C/V.28 specifications define a voltage level greater than +3V as a 0, the receivers are inverting. Maxim has set the guaranteed input thresholds of the receivers to 0.8V minimum and 2.4V maximum, which are significantly tighter than the -3.0V minimum and +3.0V maximum required by the RS-232 and V.28 specifications. This allows the receivers to respond both to RS-232/V.28 levels and TTL level inputs. The receivers are protected against input overvoltage up to ±30V.

The 0.8V guaranteed lower threshold is important to ensure that the receivers will have a logic 1 output if the receiver is not being driven because the equipment containing the line driver is turned off or disconnected, or if the connecting cable has an open circuit or short circuit. In other words, the receiver implements Type 1 interpretation of fault conditions (§7 of V.28, §2.5 of RS-232C). While a 0V or even a -3V receiver threshold would be acceptable for the data lines, these lower thresholds would not give proper indication on the control lines such as DTR and DSR. The receivers, on the other hand, have a full 0.8V noise margin for detecting the power-down or cable-disconnected states.

The receivers have a hysteresis of approximately 0.5V, with a minimum guaranteed hysteresis of 200mV. This aids in obtaining clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. The propagation delays of the receivers are 350ns for negative-going input signals, and 650ns for positive-going input signals (see Typical Characteristics graphs).

The MAX239 has a receiver 3-state control line, and the MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low power shutdown control. The receiver TTL/CMOS outputs are in a high impedance 3-state mode whenever the 3-state $\overline{\text{EN}}$able line is high, and are also high impedance whenever the Shutdown control line is high.

+5V Powered RS-232 Drivers/Receivers

Review of EIA Standard RS-232-C and CCITT Recommendations V.28 and V.24

The most common serial interface between electronic equipment is the "RS232" interface. This serial interface has been found to be particularly useful for the interface between units made by different manufacturers since the voltage levels are defined by the EIA Standard RS-232-C and CCITT Recommendation V.28. The RS-232 specification also contains signal circuit definitions and connector pin assignments, while CCITT circuit definitions are contained in a separate document, Recommendation V.24. Originally intended to interface modems to computers and terminals, these standards have many signals which are not used for computer-to-computer or computer-to-peripheral communication.

Serial interfaces can be used with a variety of transmission formats. The most popular by far is the asynchronous format, generally at one of the standard baud rates of 300, 600, 1200, etc. The maximum recommended baud rate for RS-232 and V.28 is 20,000 baud, and the fastest commonly used baud rate is 19,200 baud. Asynchronous serial links use a variety of combinations of the number of data bits, what type (if any) of parity bit, and the number of stop bits. A typical combination is 7 data bits, even parity, and 1 stop bit.

RS232/V.28 physical links are also suitable for synchronous transmission protocols. These higher level protocols often use the standard RS-232C/V.28 voltage levels. Note that one type of physical link (such as RS-232/V.28 voltage levels) can be used for a variety of higher level protocols. Table 2 summarizes the voltage levels and other requirements of V.28 and RS-232.

Comparison of RS-232C/V.28 with other Standards

The other two most common serial interface specifications are the EIA RS423 and RS422/RS485 (CCITT recommendations V.10 and V.11). While the RS-232 or V.28/V.24 interface is the most common interface for communication between equipment made by different manufacturers, the RS423/V.10 interface and RS422/V.11 interfaces can operate at higher baud rates. In addition, the RS485 interface can be used for low cost local area networks.

The RS423 and V.10 interfaces are unbalanced or "single-ended" interfaces which use a differential receiver. This standard is intended for data signaling rates up to 100 kbit/s (100 kilobaud). It achieves this higher baud rate through more precise requirements on the waveshape of the transmitters and through the use of differential receivers to compensate for ground potential variations beween the transmitting and receiving equipment. With certain limitations, this interface is compatible with RS-232 and V.28. The limitations are:

1) less than 20,000 baud rate,
2) maximum cable lengths determined by RS-232 performance,
3) RS423/V.10 DTE and DCE signal return paths must be connected to the the RS232/V.28 signal ground,
4) the RS-232 transmitter output voltages must be limited to ±12V, or additional protection must be provided for the RS423/V.10 receivers, and
5) not all RS232/V.28 receivers will show proper power-off detection of V.10 transmitter outputs.

Maxim's MAX230 and MAX232-MAX238, MAX240 and MAX241 meet restrictions 4 and 5 over the entire range of recommended operating conditions. The MAX231 and MAX239 meet restrictions 4 and 5 provided that the V^+ voltage is 12.5V or less.

The RS422, RS485, and V.11 interfaces are balanced double-current interchanges suitable for baud rates up to 10 Mbit/s. These interfaces are not compatible with RS-232 or V.28 voltage levels.

Application Hints

Operation at High Baud Rates

V.28 states that "the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 percent of the nominal element period on the interchange circuit, whichever is less." RS-232C allows the transition time to be 4 percent of the duration of a signal element. At 19,200 baud, the "nominal element period" is approximately 50μs, of which 3 percent is 1.5μs. Since the transition region is from -3V to +3V, this means the V.28 slew rate would ideally be faster than 6V/1.5μs = 4V/μs at 19.2 kbaud and 2V/μs at 9600 baud. The RS-232 requirement is equivalent to 3V/μs at 19.2 kbaud, 1.5V/μs at 9600 baud, etc. The slew rate of the MAX230 series devices is about 3V/μs with the maximum recommended load of 2500pF. In practice, the effect of less than optimum slew rate is a distortion of the recovered data, where the 1's and 0's no longer have equal width. This distortion generally has negligible effect and the devices can be reliably used for 19.2 kbaud serial links when the cable capacitance is kept below 2500pF. With very low capacitance loading, the MAX230 and MAX234-239, MAX240 and MAX241 may even be used at 38.4 kbaud, since the typical slew rate is 5V/μs when loaded with 500pF in parallel with 5kΩ. Under no circumstance will the

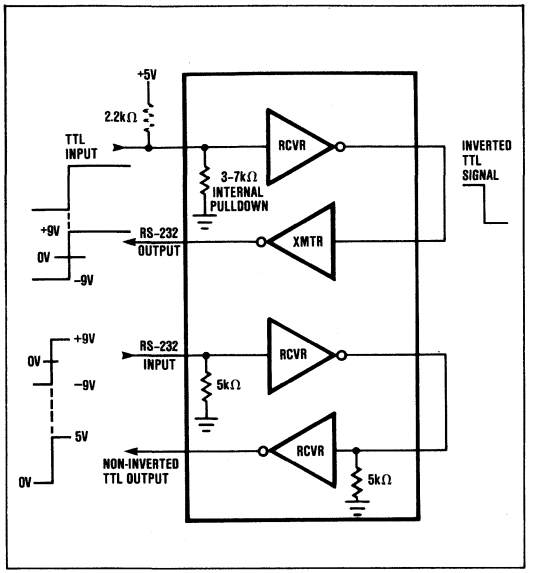


Figure 17. Non-inverting RS-232 Transmitters and Receivers.

slew rate exceed the RS-232/V.28 maximum spec of 30V/μs and, unlike the 1488 driver, no external compensation capacitors are needed under any load condition.

Driving Long Cables

The RS-232 standard states that "The use of short cables (each less than approximately 50 feet or 15 meters) is recommended; however, longer cables are permissible, provided that the load capacitance . . . does not exceed 2500pF."

Baud rate and cable length can be traded off: use lower baud rates for long cables, use short cables if high baud rates are desired. For both long cables and high baud rates, use RS422/V.11. The maximum cable length for a given baud rate is determined by several factors, including the capacitance per meter of cable, the slew rate of the driver under high capacitive loading, the receiver threshold and hysteresis, and the acceptable bit error rate. The receivers have 0.5V of hysteresis, and the drivers are designed such that the slew rate reduction caused by capacitive loading is minimized (see Typical Characteristics).

Non-Inverting Drivers and Receivers

Occasionally a non-inverting driver or receiver is needed instead of the inverting drivers and receivers of the family. Simply use one of the receivers as a TTL/CMOS inverter to get the desired operation (Figure 17). If the logic output driving the receiver input has less than 1mA of output source capability, then add the 2.2kΩ pullup resistor.

The receiver TTL outputs can directly drive the input of another receiver to form a non-inverting RS-232 receiver.

Protection for Shorts to ±15V Supplies

All driver outputs except on the MAX231, MAX232 and MAX233 are protected against short circuits to ±15V, which is the maximum allowable loaded output voltage of an RS-232/V.28 transmitter. The MAX231, MAX232, and MAX233 can be protected against short circuits to ±15V power supplies by the addition of a series 220Ω resistor in each output. This protection is not needed to protect against short circuits to most RS-232 transmitters such as the 1488, since they have an internal short circuit current limit of 12mA.

The power dissipation of the MAX230 and MAX234-MAX239, MAX240 and MAX241 is about 200mW with all transmitters shorted to ±15V.

Isolated RS-232 Interfaces

RS-232 and V.28 specifications require a common ground connection between the two units communicating via the RS-232/V.28 interface. In some cases, there may be large differences in ground potential between the two units, and in other cases it may be desired to avoid ground loop currents by isolating the two grounds. In other cases, a computer or control system must be protected against accidental connection of the RS-232/V.28 signal lines to 110/220VAC power lines. Figure 18 shows a circuit with this isolation. The power for the MAX233 is generated by a MAX635 DC-DC converter. When the MAX635 regulates point "A" to -5V, the isolated output at point "B" will be semi-regulated to +5V. The two optocouplers maintain isolation between the system ground and the RS-232 ground while transferring the data across the isolation barrier. While this circuit will not withstand 110VAC between the RS-232 ground and either the receiver or transmitter lines, the voltage difference between the two grounds is only limited by the optocoupler and DC-DC converter transformer breakdown ratings.

+5V Powered RS-232 Drivers/Receivers

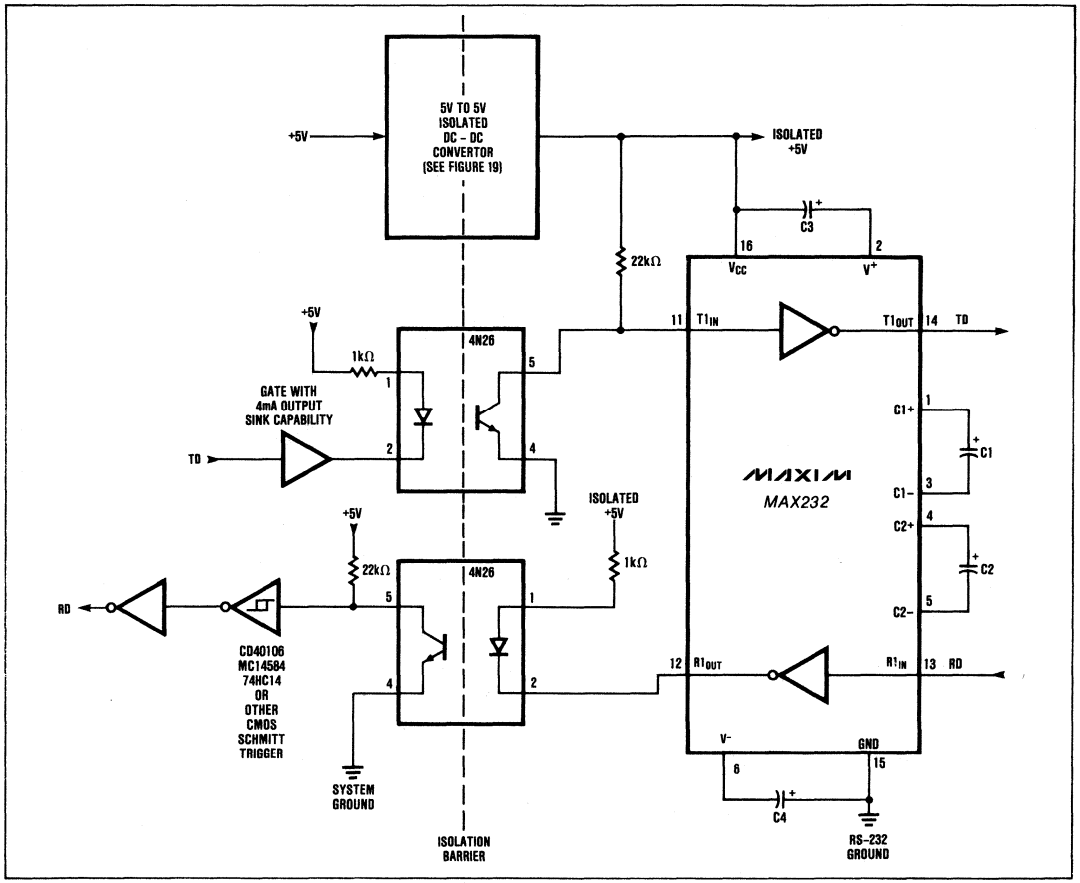


Figure 18. Optically isolated RS-232 Interface.

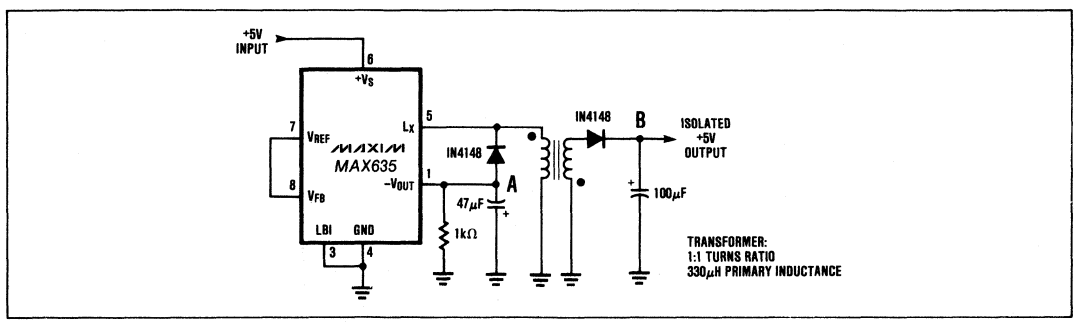


Figure 19. +5V Isolated Power Supply For Optically Isolated RS-232 Interface.

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX230		**0.3" Wide**
MAX230CPP	0°C to +70°C	20 Lead Plastic DIP
MAX230CWP	0°C to +70°C	20 Lead Wide S.O.
MAX230C/D	0°C to +70°C	Dice
MAX230EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX230EWP	-40°C to +85°C	20 Lead Wide S.O.
MAX230EJP	-40°C to +85°C	20 Lead CERDIP
MAX230MJP	-55°C to +125°C	20 Lead CERDIP
MAX231		**0.3" Wide**
MAX231CPD	0°C to +70°C	14 Lead Plastic DIP
MAX231CWE	0°C to +70°C	16 Lead Wide S.O.
MAX231C/D	0°C to +70°C	Dice
MAX231EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX231EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX231EJD	-40°C to +85°C	14 Lead CERDIP
MAX231MJD	-55°C to +125°C	14 Lead CERDIP
MAX232		**0.3" Wide**
MAX232CPE	0°C to +70°C	16 Lead Plastic DIP
MAX232CWE	0°C to +70°C	16 Lead Wide S.O.
MAX232C/D	0°C to +70°C	Dice
MAX232EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX232EJE	-40°C to +85°C	16 Lead CERDIP
MAX232EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX232MJE	-55°C to +125°C	16 Lead CERDIP
MAX233		**0.3" Wide**
MAX233CPP	0°C to +70°C	20 Lead Plastic DIP
MAX233EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX234		**0.3" Wide**
MAX234CPE	0°C to +70°C	16 Lead Plastic DIP
MAX234CWE	0°C to +70°C	16 Lead Wide S.O.
MAX234C/D	0°C to +70°C	Dice
MAX234EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX234EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX234EJE	-40°C to +85°C	16 Lead CERDIP
MAX234MJE	-55°C to +125°C	16 Lead CERDIP
MAX235		**0.6" Wide**
MAX235CPG	0°C to +70°C	24 Lead Plastic DIP*
MAX235EPG	-40°C to +85°C	24 Lead Plastic DIP*
MAX235EDG	-40°C to +85°C	24 Lead Ceramic*
MAX235MDG	-55°C to +125°C	24 Lead Ceramic*

** = 0.600" package*

PART	TEMP. RANGE	PACKAGE
MAX236		**0.3" Wide**
MAX236CNG	0°C to +70°C	24 Lead Plastic DIP
MAX236CWG	0°C to +70°C	24 Lead Wide S.O.
MAX236C/D	0°C to +70°C	Dice
MAX236ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX236EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX236ERG	-40°C to +85°C	24 Lead CERDIP
MAX236MRG	-55°C to +125°C	24 Lead CERDIP
MAX237		**0.3" Wide**
MAX237CNG	0°C to +70°C	24 Lead Plastic DIP
MAX237CWG	0°C to +70°C	24 Lead Wide S.O.
MAX237C/D	0°C to +70°C	Dice
MAX237ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX237EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX237ERG	-40°C to +85°C	24 Lead CERDIP
MAX237MRG	-55°C to +125°C	24 Lead CERDIP
MAX238		**0.3" Wide**
MAX238CNG	0°C to +70°C	24 Lead Plastic DIP
MAX238CWG	0°C to +70°C	24 Lead Wide S.O.
MAX238C/D	0°C to +70°C	Dice
MAX238ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX238EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX238ERG	-40°C to +85°C	24 Lead CERDIP
MAX238MRG	-55°C to +125°C	24 Lead CERDIP
MAX239		**0.3" Wide**
MAX239CNG	0°C to +70°C	24 Lead Plastic DIP
MAX239CWG	0°C to +70°C	24 Lead Wide S.O.
MAX239C/D	0°C to +70°C	Dice
MAX239ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX239EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX239ERG	-40°C to +85°C	24 Lead CERDIP
MAX239MRG	-55°C to +125°C	24 Lead CERDIP
MAX240		**Flatpak**
MAX240CMH MAX240EMH	0°C to +70°C -40°C to +85°C	44 Lead Flatpak 44 Lead Flatpak
MAX241		**0.3" Wide**
MAX241CWI MAX241EWI	0°C to +70°C -40°C to +85°C	28 Lead Wide S.O. 28 Lead Wide S.O.

+5V Powered RS-232 Drivers/Receivers

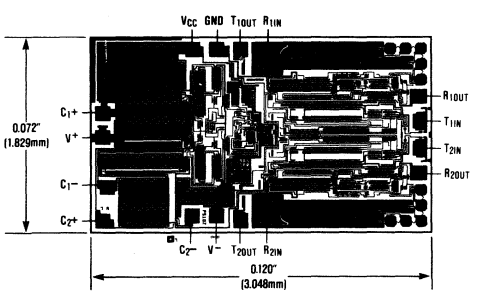
Table 1. Circuits Commonly Used for RS-232C and V.24 Asynchronous Interfaces

PIN	CIRCUIT	
1	Protective Ground	Connect to Earth Ground
2	Transmit Data (TD)	Data from DTE
3	Receive Data (RD)	Data from DCE
4	Request To Send (RTS)	Handshake from DTE
5	Clear to Send (CTS)	Handshake from DCE
6	Data Set ready (DSR)	Handshake from DCE
7	Signal Ground	Reference Point for Signals
8	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
11	Printer Busy Signal	Handshake from Printer
20	Data Terminal Ready	Handshake from DTE
22	Ring Indicator	Handshake from DCE

Table 2. Summary of RS-232C and V.28 Electrical Specifications

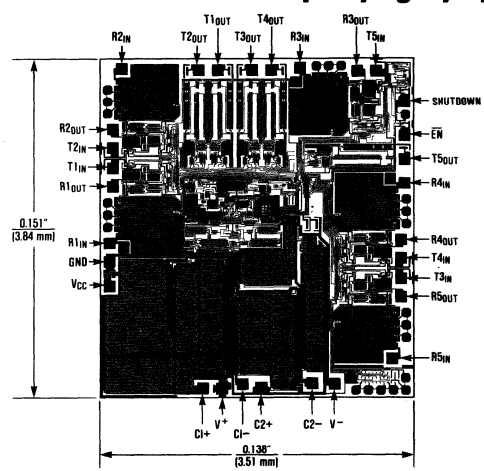
PARAMETER	SPECIFICATION	COMMENTS
Driver Output Voltage		
0 level	+5V to +15V	With 3-7kΩ load
1 level	-5V to -15V	With 3-7kΩ load
Max. output	±25V Max.	No Load
Receiver Input Thresholds (data and clock signals)		
0 level	+3V to +25V	
1 level	-3V to -25V	
Receiver Thresholds RTS, DSR, DTR		
On level	+3V to +25V	
Off level	Open Circuit or -3V to -25V	Detects Power Off Condition at Driver
Receiver Input Resistance	3kΩ to 7kΩ	
Driver Output Resistance, power off condition	300Ω Min.	V_{OUT} < ±2V
Driver Slew Rate	30V/μs Max.	3kΩ < R_L < 7kΩ; 0pF < C_L < 2500pF
Signalling Rate	Up to 20kbits/sec.	
Cable Length	50'/15 m. Recommended Max. Length	Longer cables permissible, if C_{LOAD} ≤ 2500pF

Chip Topography



MAX231, MAX232 and MAX233

Note: Connect substrate to V^+.



MAX230 and MAX234-239, MAX240, MAX241

Notes:
1. Shutdown pin of MAX234, MAX237, MAX238, MAX239, MAX240 and MAX241 are internally connected to ground.
2. Connect substrate to V^+.

19-4323, Rev.0; 7/91

MAXIM

+5V Powered Multi-Channel RS-232 Drivers/Receivers

General Description

The MAX244-249 are +5V enhanced, multiple-channel drivers/receivers ideal for EIA-232D and V.28/V.24 interfaces. All devices feature on-board charge pumps that convert +5V to the ±10V needed to generate EIA-232D levels. The MAX244/248/249 require four external 1µF capacitors; the MAX245/246/247 operate with internal capacitors to save board space and simplify designs.

MAX244: Eight transmitters and ten receivers, with no controls. Requires four external 1µF capacitors.

MAX245: One transmitter enable input controls all eight transmitters outputs. Eight of ten receivers are controlled by one receiver enable input. The two remaining receivers are always active in either low-power or full-speed receive mode. Requires no external capacitors.

MAX246: Two sets of four transmitters and four receivers; each set is controlled by a separate control pin. Two additional receivers are always active in low-power or full-speed receive mode. Requires no external capacitors.

MAX247: Separate transmitter enable inputs control two sets of four transmitters. Separate receiver enable inputs control two sets of four receivers. One additional receiver is always active in low-power or full-speed receive mode. Requires no external capacitors.

MAX248: Separate transmitter enable inputs control two sets of four transmitters. Separate receiver enable inputs control two sets of four receivers. Requires four external 1µF capacitors.

MAX249: Separate transmitter enable inputs control two sets of three transmitters. Separate receiver enable inputs control two sets of five receivers. Requires four external 1µF capacitors.

Features

- ♦ **Operate from a Single +5V Power Supply**
- ♦ **On-Board DC-DC Converter**
- ♦ **Low-Power Receive Mode in Shutdown**
- ♦ **Meet All EIA-232D and V.28 Specifications**
- ♦ **Multiple Drivers and Receivers**
- ♦ **3-State Driver and Receiver Outputs**
- ♦ **64kb/s Data Rate**
- ♦ **25µA Supply Current in Shutdown Mode**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic Dip
MAX245C/D	0°C to +70°C	Dice*
MAX245EPL	-40°C to +85°C	40 Plastic Dip
MAX246CPL	0°C to +70°C	40 Plastic Dip
MAX246C/D	0°C to +70°C	Dice*
MAX246EPL	-40°C to +85°C	40 Plastic Dip

Ordering information continued on last page.

* *Contact factory for dice specifications.*

Selection Table

Device	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Shutdown & Three-State Outputs	Control Pins		Pin-Package
					Transmitter Enable	Receiver Enable	
MAX244	8	10	1µF	N	None	None	44 PLCC
MAX245	8	10	None	Y	$\overline{ENT}$ controls 8 Transmitters	$\overline{ENR}$ controls 8 Receivers, 2 Receivers always Active	40 PDIP
MAX246	8	10	None	Y	$\overline{ENTA}$ control 4 "A" Transmitters & 4 "A" Receivers $\overline{ENTB}$ control 4 "B" Transmitters & 4 "B" Receivers, 2 Receivers always Active		40 PDIP
MAX247	8	9	None	Y	$\overline{ENTA}$ controls 4 "A" Transmitters, $\overline{ENTB}$ controls 4 "B" Transmitters	$\overline{ENRA}$ controls 4 "A" Receivers, $\overline{ENRB}$ controls 4 "B" Receivers, 1 Receiver always Active	40 PDIP
MAX248	8	8	1µF	Y	$\overline{ENTA}$ controls 4 "A" Transmitters, $\overline{ENTB}$ controls 4 "B" Transmitters	$\overline{ENRA}$ controls 4 "A" Receivers, $\overline{ENRB}$ controls 4 "B" Receivers	44 PLCC
MAX249	6	10	1µF	Y	$\overline{ENTA}$ controls 3 "A" Transmitters, $\overline{ENTB}$ controls 3 "B" Transmitters	$\overline{ENRA}$ controls 5 "A" Receivers, $\overline{ENRB}$ controls 5 "B" Receivers	44 PLCC

+5V Powered Multi-Channel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
  T_{IN}, ENA, ENB, ENR, ENT, ENRA, ENRB, ENTA, ENTB ..... -0.3V to (V_{CC} +0.3V)
  R_{IN} ..... ±25V
  T_{OUT} (Note 1) ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} +0.3V)
Short Circuit (1 output at a time)
  T_{OUT} to GND ..... Continuous
  R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  40-Pin Plastic Dip (derate 11.11mW/°C above +70°C) .. 611mW
  44-Pin PLCC (derate 13.33mW/°C above +70°C) 733mW
Operating Temperature Ranges:
  MAX24_C_ _ ..... 0°C to +70°C
  MAX24_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables 2A-2C	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables 2A-2C, normal operation				64	kb/s
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±7.5		V
Output Leakage Current (Shutdown)	Tables 2A-2C			±0.01	±25	µA
				±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 2)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±30		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC}-0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 2A-2C, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current (Normal Operation)	No load			11	30	mA
	3kΩ loads on all outputs			57		
Shutdown Supply Current	TA = +25°C			8	25	µA
	TA = T_{MIN} to T_{MAX}				50	
Control Input	Leakage Current				±1	µA
	Threshold Low			1.4	0.8	V
	Threshold High		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.5	3.5	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay RS-232 to TTL (Low Power Mode), Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time, Figure 4	t_{ET}	MAX246, 247, 248, 249 (excludes charge-pump startup)		5		µs
		MAX245,247 (includes charge-pump startup)		10		ms
Transmitter Disable Time, Figure 3	t_{DT}			100		ns

Note 1: Input voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V.
Note 2: The 300Ω minimum specification complies with EIA-232D, but the actual resistance when in shutdown mode or V_{CC} = 0 is 10MΩ as is implied by the leakage specification.

+5V Powered Multi-Channel RS-232 Drivers/Receivers

Table 1A. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State, RA5 Active	RB1-RB4 3-State, RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low-Power Receive Mode	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State, RA5 Low-Power Receive Mode	RB1-RB4 3-State, RB5 Low-Power Receive Mode

Table 1B. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1-RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receive Mode	RB1-RB4 3-State RB5 Low-Power Receive Mode

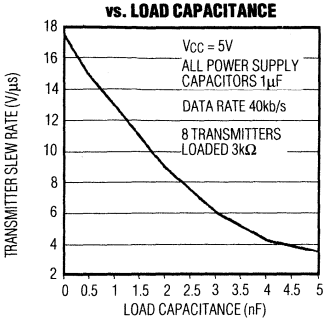
Table 1C. MAX247/248/249 Control Pin Configurations

$\overline{ENTA}$	$\overline{ENTB}$	$\overline{ENRA}$	$\overline{ENRB}$	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB5
					MAX248	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB4
					MAX249	TA1-TA3	TB1-TB3	RA1-RA5	RB1-RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State, except RB5 stays Active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State, except RB5 Low-Power Receive Mode on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247

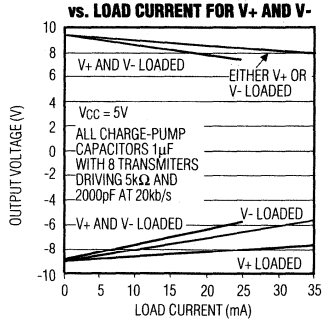
+5V Powered Multi-Channel RS-232 Drivers/Receivers

Typical Operating Characteristics

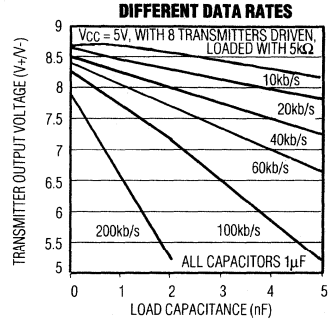
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



OUTPUT VOLTAGE vs. LOAD CURRENT FOR V+ AND V-



MAX244-249 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



Detailed Description

The MAX244-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX244-MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output. The equivalent circuit is shown in Figure 11.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see Typical Operating Characteristics), except on the MAX245-MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA-232D driver output voltage when sourcing current from V+ and V- to external circuitry.

Charge-pump switches on the MAX244/MAX248/MAX249 are optimized for small, inexpensive 1µF capacitors. The MAX743 DC-DC converter is recommended if more than ±10V power is required.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA-232D and V.28 specification, that calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built-in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The driver output slew rate is limited to less than 30V/µs as required by the EIA-232D and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3kΩ and 2500pF.

RS-232 Receivers

EIA-232D and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA-232D and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA-232D.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Receiver and Transmitter Enable Control Inputs

The MAX245-249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1A-1C define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX245 provides ten receivers and eight drivers with separate receiver and transmitter enable controls. The charge pumps turn off and the device shuts down when a logic high is applied to the $\overline{ENT}$ input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). Eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled, ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates less than 20kb/s.

Applications Information

Figures 5-10 show typical operating circuits. V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2, and connected as close as possible to the device in applications that are sensitive to power-supply noise. RS-232 receivers and drivers on all devices invert.

Low-Power Receive Mode

The low-power receive-mode feature puts the IC into shutdown mode, but still allows it to receive information at a slower (20kb/s) data rate. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates (64kb/s max). This operation conserves system power.

+5V Powered Multi-Channel RS-232 Drivers/Receivers

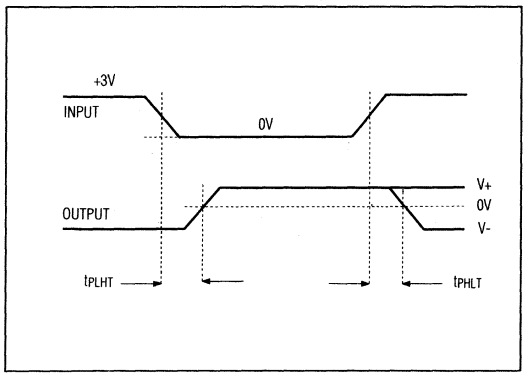


Figure 1. Transmitter Propagation Delay Timing

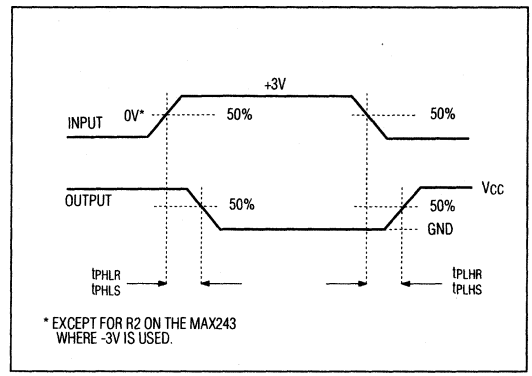


Figure 2. Receiver Propagation Delay Timing

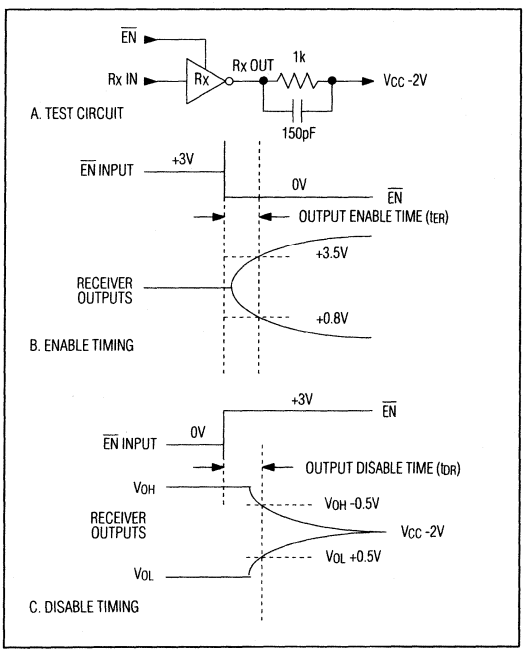


Figure 3. Receiver-Output Enable and Disable Timing

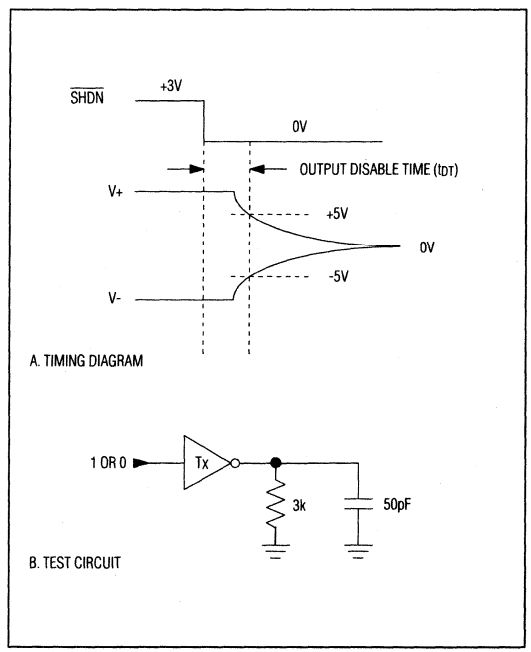
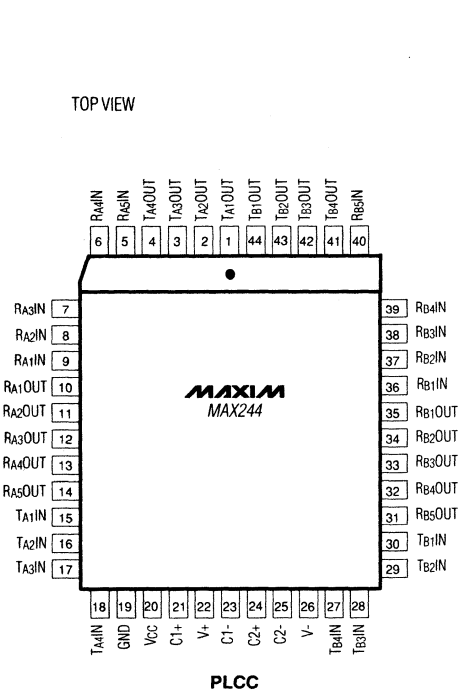
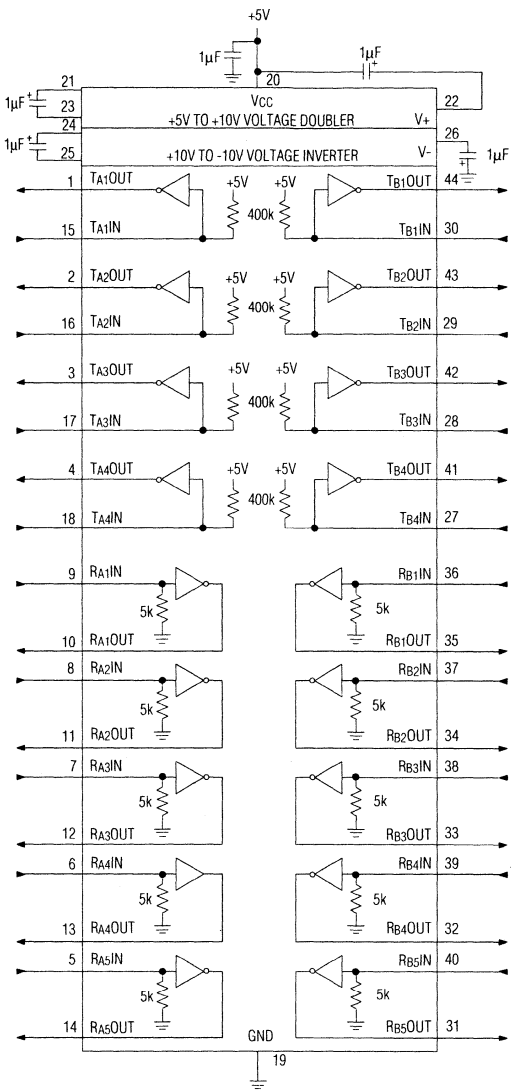


Figure 4. Transmitter-Output Disable Timing





MAX244 Functional Description

10 Receivers Always Active
- 5 A-Side Receivers
- 5 B-Side Receivers

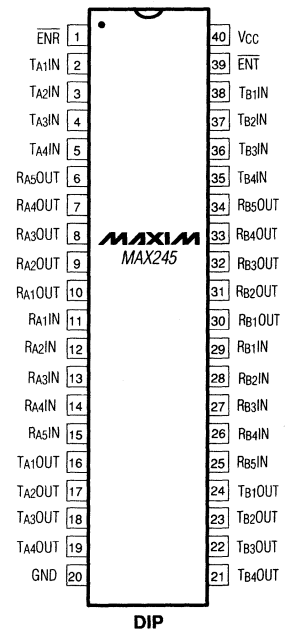
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

No Control Pins

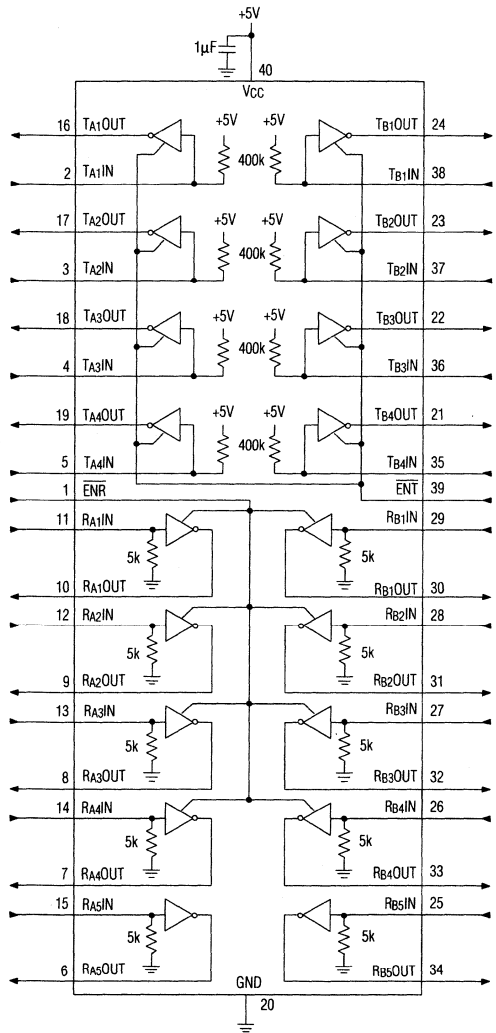
Figure 5. MAX244 Typical Operating Circuit

+5V Powered Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP



MAX245 Functional Description

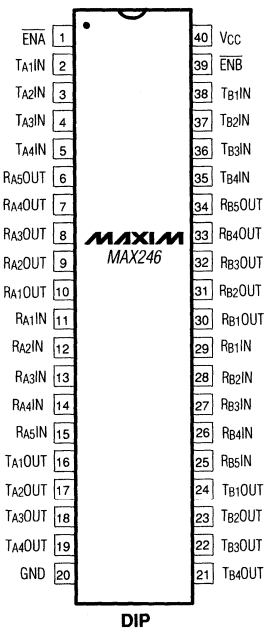
10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

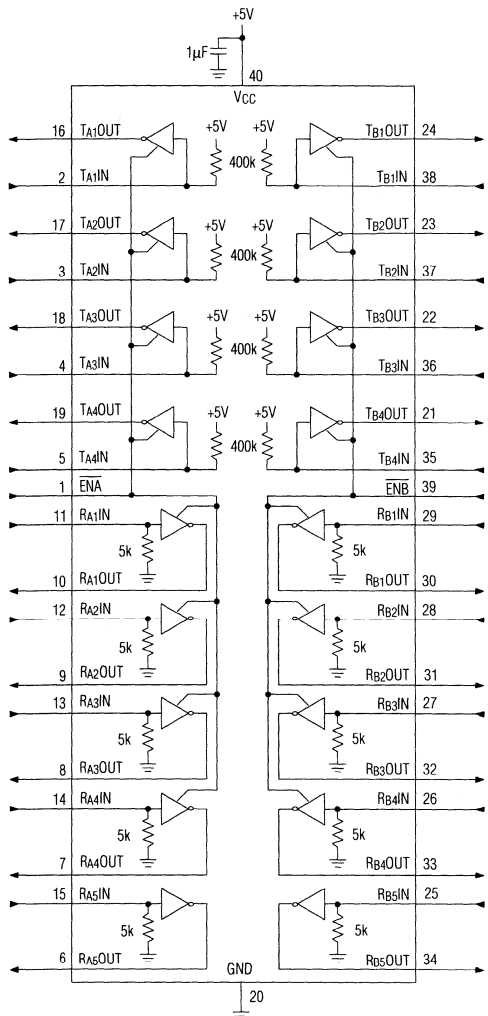
2 Control Pins
- 1 Receiver Enable ($\overline{ENR}$)
- 1 Transmitter Enable ($\overline{ENT}$)

Figure 6. MAX245 Typical Operating Circuit

TOP VIEW



DIP



MAX246 Functional Description

10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

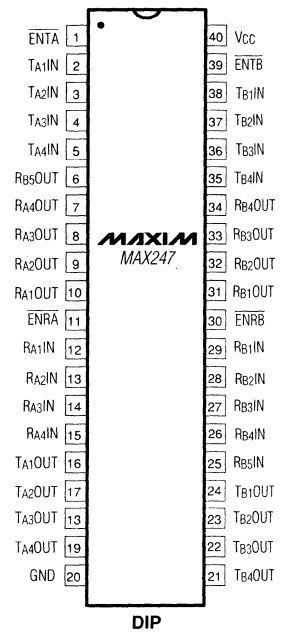
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- Enable A-Side ($\overline{ENA}$)
- Enable B-Side ($\overline{ENB}$)

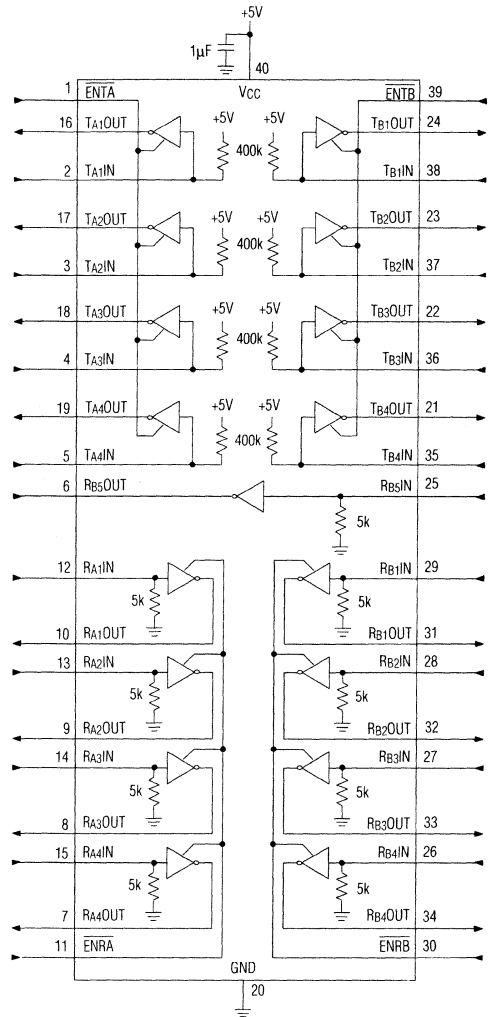
Figure 7. MAX246 Typical Operating Circuit

+5V Powered Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP



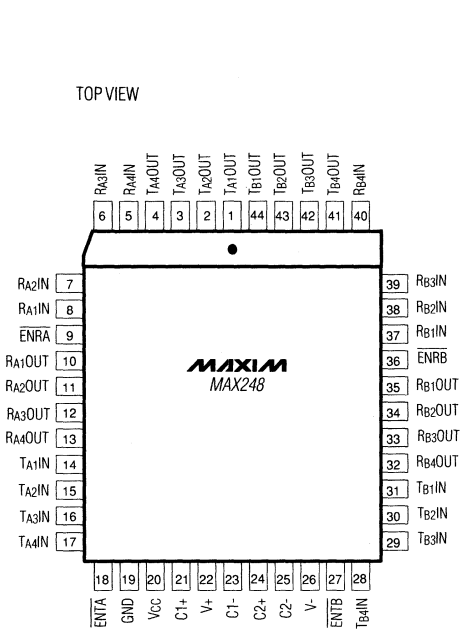
MAX247 Functional Description

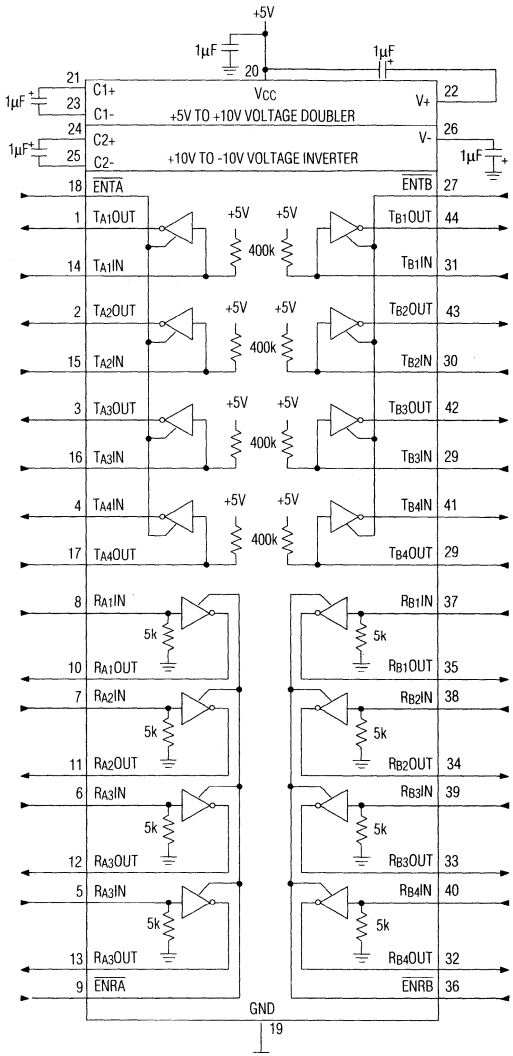
9 Receivers
- 4 A-Side Receivers
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 8. MAX247 Typical Operating Circuit





MAX248 Functional Description

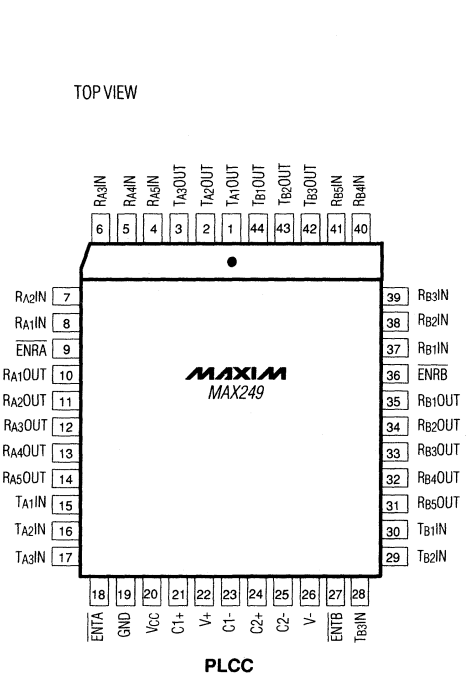
8 Receivers
- 4 A-Side Receivers
- 4 B-Side Receivers

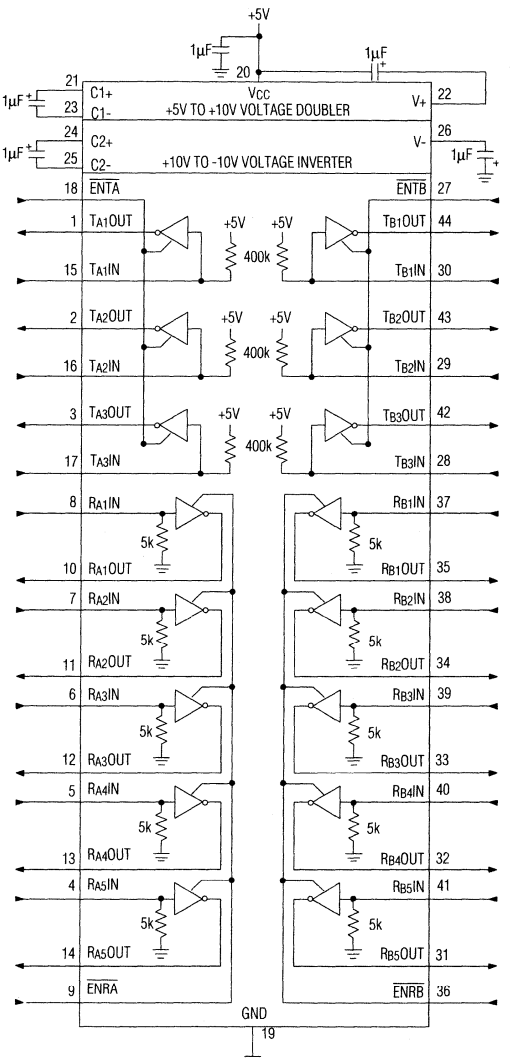
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 9. MAX248 Typical Operating Circuit

+5V Powered Multi-Channel RS-232 Drivers/Receivers





MAX249 Functional Description

10 Receivers
- 5 A-Side Receivers
- 5 B-Side Receivers

6 Transmitters
- 3 A-Side Transmitters
- 3 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 10. MAX249 Typical Operating Circuit

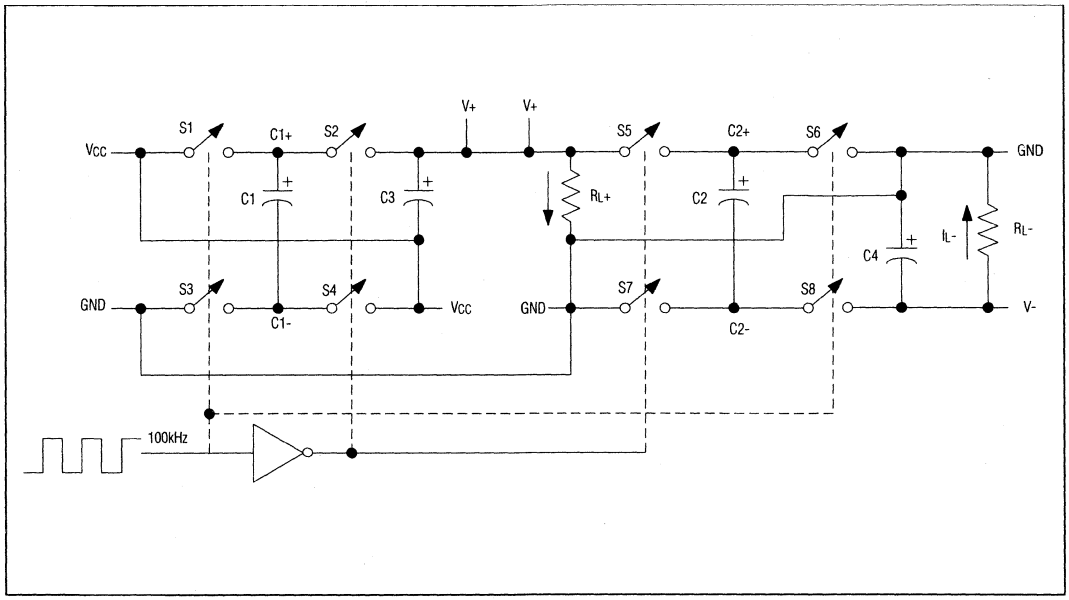


Figure 11. Charge Pump

+5V Powered Multi-Channel RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX247CPL	0°C to +70°C	40 Plastic Dip
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic Dip
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +85°C	44 PLCC

* *Contact factory for dice specifications.*

MAXIM

+5V Powered
Isolated RS-232 Drivers/Receivers

General Description

The MAX250 and MAX251 chip set form the heart of a complete, electrically isolated, RS-232 dual transmitter/receiver. By combining many functions on two chips, the cost and complexity required for an isolated digital interface is greatly reduced. Four low cost optocouplers, four capacitors, a diode and a small pot-core type transformer are all that are required to complete a 19.2k baud transceiver. Faster data rates are possible by using high speed optocouplers. In addition to the driving and receiving circuitry for the optocouplers, the chip set includes a push-pull transformer driver to supply power to the interface's isolated side.

Other convenient features include single +5V operation, a low power shutdown mode, and output enable control for three-state operation. The MAX250 and MAX251 are supplied in 14 lead DIP, 14 lead small outline and 20 leadless chip carrier packages.

The MAX252 has all the required components for RS-232 communication in a single package.

Applications

High Noise Data Communications
Industrial Communications
Data Links To Analog Circuits
Bridge Ground Differentials

Features

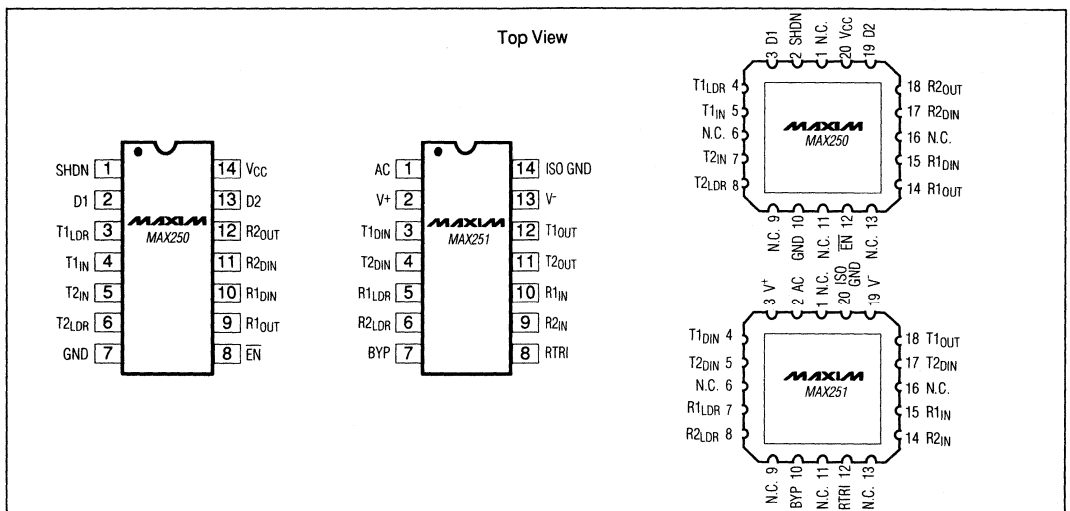
- ♦ **Isolated Data Interface**
- ♦ **Single +5V Supply**
- ♦ **Uses Low Cost Optocouplers**
- ♦ **5μW Low Power Shutdown**
- ♦ **2 Transmitters and 2 Receivers**

Ordering Information

PART	TEMP. RANGE	PACKAGE*
MAX250CPD	0°C to +70°C	14 Lead Plastic DIP
MAX250CSD	0°C to +70°C	14 Lead SO
MAX250C/D	0°C to +70°C	Dice
MAX250EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX250ESD	-40°C to +85°C	14 Lead SO
MAX250EJD	-40°C to +85°C	14 Lead CERDIP
MAX250MJD	-55°C to +125°C	14 Lead CERDIP
MAX250MLP	-55°C to +125°C	20 Lead LCC
MAX251CPD	0°C to +70°C	14 Lead Plastic DIP
MAX251CSD	0°C to +70°C	14 Lead SO
MAX251C/D	0°C to +70°C	Dice
MAX251EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX251ESD	-40°C to +85°C	14 Lead SO
MAX251EJD	-40°C to +85°C	14 Lead CERDIP
MAX251MJD	-55°C to +125°C	14 Lead CERDIP
MAX251MLP	-55°C to +125°C	20 Lead LCC

** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configurations



+5V Powered Isolated RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS: MAX250

Supply Voltage, V_{CC} 6V
Input Voltages ..... -0.3V to (V_{CC} +0.3V)
Output Drive Current, D1, D2 ..... 240mA
Output Drive Voltage, D1, D2 ..... V_{CC} + 6V
Opto Driver pins $T1_{LDR}$, $T2_{LDR}$, $R1_{OUT}$ and $R2_{OUT}$ may be shorted one at a time indefinitely to V_{CC} or GND

Power Dissipation
Plastic DIP (derate 7mW/°C above 70°C) 375mW
CERDIP (derate 9.5mW/°C above 70°C) 675mW
Small Outline (derate 7mW/°C above 70°C) 375mW
LCC (derate 7mW/°C above 70°C) 375mW
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX250

(V_{CC} = 5V ±10%, T_A = Full Temperature Range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Over Temp.	4.5		5.5	V
Operating Supply Current	I_{CC}	D1, D2 Open		0.1	0.5	mA
Shutdown Supply Current	I_{CS}	Shutdown T_A = -40°C to +85°C T_A = -55°C to +125°C		1	10 100	µA
Input Currents	$I_{\overline{EN}}$, I_{SHDN}	Input = GND to V_{CC}		0.001	1	µA
POWER DRIVER D1, D2						
Switch Frequency	$f_{D1, D2}$	V_{CC} = 5V, T_A = 25°C	100	200	275	kHz
ON Resistance Power Driver	$r_{DS(ON)}$	At 25 mA		25	50	Ω
Leakage Current					10	µA
Zener Clamp Voltage	V_{CL}	w. r. t. V_{CC}	6	8	10	V
DRIVER SECTION						
Pull-up Current Input source	I_P	V_{CC} = 5V, V_{IN} = 0V, T_A = 25°C	2	3	6	µA
Current Output Source	I_S	V_{OUT} = 1.4V, T_A = 25°C	-5	-8	-15	mA
TTL/CMOS Output Voltage Low	V_{OL}	I_{OUT} = 3.2mA			0.4	V
TTL/CMOS Output Voltage High	V_{OH}	I_{OUT} = -1.0mA	2.4			V
Input Logic Threshold High	V_{IH}	T_{IN}, R_{DIN}, $\overline{EN}$, Shutdown		1.8	2.4	V
Input Logic Threshold Low	V_{IL}	T_{IN}, R_{DIN}, $\overline{EN}$, Shutdown	0.8	1.3		V
Input Hysteresis	V_{IHYS}			0.5		V
Leakage Current Input and Output	I_L	($\overline{EN}$ or Shutdown) = V_{CC}			10	µA
Input Capacitance	C_{IN}			5		pF

ABSOLUTE MAXIMUM RATINGS: MAX251

Positive Input Voltage, AC terminal 15V
Positive Input Voltage, V^+ terminal 14V
Negative Input Voltage, V^- terminal ..... -14V
RS-232 Input Voltage ..... -30V to 30V
RS-232 Applied Output Voltage ..... -15V to 15V
Tristate Input Voltage, V_{RTRI} ..... -0.3V to (V^+ + 0.3V)
RS-232 Transmitters may be indefinitely shorted to GND
Opto Driver pins $R1_{LDR}$, $R2_{LDR}$ may be shorted one at a time indefinitely to GND

Diode Forward Current (AC to V^+) 250mA
Reverse Diode Voltage ..... -28V
Power Dissipation
Plastic DIP (derate 7mW/°C above 70°C) 375mW
CERDIP (derate 9.5mW/°C above 70°C) 675mW
Small Outline (derate 7mW/°C above 70°C) 375mW
LCC (derate 7mW/°C above 70°C) 375mW
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX251

(Test Circuit 1, See Figure 3, T_A = Full Temperature Range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	I^+	$R_L = \infty$		0.7	2.5	mA
Negative Supply Current	I^-	$R_L = \infty$		0.45	1.0	mA
RS-232 CHARACTERISTICS						
RS-232 Output Voltage Swing	T_{VS}	All Transmitter Outputs loaded with 3kΩ to Ground	±5	±7.2		V
RS-232 Output Leakage Current	T_{OL}	$V^+ = V^- = 0V$ $T_{OUT} = ±15V$	-10		+10	µA
RS-232 Input Threshold High	V_{IH}			1.8	3.0	V
RS-232 Input Threshold Low	V_{IL}		0.6	1.2		V
RS-232 Input Hysteresis	V_{IHYS}			0.6		V
RS-232 Input Resistance		$T_A = 25°C$	3		7	kΩ
3-State Enable	t_{EN}			3.5		µs
3-State Disable	t_{DS}			1.0		µs
Transmitter Slew Rate		$R_L = 3kΩ$, $C_L = 2500pF$	3			V/µs
OPTOINTERFACE CHARACTERISTICS						
Input Pull-up Current	I_P	$T_A = 25°C$	2.5	4	6	µA
Input Pull-up Voltage Clamp	V_{PCL}	w. r. t. ISO GND		3		V
Input Threshold Voltage High	V_{IH}			1.5	2	V
Input Threshold Voltage Low	V_{IL}		0.8	1.2		V
Input Hysteresis Voltage	V_{IHYS}			0.3		V

+5V Powered Isolated RS-232 Drivers/Receivers

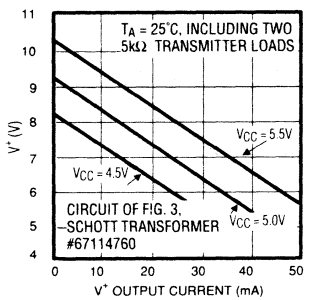
ELECTRICAL CHARACTERISTICS: MAX251 (continued)

(Test Circuit 1, See Figure 3, T_A = Full Temperature Range unless otherwise noted.)

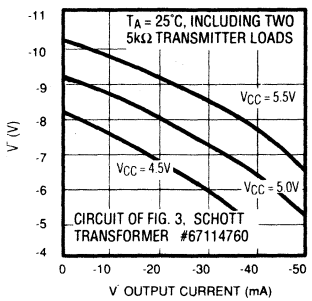
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Source Current	I_{PH}	V_{OUT} = 1.4V, T_A = 25°C	-12	-7	-5	mA
Output Voltage Low	V_{OL}	I_{OUT} = 3.2mA			0.4	V
Output Leakage Current, $R1_{LDR}$, $R2_{LDR}$	I_L	(RTRI or Shutdown) = +5V			10	µA
3-STATE CONTROL						
Pulldown Current	I_{TPD}	V = GND	10	4	1	µA
Threshold Voltage	V_T		0.6	1.4	2	V

Typical Operating Characteristics

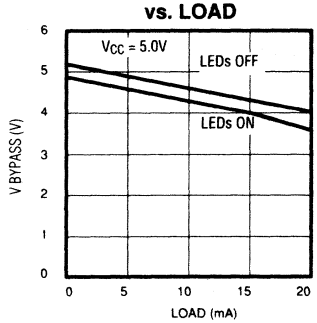
MAX251 V+ SUPPLY VOLTAGE vs. LOAD CURRENT



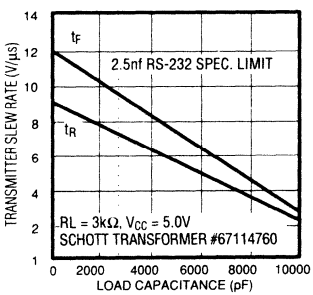
MAX251 V- SUPPLY VOLTAGE vs. LOAD CURRENT



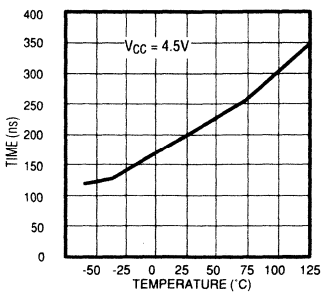
MAX251 V BYPASS vs. LOAD



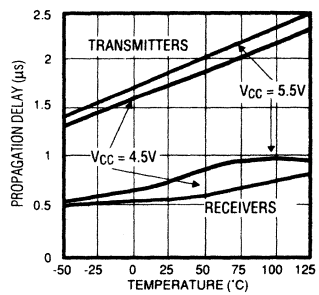
MAX251 TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



MAX250 PROPAGATION DELAY vs. TEMPERATURE

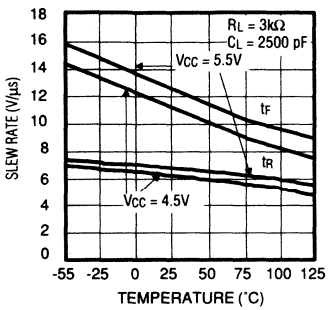


MAX251 PROPAGATION DELAY vs. TEMPERATURE

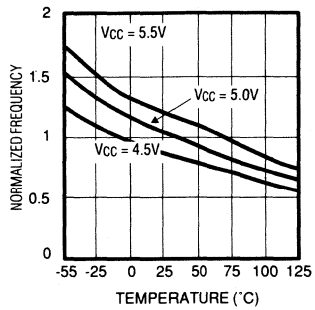


Typical Operating Characteristics (continued)

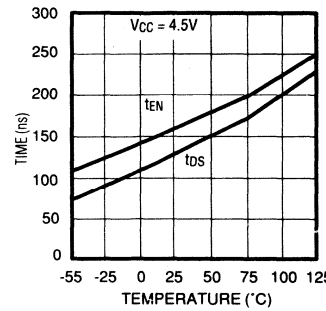
MAX251 TRANSMITTER SLEW RATE vs. TEMPERATURE



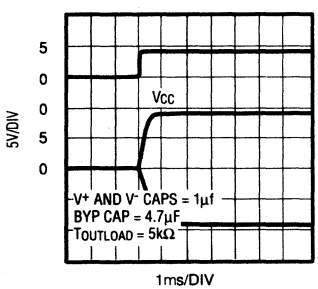
MAX250 D1, D2 SWITCH FREQUENCY vs. TEMPERATURE



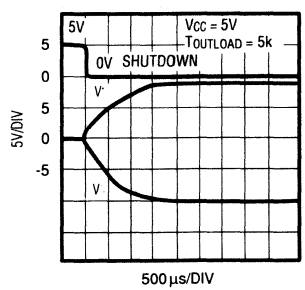
MAX250 ENABLE, DISABLE TIME vs. TEMPERATURE



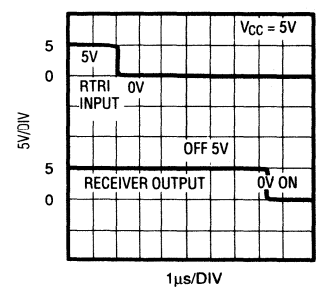
POWER UP DELAY FROM MAX250 V_{CC} TO MAX251 TRANSMITTER OUTPUTS



TIME FROM SHUTDOWN TO POWER UP



RTRI DELAY TIME TO RECEIVER OUTPUT ACTIVE



+5V Powered Isolated RS-232 Drivers/Receivers

Pin Description

MAX250 LCC PIN#	MAX250 DIP & SO PIN#	SYMBOL	DESCRIPTION
1	-	N.C.	
2	1	SHDN	Shutdown: When+5V, turns off the oscillator, disconnects driver input pull-up resistors and opens D1, D2. For normal operation, ground shutdown.
3	2	D1	Open Drain of Transformer Driver MOSFET
4	3	$T1_{LDR}$	Transmitter #1 LED Driver
5	4	$T1_{IN}$	TTL/CMOS Transmitter #1 Input
6	-	N.C.	
7	5	$T2_{IN}$	TTL/CMOS Transmitter #2 Input
8	6	$T2_{LDR}$	Transmitter #2 LED Driver
9	-	N.C.	
10	7	GND	Ground
11	-	N.C.	
12	8	$\overline{EN}$	Output Enable: When +5V, Pins $T1_{LDR}$, $T2_{LDR}$, $R1_{OUT}$ and $R2_{OUT}$ go Hi impedance
13	-	N.C.	
14	9	$R1_{OUT}$	TTL/CMOS Receiver #1 Output
15	10	$R1_{DIN}$	Receiver #1 Detector Input
16	-	N.C.	
17	11	$R2_{DIN}$	Receiver #2 Detector Input
18	12	$R2_{OUT}$	TTL/CMOS Receiver #2 Output
19	13	D2	Open Drain of Transformer Driver MOSFET
20	14	V_{CC}	+5V Positive Supply Voltage

MAX251 LCC PIN#	MAX251 DIP & SO PIN#	SYMBOL	DESCRIPTION
1	-	N.C.	
2	1	AC	Anode of Input Power Supply Diode
3	2	V^+	Positive Supply Output Terminal
4	3	$T1_{DIN}$	Transmitter #1 Detector Input
5	4	$T2_{DIN}$	Transmitter #2 Detector Input
6	-	N.C.	
7	5	$R1_{LDR}$	Receiver #1 LED Driver
8	6	$R2_{LDR}$	Receiver #2 LED Driver
9	-	N.C.	
10	7	BYP	Internal V_{CC} Bypass Point
11	-	N.C.	
12	8	RTRI	Receiver Output 3-State: When +5V, Receiver Outputs go Hi impedance
13	-	N.C.	
14	9	$R2_{IN}$	RS-232 Receiver #2 Input
15	10	$R1_{IN}$	RS-232 Receiver #1 Input
16	-	N.C.	
17	11	$T2_{OUT}$	RS-232 Transmitter #2 Output
18	12	$T1_{OUT}$	RS-232 Transmitter #1 Output
19	13	V^-	Negative Supply Output Voltage
20	14	ISO GND	Isolated Ground

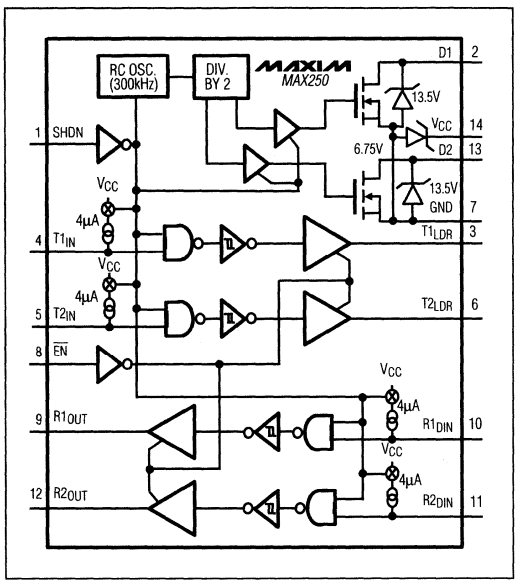


Figure 1. MAX250 Block Diagram

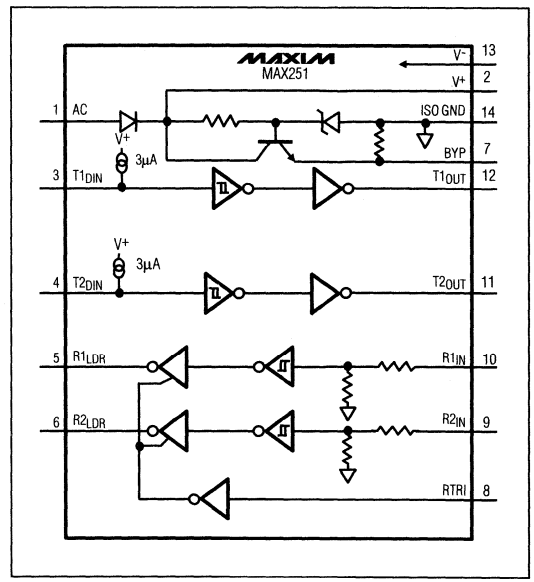


Figure 2. MAX251 Block Diagram

Typical Applications

Figure 3 shows the typical connection for a complete 19.2k baud isolated RS-232 circuit. Figure 3 also shows how 4N26 optocouplers can be replaced by 6N136 devices to achieve 90k baud rates.

A recommended printed circuit board layout is shown in Figure 4. This may be modified for individual designs but two important factors should be considered. 1.) To maximize isolation, the "isolation line" through the center of Figure 4 should not be breached. Connections and components from one side should not be located near those of the other side. 2.) Since the optocoupler outputs are relatively high impedance nodes, they should be located as close as possible to the MAX250 and MAX251. This minimizes stray capacitance and maximizes data rate.

When the MAX250's shutdown input (SHDN) is taken high, power is removed from the MAX251, and the RS-232 transmitter outputs ($T1_{OUT}$, $T2_{OUT}$) go to high impedance states. Timing plots in the Typical Operating Characteristics section show the turn-on and enable delays for various control functions.

The circuit in Figure 4 has been laid out so that it can be used for either a one or two sided PC board. The lines that are thick from one IC pad to the next IC pad are on the bottom side. Lines that are broken by a thin line can either go on the top side of the board or on the bottom side with jumpers where the thin lines appear. At no time should any lines cross the middle of the board at the isolation barrier.

The MAX250 and MAX251 have a logic inversion in the optocoupler when using the standard configuration. For applications where no inversion is required, or more LED drive current is needed, Figure 5 shows the output structure of the LDR output. The LDR output can typically source 7mA and sink 25mA. Because of the higher sinking capability, a current limiting resistor is required.

Detailed Description

The MAX250 and MAX251, together with four optocouplers and a transformer, form an isolated dual RS-232 transmitter and receiver (See Figure 3). The MAX250 connects to the non-isolated or "logic" side of the interface, translating logic signals to and from the optocouplers, while the MAX251 resides on the isolated or "cable" side, translating data between the optocouplers and RS-232 line drivers and receivers. In addition to the optocoupler drivers and receivers, the MAX250 also contains isolation transformer drive circuitry which supplies power to the isolated side of the interface, and the MAX251.

+5V Powered Isolated RS-232 Drivers/Receivers

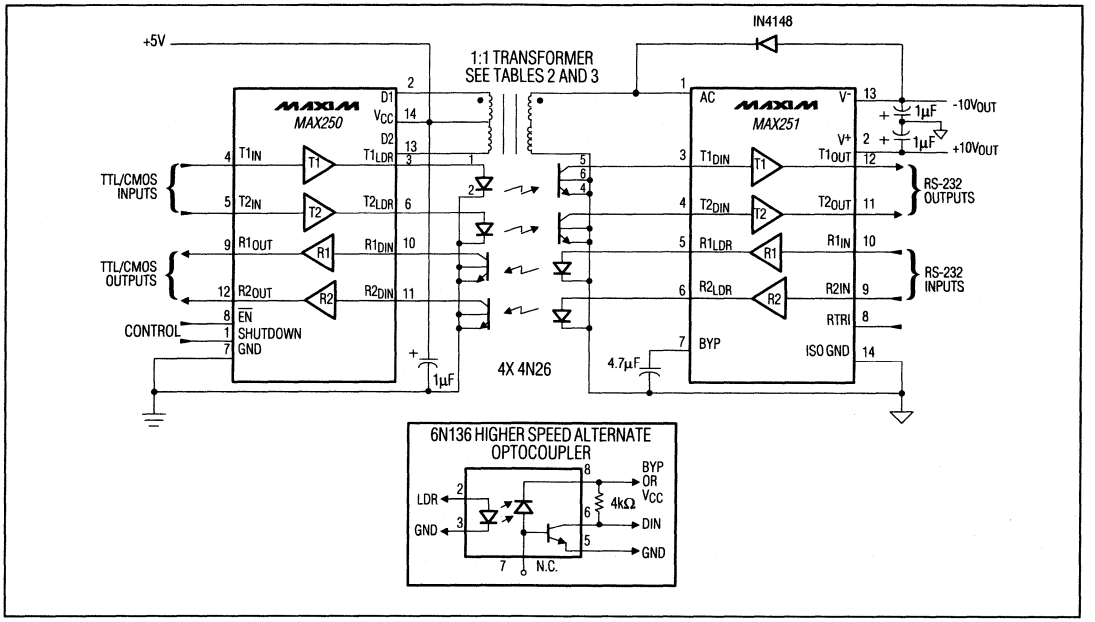


Figure 3. Isolated RS-232 Interface

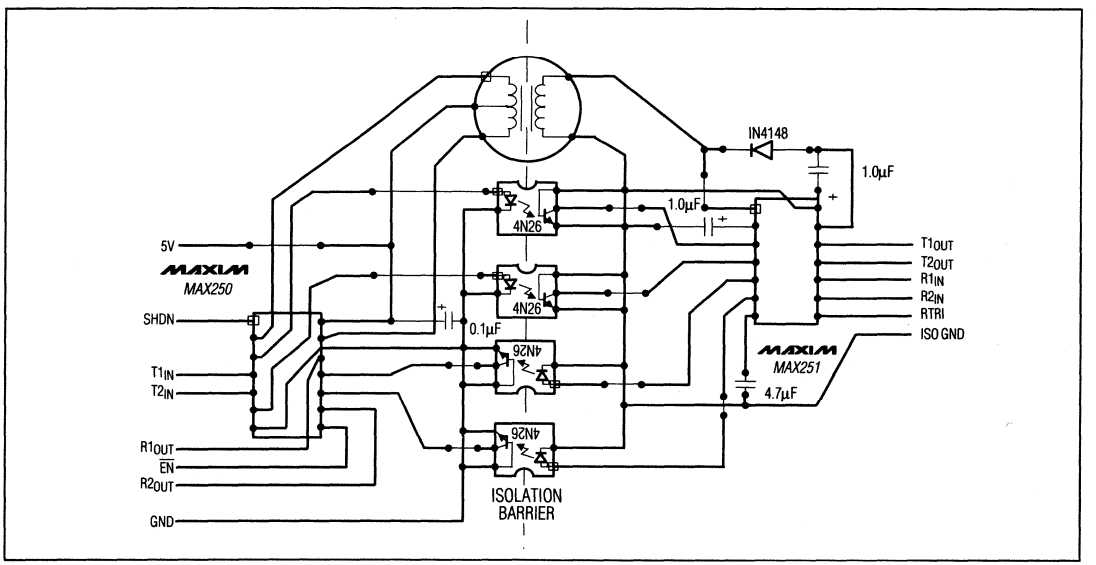


Figure 4. Recommended PC Board Layout for Dual Channel, Optoisolated, Self-Powered RS-232

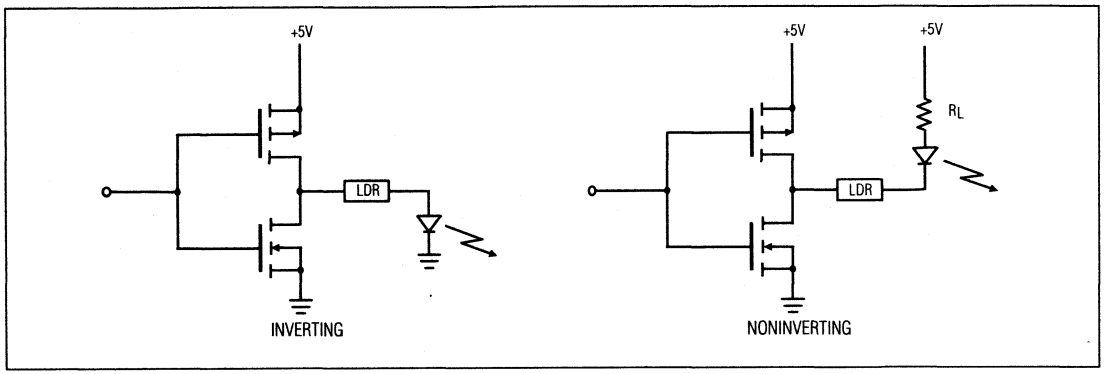


Figure 5. LDR Output Structure

MAX250

The MAX250 contains four identical noninverting drivers whose outputs may be used either as optocoupler LED drivers or as TTL/CMOS logic outputs. Each driver input ($T1_{IN}$, $T2_{IN}$, $R1_{DIN}$, $R2_{DIN}$) has a "weak" 4µA internal pull-up current source, and 0.5V of hysteresis to improve noise rejection. The input logic thresholds conform to standard TTL/CMOS specifications.

In normal operation, the MAX250 driver outputs ($T1_{LDR}$, $T2_{LDR}$, $R1_{OUT}$, $R2_{OUT}$) source 7mA via internal current sources and do not require limiting resistors when driving grounded optocoupler LEDs or CMOS/TTL logic inputs. The outputs can also sink up to 25mA when the current is limited by external resistors.

D1 and D2 are open-drain N-Channel MOSFETs which drive an external isolation transformer in push-pull fashion at 150kHz with a 50% duty cycle. A 1:1 transformer turns ratio provides a 10V peak-to-peak output at the secondary. Specifications and suitable manufacturer's part numbers for this transformer are listed in Tables 2 and 3. No transformer snubbers are required because D1 and D2 are protected against switching transients by internal 13.5V zener clamp diodes as shown in Figure 1.

The MAX250 functions also include an output enable control (EN) and a SHUTDOWN pin (SHDN). EN puts all driver outputs into a high impedance state when driven high. SHDN, when pulled high, disables the following MAX250 functions:

1.) Disables D1 and D2;

2.) Turns off the oscillator;

3.) Shuts off 4µA pull-up currents at driver inputs;

4.) Resets driver outputs to a low state;

5.) Lowers power consumption to 5µW.

MAX251

The MAX251 connects to the "cable" side of the RS-232 interface and includes two line drivers and receivers along with circuitry to translate these levels to optocoupler signals. The RS-232 inputs ($R1_{IN}$, $R2_{IN}$) and outputs ($T1_{OUT}$, $T2_{OUT}$) completely conform to all EIA RS-232C and CCITT V.28 specifications. The receiver outputs ($R1_{LDR}$, $R2_{LDR}$) source 7mA and can drive optocoupler inputs without external current limiting resistors. The MAX251 transmitter inputs ($T1_{DIN}$, $T2_{DIN}$) contain 4µA internal pull-ups which allow direct connection to optocoupler output transistors, again without external resistors.

When the MAX251's RTRI input is pulled high, the receiver outputs ($R1_{LDR}$, $R2_{LDR}$) are disabled and go to a high impedance state. In normal operation, this pin is left open or grounded.

Optocoupler Limitations

In Figure 3, the 4N26 optocouplers are connected in "diode mode" to optimize cost and data rate. While Current Transfer Ratio (CTR) is generally unspecified for this configuration, optocouplers from several manufacturers have been successfully tested in this circuit. The MAX250/MAX251 require a minimum optocoupler current transfer ratio of 0.12%, but may exhibit data rate limitations from the combined effect of higher MAX250/MAX251 drive and high optocoupler CTR.

The 6N136 optocouplers, shown in the inset in Figure 3 and listed in Table 1, operate in phototransistor mode, with limiting values of CTR specified by the manufacturers.

If further information is required, please contact Maxim Applications.

+5V Powered Isolated RS-232 Drivers/Receivers

Component Selection

Optoisolators

Optoisolator manufacturers are listed in Table 1 for easy selection. The MAX250/251 combination can be used with a 4N26 to obtain a 19.2k baud rate when used in the diode-to-diode mode (base tied to the emitter). When the MAX250/251 is used with the 6N136, a 90k baud rate can be achieved when a 4kΩ pull-up resistor to 5V is used on pin 6 of the 6N136.

Table 1. Manufacturers of Optoisolators

PART NO.	MFGS	SUGGESTED R_L	V_{IOS} (V_{PK})	TYP. PROP t_{PHL}	t_{PLH}
4N25	MOT,PHL,QT,SM,TRW*	NONE[2]	2500V	14µs	6.3µs
4N26	MOT,PHL,QT,SM,TRW	NONE[2]	1500V	14µs	4.3µs
6N136	HP,QT,TRW	4K	2500V	1.8µs	1.5µs

* MOT= Motorola Inc. (303) 337-3434
PHL= Phillips (401) 232-0500
QT = Quality Technologies (General Instrument) (415) 493-0400
SM = Siemens Components (408) 257-7910
TRW= TRW Electronic Components Group (214) 323-2200

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.
Note 2: When used with a MAX250/251.

Transformers

Table 2 is a list of transformer characteristics that should be used to customize your own transformer. Table 3 is a list of transformers that are compatible with the MAX250/251 chip set. The list includes both transformers that are small and more expensive and transformers that are larger and less expensive.

Table 2. Transformer Characteristics

Pri. Inductance	1mH to 2.5mH
Pri. Leakage Inductance	30µH
Turns Ratio	1:1 Pri. center tapped
ET	50V-µs
Switching Frequency	150kHz
Interwinding Capacitance	< 100pF
DC Resistance	< 2Ω
Ipk	300mA
Dielectric Strength	> 1500 VAC/1sec.

Table 3. Transformers Selection for Common Designs

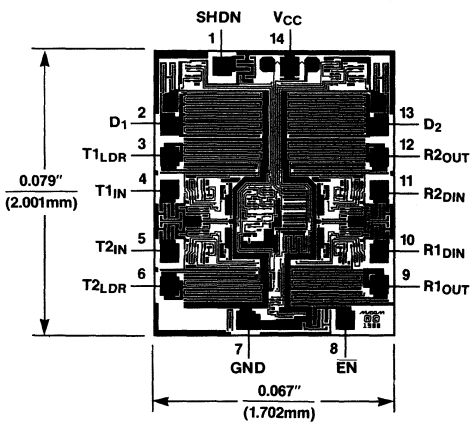
MANUFACTURERS	LESS EXPENSIVE	SMALL
BH ELECTRONICS 604 Michigan Rd. Marshall, MN 56258 (507) 532-3211	Q6471-1	Q6471-2
MINI-MAGNETICS 1100 Fulton Place Fremont, CA 94539-7077 (415) 490-7500	MM2757	MM2758
SCHOTT Corporation 1000 Parkers Lake Rd. Minneapolis, MN 55391 (612) 475-1173	67114760	67117970

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

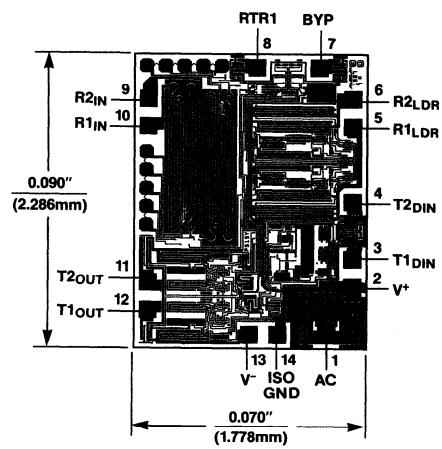
Chip Topographies

2

MAX250



MAX251



19-2370; Rev. 1; 4/91

MAXIM

Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

General Description

The MAX252 complete, electrically-isolated, dual RS-232 transmitter/receiver system requires no external components. By combining many functions in one package, the cost and complexity of an isolated digital interface are greatly reduced.

A single +5V supply powers both sides of the interface. Transceivers, optocouplers, and a transformer in one low-cost package provide a complete interface up to 9600 bits/sec. Additional pins provide low-power shutdown and a high-impedance state for both transmitter outputs.

The MAX252A withstands 130V_{RMS} (continuous), 1260V_{RMS} (1 min.) or 1520V_{RMS} (1 sec.) and is intended for applications where very high transient voltages, differential ground potentials or noise may be encountered. The MAX252A is UL recognized. The MAX252B is intended for less stringent applications and is rated for 500V_{RMS} (1 min.) or 600V_{RMS} (1 sec.).

Receivers and line drivers (transmitters) meet EIA RS-232D and CCITT V.28 specifications. The MAX252 is supplied in 40-pin plastic DIP packages in commercial (0°C to +70°C) and extended (-40°C to +85°C) temperature ranges.

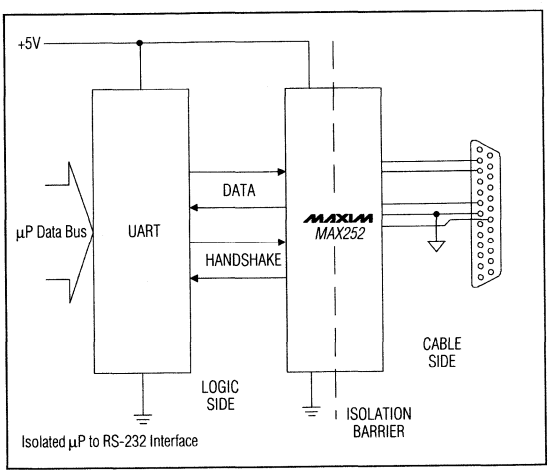
Applications

High-Noise Environments

Automatic Test Equipment

Differential Ground Potentials

Typical Application



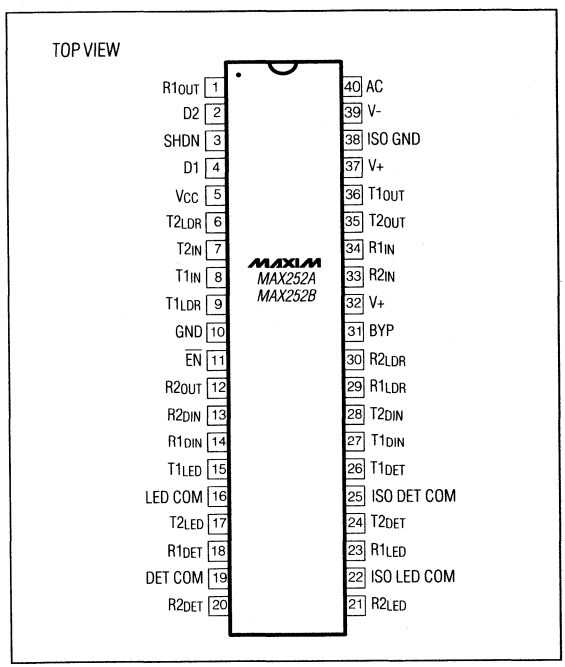
Features

- ♦ **Isolated Data Interface**
- ♦ **No External Components**
- ♦ **Single +5V Supply**
- ♦ **50µW Low-Power Shutdown**
- ♦ **Two Transmitters and Two Receivers**
- ♦ **UL Recognized (MAX252A) - File E118032 to UL1577**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX252ACHL	0°C to +70°C	40 Plastic Module
MAX252BCHL	0°C to +70°C	40 Plastic Module
MAX252AEHL	-40°C to +85°C	40 Plastic Module
MAX252BEHL	-40°C to +85°C	40 Plastic Module

Pin Configuration



Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

ABSOLUTE MAXIMUM RATINGS

Voltages with respect to GND (pin 10)
- Supply Voltage, V_{CC} ..... -0.3V to +6V
- Input Voltage
  - Pins 3, 7, 8, 11, 13, 14, 18, 20 ..... -0.3V to (V_{CC} +0.3V)

Voltages with respect to ISO GND (pin 38)
- RS-232 Input Voltage (pins 33, 34) ..... -30V to +30V
- RS-232 Applied Output Voltage (pins 35, 36) ... -15V to +15V
- Pins 32, 37 (V+) ..... +15V
- Pins 24, 26, 31 ..... V+
- RS-232 Transmitter outputs may be shorted individually and indefinitely to ISO GND.

LED Forward Continuous Current (pins 15, 17, 21, 23) ...30mA

Power Dissipation
- Plastic DIP (derate 10mW/°C above +70°C) 650mW

Operating Temperature Ranges:
- MAX252ACHL/BCHL ..... 0°C to +70°C
- MAX252AEHL/BEHL ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ISOLATION (Note 1)							
Test Voltage	V_{ISO}	T_A = +25°C MAX252A	1sec.	1520			V_{RMS}
			1 min. (Note 2)	1260			
			Continuous (Note 2)	130			
		MAX252B	1 sec.	600			
			1 min. (Note 2)	500			
Leakage Current		10 sec., V_{ISO} = 500V_{RMS}, 60Hz, T_A = +25°C			10	50	μA_{RMS}
Isolation Resistance		T_A = +25°C 500V_{DC}			10^{10}		Ω
Capacitance		0V			10		pF
POWER SUPPLY							
Operating Supply Current	I_{CC}	T_A = +25°C, SHDN = 0V	$T1_{IN}$, $T2_{IN}$, $R1_{IN}$, $R2_{IN}$ = V_{CC}		60	90	mA
			$T1_{IN}$, $T2_{IN}$, $R1_{IN}$, $R2_{IN}$ = 0		8	15	
Shutdown Supply Current	I_{CS}	SHDN = 1V			1	10	µA
$\overline{EN}$, SHDN Input Current	I_{EN}, I_{SHDN}	Input = GND to V_{CC}			0.001	1	µA
TTL/CMOS INPUTS/OUTPUTS							
TTL/CMOS Input Pull-Up Current	I_P	V_{IN} = 0V			4	20	µA
TTL/CMOS Output Voltage Low	V_{OL}	I_{OUT} = 3.2mA				0.4	V
TTL/CMOS Output Voltage High	V_{OH}	I_{OUT} = -1.0mA		3.5			V
Input Logic Threshold High	V_{IH}	$T1_{IN}$, $T2_{IN}$, $\overline{EN}$, SHDN			1.8	2.4	V
Input Logic Threshold Low	V_{IL}	$T1_{IN}$, $T2_{IN}$, $\overline{EN}$, SHDN		0.8	1.3		V
Input Hysteresis		$T1_{IN}$, $T2_{IN}$			0. 5		V
Leakage Current, Output Disabled	I_L	$T1_{IN}$, $T2_{IN}$; $\overline{EN}$ or SHDN = V_{CC}				10	µA
Input Capacitance	C_{IN}	$T1_{IN}$, $T2_{IN}$			5		pF

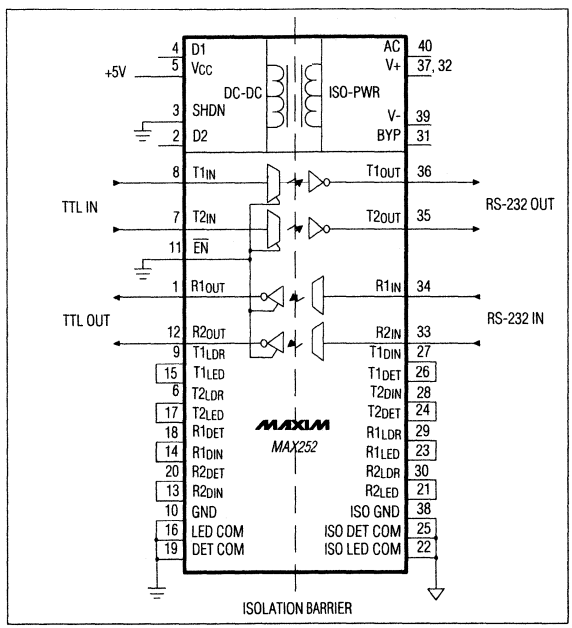
Note 1: Pins 1-20 tied together and pins 21-40 tied together.
Note 2: Value derived from 1 sec. test.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 CHARACTERISTICS						
RS-232 Output Voltage Swing	V_{PP}	$T1_{OUT}$, $T2_{OUT}$, R_L = 3kΩ to ISO	±5	±7.2		V
RS-232 Output Leakage Current		V+ = V- = 0V or SHDN = V_{CC}, $T1_{OUT}$, $T2_{OUT}$ = ±15V	-10		+10	µA
RS-232 Input Threshold High		$R1_{IN}$, $R2_{IN}$		1.8	3.0	V
RS-232 Input Threshold Low		$R1_{IN}$, $R2_{IN}$	0.6	1.2		V
RS-232 Input Hysteresis		$R1_{IN}$, $R2_{IN}$		0.6		V
RS-232 Input Resistance		$R1_{IN}$, $R2_{IN}$, T_A = +25°C	3		7	kΩ
Transmitter Output Slew Rate	SR	R_L = 3kΩ, C_L = 2500pF Sample Tested Measured from +3v to -3V or -3V to +3V		3	30	V/µs
Propagation Delay	t_R	RS-232 to TTL		24		µs
	t_T	TTL to RS-232		20		
Transmission Rate		Sample Tested R_L = 3kΩ C_L = 2500pF	9600	19200		Bits/sec.

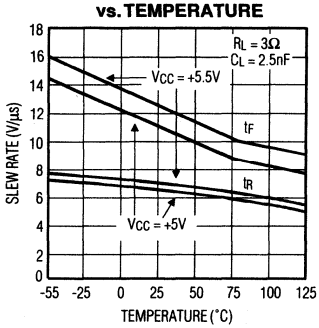
Typical Operating Circuit



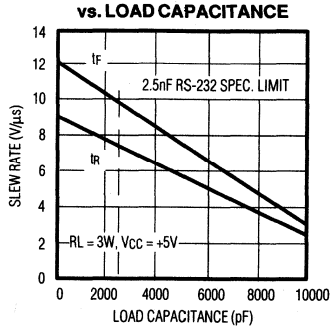
Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

Typical Operating Characteristics

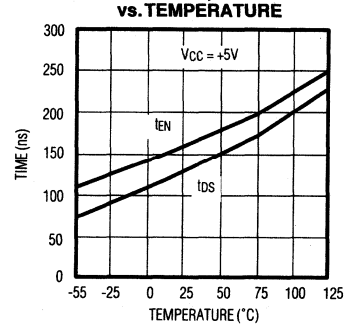
MAX252 TRANSMITTER SLEW RATE vs. TEMPERATURE



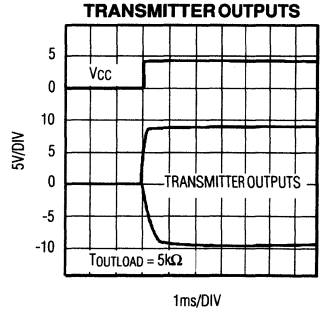
MAX252 TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



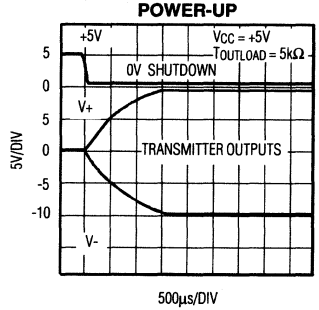
MAX252 ENABLE, DISABLE TIME vs. TEMPERATURE



POWER-UP DELAY TO TRANSMITTER OUTPUTS



TIME FROM SHUTDOWN TO POWER-UP



Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

Pin Description

PIN #	NAME	FUNCTION
1	$R1_{OUT}$	Receiver #1 Output; TTL/CMOS logic levels
2	D2	Internal Connection. Leave this pin unconnected. Do not ground.
3	SHDN	Shutdown. When high, turns off the oscillator and disconnects driver inputs. Ground for normal operation.
4	D1	Internal Connection. Leave this pin unconnected. Do not ground.
5	V_{CC}	+5V Supply Voltage
6	$T2_{LDR}$	Transmitter #2 LED Driver
7	$T2_{IN}$	Transmitter #2 Input; TTL/CMOS logic levels
8	$T1_{IN}$	Transmitter #1 Input; TTL/CMOS logic levels
9	$T1_{LDR}$	Transmitter #1 LED Driver
10	GND	Ground
11	$\overline{EN}$	Output Enable. If High, $T1_{LDR}$, $T2_{LDR}$, $R1_{OUT}$, and $R2_{OUT}$ go to high-impedance state. Ground for normal operation.
12	$R2_{OUT}$	Receiver #2 Output; TTL/CMOS logic levels
13	$R2_{DIN}$	Receiver #2 Detector Input
14	$R1_{DIN}$	Receiver #1 Detector Input
15	$T1_{LED}$	T1 LED Anode Input
16	LED COM	Common $T1_{LED}$, $T2_{LED}$ Cathode. Tie to Ground.
17	$T2_{LED}$	T2 LED Anode Input
18	$R1_{DET}$	R1 Photodiode Cathode Output
19	DET COM	Common $R1_{DET}$, $R2_{DET}$ Anode. Tie to Ground.
20	$R2_{DET}$	R2 Photodiode Cathode Output

PIN #	NAME	FUNCTION
21	$R2_{LED}$	R2 LED Cathode Input
22	ISO LED COM	Common $R1_{LED}$, $R2_{LED}$ Cathode. Tie to Isolated Ground.
23	$R1_{LED}$	R1 LED Cathode Input
24	$T2_{DET}$	T2 Photodiode Anode Output
25	ISO DET COM	Common $T1_{DET}$, $T2_{DET}$ LED Anode. Tie to Isolated Ground.
26	$T1_{DET}$	T1 Photodiode Anode Output
27	$T1_{DIN}$	Transmitter #1 Detector Input
28	$T2_{DIN}$	Transmitter #2 Detector Input
29	$R1_{LDR}$	Receiver #1 LED Driver
30	$R2_{LDR}$	Receiver #2 LED Driver
31	BYP	Internal Connection. Leave this pin unconnected. Do not ground.
32	V+	Isolated Positive Supply
33	$R2_{IN}$	RS-232 Receiver #2 Input
34	$R1_{IN}$	RS-232 Receiver #1 Input
35	$T2_{OUT}$	RS-232 Transmitter #2 Output
36	$T1_{OUT}$	RS-232 Transmitter #1 Output
37	V+	Isolated Positive Supply
38	ISO GND	Isolated Ground
39	V–	Isolated Negative Supply Voltage
40	AC	Internal Connection. Leave this pin unconnected. Do not ground.

Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

Isolation Applications

The MAX252 is intended for industrial communications and control applications where voltage transients, differential ground potentials or high noise may be encountered. The MAX252A withstands 130V_{RMS} (continuous), 1260V_{RMS} (1 min.) or 1520V_{RMS} (1 sec.). For less stringent applications, the MAX252B is rated at 500V_{RMS} (1 min.) or 600V_{RMS} (1 sec.). For applications requiring higher isolation ratings or transmission rates greater than 9600 baud, Maxim recommends the MAX250 and MAX251 device set that uses external optocouplers and transformer.

Figure 1 shows the typical interconnection for a complete 9600 bits/sec. transceiver. Important layout considerations include:

* For maximum isolation, the isolation line through the center of Figure 1 should not be breached; connections from each side should be kept separate.

* Optocoupler outputs (pins 18, 20, 24, and 26) are high-impedance nodes, so connecting traces should be as short as possible to minimize stray capacitance and maximize data transfer rate; shunt capacitance seen by each pin should not exceed 10pF.

The MAX252 pin out enables optimal printed circuit board layout by minimizing interconnect lengths and crossovers. Figure 2 shows the preferred layout, which is strongly recommended for 9600 bits/sec. applications. Note the position of the ground traces, particularly the protection of pin 20 by the wraparound from pin 19.

Isolation Example

Figure 3 illustrates how to isolate an existing RS-232 interface by inserting a MAX252 and MAX233 in series. Both devices invert while translating RS-232 to TTL and TTL to RS-232 levels. Since there is no net inversion, the circuit functions like two plain pieces of wire, but with 1520V_{RMS} (at 1 sec.) isolation between the ports.

Detailed Description

The MAX252 contains two integrated circuits, four optocouplers, four capacitors, two diodes, and a small transformer. Together, these provide a complete, isolated, dual RS-232 transmitter and receiver. The non-isolated or logic side of the interface transfers logic signals to and from the optocouplers, while the isolated or cable side transfers data between the optocouplers and RS-232

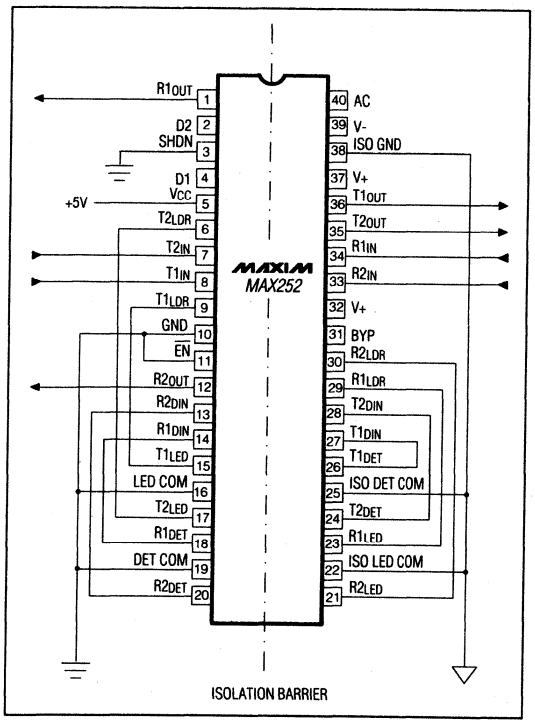


Figure 1. Typical Interconnections

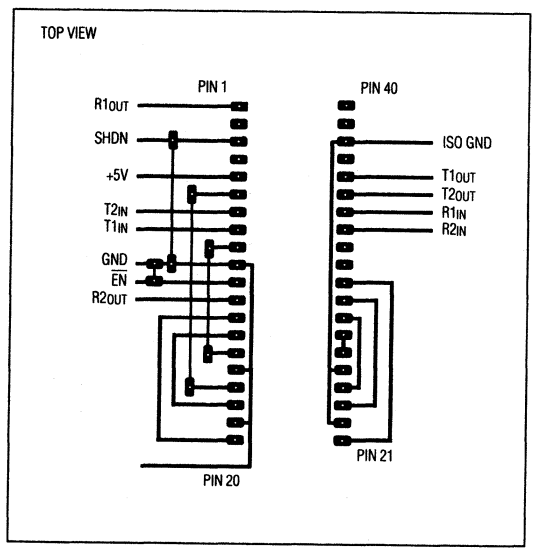


Figure 2. Preferred Layout

Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

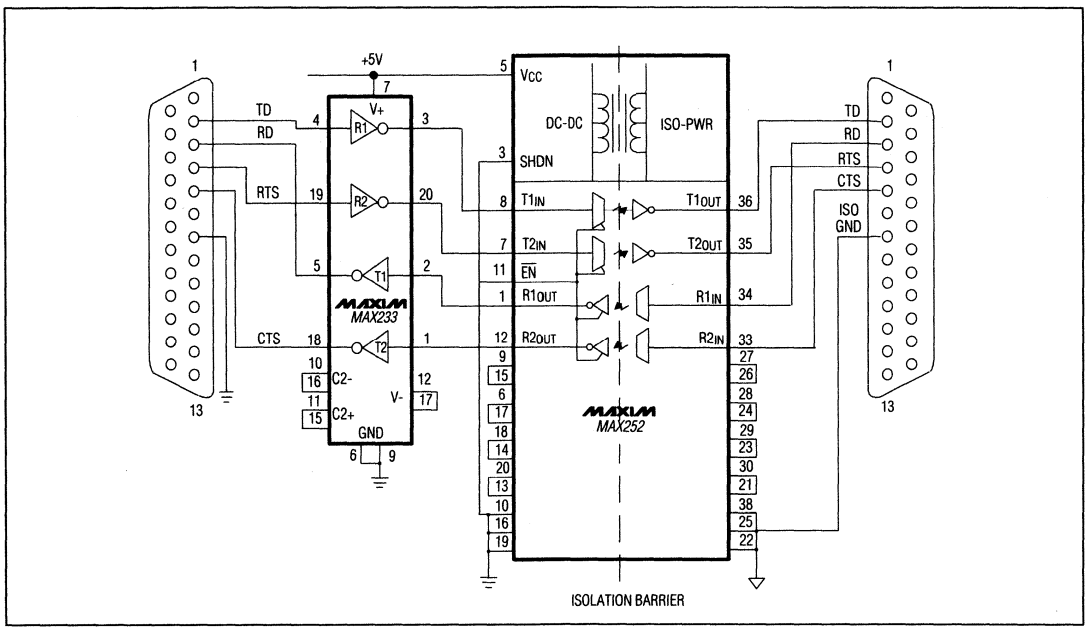


Figure 3. RS-232 Isolation Adapter from a Single +5V Supply

transmitters (line drivers) and receivers. The MAX252 also contains an isolation transformer and drive circuitry to supply power to the isolated side of the interface.

On the logic side of the MAX252 are four identical non-inverting drivers whose outputs may be used either as optocoupler LED drivers or as TTL/CMOS logic outputs. Each driver input ($T1_{IN}$, $T2_{IN}$, $R1_{DIN}$, $R2_{DIN}$) has a weak 4µA internal pull-up current source, and 0.5V hysteresis to improve noise rejection; logic thresholds for the driver inputs conform to standard TTL/CMOS specifications.

The RS-232 side of the interface includes two line drivers and receivers along with circuitry to translate these levels to optocoupler signals. The RS-232 inputs ($R1_{IN}$, $R2_{IN}$) and outputs ($T1_{OUT}$, $T2_{OUT}$) conform to EIA RS-232D and CCITT V.28 specifications. The inputs to the RS-232 line drivers ($T1_{DIN}$, $T2_{DIN}$), which are normally strapped to the internal optoisolators, are TTL/CMOS compatible.

Also included are an OUTPUT ENABLE control ($\overline{EN}$) and a SHUTDOWN pin (SHDN). $\overline{EN}$ places all driver outputs in a high-impedance state when driven high. SHDN, when pulled high, performs the following functions:

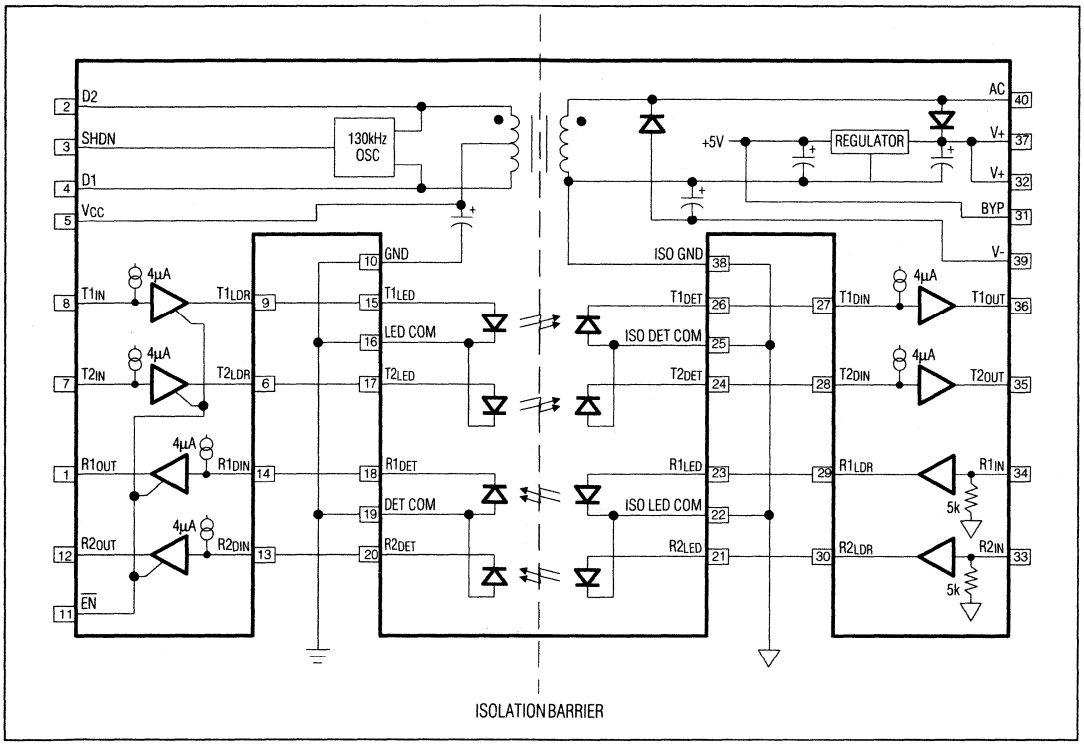
1) Turns off the 130kHz oscillator, removing power from the RS-232 side of the interface.
2) Places $T1_{OUT}$ and $T2_{OUT}$ in a high-impedance state.
3) Disables the 4µA pull-up currents at the logic-side driver inputs ($T1_{IN}$, $T2_{IN}$, $R1_{DIN}$, $R2_{DIN}$).
4) Resets logic-side driver outputs ($T1_{LDR}$, $T2_{LDR}$, $R1_{OUT}$, $R2_{OUT}$) to low.
5) Reduces power consumption to 50µW.

Module Product Reliability

For reliability data on Maxim's Module Product Line, see Reliability Report RR-3A .

Complete, +5V-Powered, Isolated, Dual RS-232 Transceiver Module

MAX252 Block Diagram

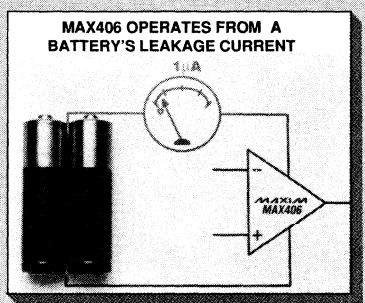


MAXIM

Op Amps/Buffers/Comparators

1µA Op Amp Extends Battery Life 15X

Output Swings Rail-to-Rail, Drives 2000 Times Supply Current



At 1.2µA max supply current, the MAX406 operates with a current as low as a battery's typical leakage current.

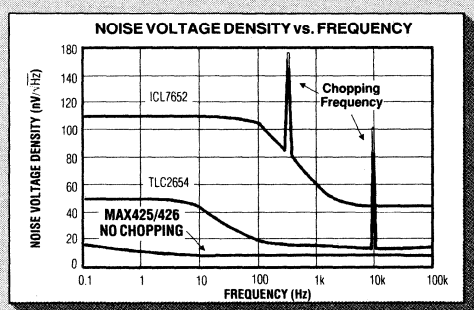
Before the MAX406, 15µA supply current was considered the state-of-the-art for a micropower op amp. Operating at only 1µA, the MAX406 has now redefined the term micropower. If batteries had an indefinite shelf-life, the MAX406 could operate up to 250,000 hours (28 years) from a 250mA-hr lithium coin cell. Drawing no more than a battery's leakage current, the MAX406 enables battery-powered systems to operate over 15 times longer. It works off a single 2.5V to 10V supply, or a dual ±1.25V to ±5V supply.

The MAX406 is unity gain stable and offers superior stability compared to other micropower CMOS op amps—it remains stable while driving capacitive loads as high as 1µF without oscillating. For high-speed applications, pin 8 can be connected to the positive supply for a 20V/ms slew rate and a 40kHz gain bandwidth (A_{VCL} ≥ 2V/V), without drawing any extra supply current.

★ FUTURE PRODUCTS ★

Lowest Noise & Drift, Highest Gain Op Amps—No Chopping

250nV$_{pp}$ Noise, 0.005µV/°C Drift, 0.5µV Offset, 190dB Gain



MAX425/426 eliminates clock ripple noise and offer a 6 to 10 times improvement in noise (0.1Hz to 10Hz) over chopper op amps.

The new MAX425 and MAX426 are the first op amps to provide the lowest noise ***and*** "zero" drift (TCV_{OS}) in an 8-pin DIP. A unique non-chopper error-correction technique virtually eliminates input offset voltage, drift, noise, and common mode errors without the drawbacks associated with chopper stabilized op amps such as external capacitors, clock ripple noise, and external filtering.

The MAX425 and MAX426 250nV$_{PP}$ (0.1Hz-10Hz) noise and 0.005µV/°C drift represent a 6-times improvement over the lowest noise chopper stabilized op amp, and 40-times lower drift than the lowest noise precision bipolar op amp. The improvement in noise alone translates to a significant increase in system accuracy and resolution.

The MAX425 is unity-gain stable. The MAX426 is stable for gains ≥ 30V/V and offers a 15MHz gain-bandwidth product, 12V/µs slew rate, and DC performance equivalent to the MAX425. Applications include weigh-scales, sensors, low frequency active filters, current-to-voltage converters, and S/H amplifiers.

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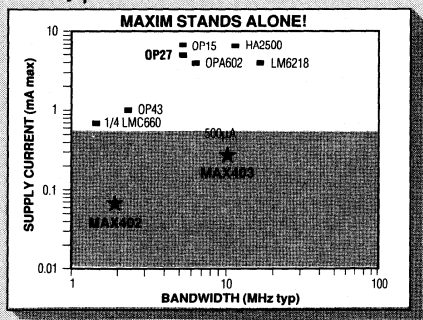
3

Fastest 10MHz Micropower Op Amps

40V/μs Slew Rate at Less Than 375μA Supply Current



Best speed/power combination: 1.7MHz at 75μA MAX402 or 10MHz at 375μA MAX403

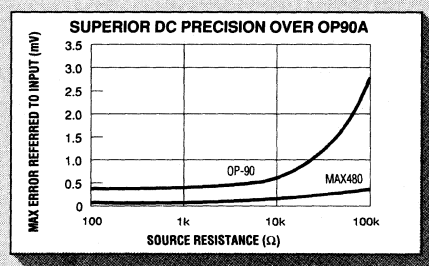
No other op amps match the new MAX402 and MAX403's combination of high-speed and micropower operation. The MAX403 guarantees a 7MHz (10MHz typ) bandwidth and a 25V/μs (40V/μs typ) slew rate from less than 375μA supply current—14 times faster than the industry standard OP27 at less than 1/10th the supply current (see graph). MAX403 power consumption is under 3.75mW at ±5V. For applications requiring even lower power, the MAX402 guarantees a 1.7MHz bandwidth and a 5V/μs slew rate while drawing less than 75μA supply current which results in a power consumption of less than 750μW at ±5V. Both op amps are unity gain stable and operate from ±3V to ±5V supplies, or a single 6V to 10V supply. Applications include low power signal processing, portable or handheld instruments, and remote sensors.

70μV Op Amp Minimizes Input Errors

Single Supply Operation From 1.6V to 36V at Only 15μA Supply Current

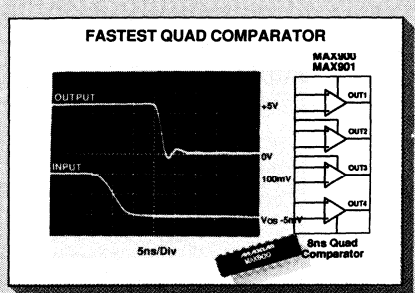
The MAX480's precision DC specifications minimize input referred errors (see graph). Guaranteed 70μV offset voltage and 1.5μV/°C drift, independent of package type or supply voltage range, represents a greater than two times improvement over the highest grade industry standard OP90A. Similarly, input bias current and offset current are improved over the OP90.

The MAX480 input and output voltage range include the negative supply rail. With single or dual supply capability ranging from +1.6V to +36V or ±0.8V to ±18V, applications include micropower voltage references, remote thermocouple conditioners, and current monitors.



MAX480 micropower op amp minimizes input errors by offering superior DC performance over the highest grade industry standard OP90A.

8ns, 18mW Comparator Family



MAX900 high-speed, lower power comparator family offers an 8ns response time while consuming only 18mW/comparator.

Fastest Low Power Comparators Operate From a Single +5V Supply

Maxim's growing MAX900 family of high-speed comparators offer single, dual, and quad devices with unparalleled performance. No other comparators offer the combination of an 8ns response time while drawing only 3.6mA (18mW) per comparator from a +5V supply. And since many low-power applications operate from a single supply, the MAX900 family's input voltage range extends all the way to ground to provide a wide common mode input voltage range.

Whether it's a 1.7ns ECL or 9ns TTL output comparator with industry standard pinouts, Maxim provides the high-speed comparator solution for your application.

Part Number	V_{OS} (mV) max	TCV_{OS} (µV/°C) max	I_{BIAS} (nA) max	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA) max	Features	Price† 1000-up ($)
MAX400	10 - 15µV	0.3	2	0.4	±3 to ±18	4	Ultra-low V_{OS} & drift non-chopper stabilized	5.16
MAX402	2	25	5	2	±5	75µA	High-speed, 7V/µs slew rate, micropower	1.98
MAX403	2	33	25	10	±5	375µA	High-speed, 40V/µs slew rate, micropower	2.75
MAX406	0.5 - 2.0	10	10pA	0.008-0.040	+2.5 to +10	1.2µA	Lowest-power, single supply output swings rail-to-rail	2.54
MAX408/28/48	6 - 12	15 - 20	1.1µA	100 ($A_V \geq 3$)	±5	10/amp.	Single/dual/quad high-speed, high output current	3.02/4.06/6.74
MAX420/422	5 - 10µV	0.05	0.03 - 0.10	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 - 10µV	0.05	0.03 - 0.10	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/4.57
MAX425/426	5µV	0.05	10pA	0.35 - 12	±5	1.4	Lowest noise & drift, superior non-chopper error correction, no clock ripple noise	††
MAX430/432	5µV	0.05	0.1	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX480	70µV	1.5	3	0.02	±0.8 to ±18	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
ICL7611	2 - 15	10 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current	1.58
ICL7612	5 - 15	15 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current, CMVR > negative rail	1.81
ICL7614	2 - 15	15 - 25	0.05	0.48*	±1.0 to ±8	0.25	External compensation	0.95
ICL7616	2 - 15	15 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current, CMVR > negative rail	1.62
ICL7621/7622	5 - 15	15 - 25	0.05	0.48	±1.0 to ±8	0.25	Dual low I_{BIAS} & I_{OS}	1.55/1.48
ICL7631/7632	5 - 20	15 - 30	0.05	0.044 - 1.4	±1.0 to ±8	0.022 - 2.5	Triple op amp, programmable quiescent current–ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 - 25	15 - 30	0.05	0.044 - 1.4	±1.0 to ±8	0.015 - 2.5	Quad op amp	1.70/1.91
ICL7650	5 - 10µV	0.05 - 0.10	0.01 - 0.02	2	±5	2	Industry-standard chopper stabilized	2.39
ICL7652	5 - 10µV	0.05	0.03	0.45	±5	2	Low noise industry-standard chopper stabilized	3.06

Notes:
* External 39pF compensation capacitor added.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

Op Amps (continued)

Part Number	V_{OS} (μV)	TCV_{OS} (μV/°C) max	I_{BIAS} (nA) max	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA) max	Features	Price† 1000-up ($)
LT1001	15 - 60	0.6 - 1	2 - 4	0.8	±3 to ±18	2	Industry-standard precision	1.75
LT1028	40 - 80	0.8 - 1	90 - 180	75 (Av > 2)	±4 to ±18	9.5 - 10.5	Lowest noise, high-speed	4.21
OP07	25 - 150	0.6 - 2.5	2 - 12	0.6	±3 to ±18	4	Industry-standard precision	0.97
OP27	25 - 100	0.6 - 1.8	40 - 80	8	±3 to ±18	4.6 - 5.6	Industry-standard low noise	††
OP37	25 - 100	0.6 - 1.8	40 - 80	63 (Av ≥ 5)	±3 to ±18	4.6 - 5.6	Industry-standard low noise	††
OP90	150 - 450	2 - 5	15 - 25	0.020	±0.8 to ±18	15 - 20μA	Industry-standard micropower	1.65

High-Speed Comparators

Part Number	# Comps	Logic	Latched Outputs	Supply Current (mA) max	Tpd (ns) typ	Features	Price† 1000-up ($)
MAX900	4	TTL	YES	33	8.0	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, Internal pull-up resistors	7.01
MAX901	4	TTL	NO	33	8.0	MAX900 without output latch	5.98
MAX902	2	TTL	YES	17	8.0	Dual MAX900	††
MAX903	1	TTL	YES	8.5	8.0	Single MAX900	††
MAX910	1	TTL	YES	60	5.0	High-speed TTL-compatible comparator with 8-bit digitally programmable input voltage threshold and on-board reference	††
MAX911	1	ECL	YES	62	2.0	MAX910 with differential ECL outputs	††
MAX9685	1	ECL	YES	54	1.3	Higher speed industry-standard	3.38
MAX9686	1	TTL	YES	45	6.0	Higher speed industry-standard	2.31
MAX9687	2	ECL	YES	114	1.4	Higher speed industry-standard	5.12
MAX9690	1	ECL	NO	54	1.3	High speed, 8-lead PDIP, SO	3.29
MAX9698	2	TTL	YES	90	6.0	Higher speed industry-standard	3.92

Notes:
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Video Products

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Vos (mV) max	Output Current (mA) max	Supply Voltage (V)	IBIAS (nA) max	Features	Price† 1000-up ($)
VIDEO AMPLIFIERS								
MAX408/28/48	100(Av ≥ 3)	90	6 - 12	50/amp	±5	1.1µA	Single, dual, quad op amps, high output drive	3.02/4.06/6.74
MAX452	50	300	5	14	±5	10	Unity gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	5	15	±5	1	Dual, unity gain stable, drives 75Ω coax cable	4.45
VIDEO BUFFERS								
MAX405	180	650	4	60	±5	2µA	0.99V/V gain guaranteed over temp, 0.01°/0.03% diff phase/gain	4.25
MAX460	140	1500	5 - 10	100	±15	0.05 - 0.1	FET input, EL2005, LH0033 upgrade	19.78
LH0033	100	1400 - 1500	5 - 20	100	±15	0.1 - 0.5	FET input, improved industry-standard	13.67
LH0063/BB3553	300	2000	25 - 50	200	±15	0.2 - 0.5	FET input, industry-standard	23.51/24.99
VIDEO MULTIPLEXER/AMPLIFIER								
MAX453	50	300	5	14	±5	10	Video amplifier with 2-channel video mux	3.94
MAX454	50	300	5	14	±5	10	Video amplifier with 4-channel video mux	5.25
MAX455	50	300	5	14	±5	10	Video amplifier with 8-channel video mux	8.75

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Vos (mV) max	OFF Isolation (dB at 5MHz)	Crosstalk (dB at 5MHz)	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCH							
MAX456	35	250	5	80	70	8x8 crosspoint switch array with 8 output buffers, three-state capability	22.09

Notes:
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†† Future products – contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

Getting High Performance From Low Power

Low Noise In Precision Measurements

Precision Amplifiers

The term "precision" in analog signal measurement generally applies to circuits that are optimized for accurate amplification or manipulation of signals. But manufacturers of op amps and other ICs differ on what constitutes precision, and their products lay claim to the term with varying degrees of success.

A precision amplifier must perform well in several respects: low offset voltage, large open-loop gain, and good power-supply and common-mode rejection. Low input-bias and input-offset currents are also important in applications where the input signal originates from a large source impedance. And to maintain the precision, these parameters must exhibit minimal drift over time and temperature.

Noise as a Precision Spec

Noise, though a less frequently scrutinized parameter, is always critical in achieving high resolution and accuracy. An IC's noise characteristics may be an obstacle even in the presence of low bandwidth and extensive filtering.

Three types of noise can contribute error in a measurement application:

1) Transmitted noise that is received with the input signal. If you have no control over the signal source, this noise can be reduced only by filtering, or in some cases, by synchronous detection.
2) Interference noise (60Hz pickup, for example) enters the circuit through magnetic coupling or power-supply and ground connections. It can be minimized by careful design and layout practices, and sometimes by filtering.
3) Intrinsic noise, generated within an IC or other component, is best minimized through careful component selection.

Wideband vs. 1/f Noise

There are two types of low noise op amps: Those exhibiting low noise at low frequency, and a much larger category—those that exhibit low wideband noise. The latter type finds application in audio, video, and other AC-coupled or high-frequency systems.

The "1/f corner frequency", at which the graph of noise energy (density) vs. frequency changes slope, is a key characteristic separating low-noise DC amplifiers from wideband types. Below this corner, the noise density of conventional op amps increases at a rate inversely proportional to frequency. At very low frequencies, the op amp noise is essentially indistinguishable from V_{OS} drift.

Excessive 1/f noise is the circuit designer's biggest concern in high gain and low frequency applications. It often appears as random changes in the least significant bit of a display or an A/D converter; hence the term "flicker noise", often used in place of 1/f noise.

Low 1/f noise is crucial in achieving accurate, high-resolution DC measurements. Filtering 1/f noise is virtually impossible because the noise increases with decreasing frequency and displays most of its energy below 1Hz. In addition, a lowpass filter for this purpose would introduce intolerably long delays in the system response time.

Best Amplifiers for 1/f Noise

Because circuit-design techniques are largely ineffective in reducing 1/f noise, you must limit this aberration by selecting a low-noise amplifier. Clock-stabilized types, for example, correct for input offset, drift, and random low-frequency variations (1/f noise). Figure 1 test circuit enables measurement of total noise in the bands 0.1 to 1Hz and 0.1 to 10Hz.

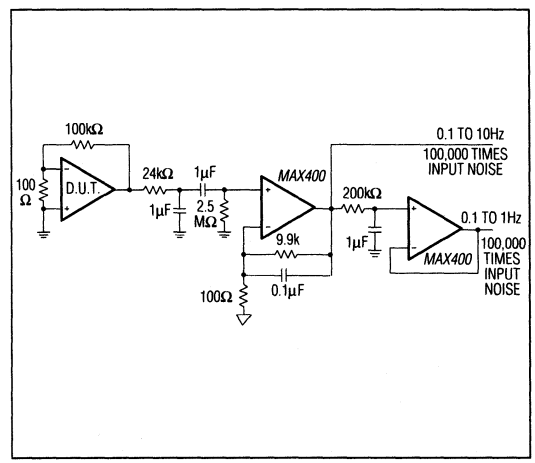

Figure 1. Op Amp 1/f Noise Test Circuit

For three such amplifiers operating with a 100Ω source impedance: The ICL7652 (Figure 2) was among the first monolithic op amps to apply the clock-stabilization (chopper-stabilized) technique, and was further refined in the TLC2654 (Figure 3). The MAX425 and MAX426, however, achieve dramatic further reductions in low-frequency noise through careful layout and unique

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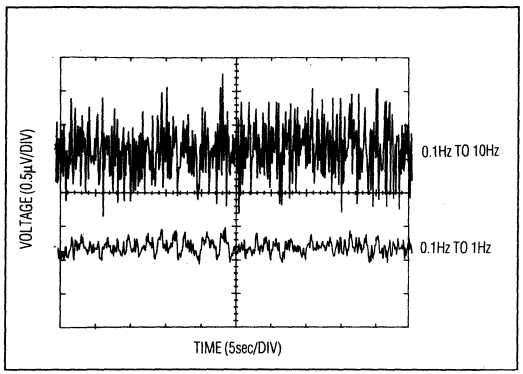

Figure 2. ICL7652 Noise in 10Hz and 1Hz Bandwidth

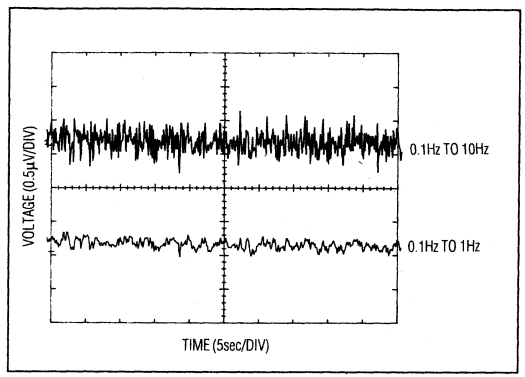

Figure 3. TLC2654 Noise in 10Hz and 1Hz Bandwidth

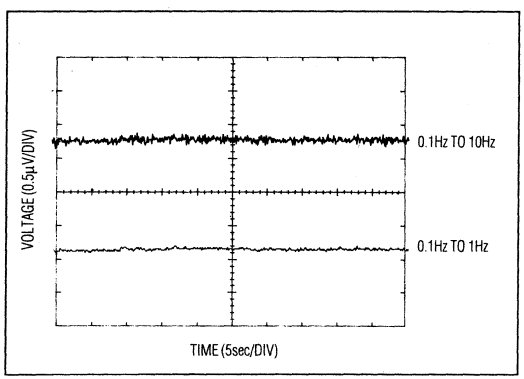

Figure 4. MAX425/MAX426 Noise in 10Hz and 1Hz Bandwidth

switched-input stages (Figure 4). (See *A "Switching" Op Amp*).

Voltage density for the three switching op amps, unlike that of conventional op amps, levels off below 10Hz instead of rising.

Current Noise

Current noise is an issue if the input signal's source resistance is sufficiently high. For some op amps, the acceptable level of source resistance is quite low. Maxim's LT1028, for example, whose wideband voltage-noise density ($<1nV/\sqrt{Hz}$) is the lowest available in a monolithic op amp, loses its noise advantage to other amplifiers (such as the MAX400) if the source resistance exceeds 1kΩ (Figure 6). The LT1028 achieves low voltage noise at the expense of a high input bias current (25nA); it must therefore operate with minimum values of external resistance to retain its low-noise advantage.

Current noise in high-gain, precision DC applications is rarely a concern because source resistances are usually low (strain gauges, for instance, measure 350Ω; thermocouples, 10Ω). A major exception to this rule is the photodiode current-to-voltage amplifier, which provides a voltage gain of one with a current gain of 10^6 or more.

Current noise in CMOS amplifiers is low (compared with bipolar amplifiers) because CMOS input bias currents are extremely low (picoamps). But this current-noise advantage is often wasted. The source impedance in wideband CMOS amplifier circuits is usually low, and the alternative bipolar amplifiers (LT1028 and MAX400, for example) offer significantly lower voltage noise.

The limitations of all components should be considered in a low-noise design. Select high quality metal-film or wirewound resistors and specify minimal resistance values. To minimize wideband noise, the system bandwidth should be no greater than necessary to avoid distortion at the highest signal frequency of interest.

What Happened to Chopper Op Amps?

Chopper-stabilized op amps have offered the highest performance available until recently. Chopper-stabilized op amps actually consist of two amplifiers: The main signal amplifier and a nulling amplifier, which zeroes the main amplifier once per clock cycle. Two capacitors store the autozero correction voltages during different periods of the amplifier's

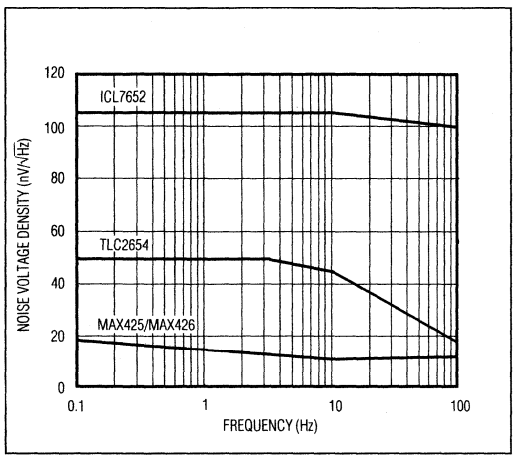

Figure 5. Noise Voltage Density vs. Frequency

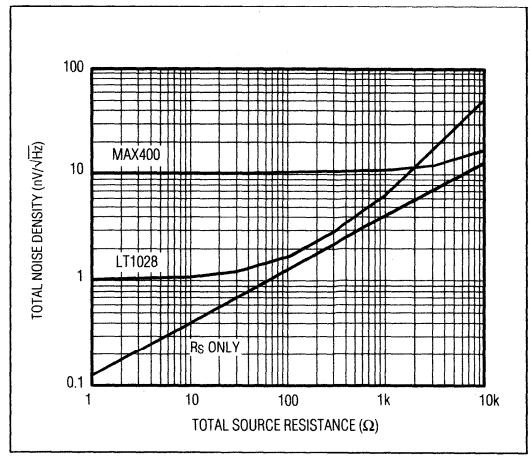

Figure 6. LT1028 and MAX400 Total Noise Density at 10Hz vs. Source Resistance

operating cycle. This almost-continuous nulling action virtually eliminates the effects of V_{OS} drift, common-mode voltage, and power-supply variations. It also reduces low-frequency and 1/f noise.

Chopper-stabilized op amps also have drawbacks:

1) The autozero information resides on capacitors, whose leakage degrades the amplifier's drift performance.
2) The chopper amplifier's autozero loop is slow to recover following an input overload.
3) Choppers generate switching noise at the clock frequency.
4) The chopper amplifier's output stage has an asymmetric drive capability.
5) Chopper amplifiers exhibit excessive phase error due to intermodulation distortion when the input signal frequency equals the switching clock frequency.

The MAX425/426 precision op amps, unlike chopper-stabilized types, have internal D/A converters for autozeroing. The error correction information is stored digitally without any loss of information from leakages common to chopper-stabilized op amps. With no need to restore charge on a capacitor, the autozero operation can be performed less often. Because there is no discharge of autozero capacitors, the digital autozero scheme also allows the MAX425/426 to recover from input overloads almost immediately. Noise voltage density at the 300Hz clock frequency is only about $17nV/\sqrt{Hz}$.

The MAX425/426 output stage is a high-speed, low-gain amplifier with 300Ω output impedance and a fixed gain of 10dB. Low output impedance makes these amplifiers relatively insensitive to load changes. And with ±5V power supplies, the amplifiers can drive a 10kΩ load rail-to-rail, or a 2kΩ load to ±4V. Unlike early chopper-stabilized amplifiers, there are no separate signal paths for AC and DC signals in the MAX425/MAX426, so phase error due to intermodulation distortion is nonexistent.

Micropower Op Amps and Their Application Requirements

Typical Output Loads

A host of parameters come to bear when an op amp operates in a low-power, low-voltage application. Not all can be picked from the spec table in a data sheet.

To achieve very low supply currents, an amplifier usually compromises on characteristics that are taken for granted by designers familiar with more conventional op amps. One such characteristic is the ability to drive low-valued resistive loads; another is the ability to remain stable while driving a

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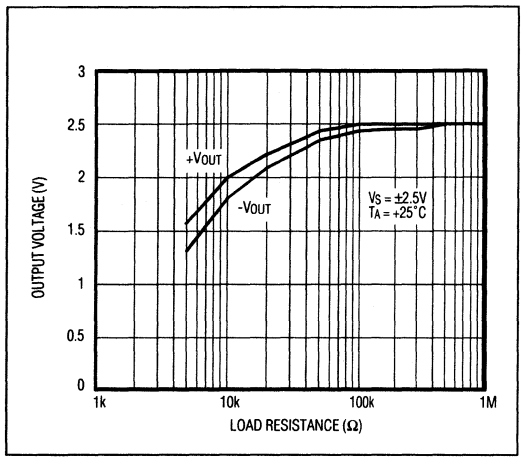


Figure 7. MAX406 Output Swing (Unity Gain Mode) vs. Load Resistance

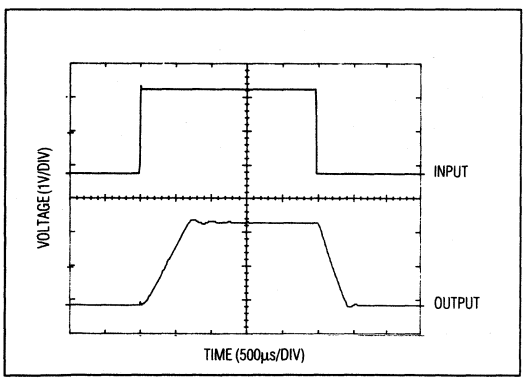


Figure 8. MAX406 Driving 1MΩ//100pF

capacitive load. The latter is especially challenging as the supply current approaches 1µA.

The MAX406 ultra-low-power op amp, capable of driving a wide range of resistive and capacitive loads, draws less than 1.2µA from ±2.5V supplies. Its output swing vs. resistive load under these conditions (Figure 7) shows that the device successfully drives load resistances well below the 1MΩ guaranteed in the data sheet.

Capacitive-load capability is also impressive—for a low-power op amp—when driving a ±1.25V square wave into a load of 1MΩ||1000pF (Figure 8).

Usable Signal Range

In designs where analog circuitry must operate at low power or low supply voltage (or both), the operating signal range receives more attention than most other parameters. With limited dynamics, you must utilize every bit of the available operating range. An unregulated battery voltage compounds the problem because the signal range shrinks as the voltage falls.

The operating signal range is even more important in single-supply systems where signal ground coincides with the most negative supply voltage. Of particular interest is the amplifier's response to signals that swing all the way to ground, especially in battery-powered systems.

Operating signal range vs. load resistance for the MAX406 at unity gain (Figure 9) differs slightly compared to a gain of two (Figure 10). As a sidenote, the signal range is the same in high-speed mode as it is in unity-gain mode at a gain of two. The amplifier operates on a single 5V supply in these figures, and the load connects between ground and the amplifier's output. Output swing decreases with load resistance as you can see, but it includes ground in all cases. The usable output range in these graphs is defined as that for which the output error is less than the amplifier's V_{OS}.

Single-Supply Considerations

When choosing op amps for use in a single-supply system, pay close attention to the input-voltage range and the output voltage swing—specs that are much less important in a dual-supply system. The input range must often extend down to ground, the most negative level in a single-supply system, to insure that low-level signals near zero volts are not "lost". The output swing, with respect to ground, is also important for the same reason.

In addition, an op amp's input and output range that extends close to the positive supply will maximize the operating signal range—a greater concern in 5V systems than 12V or 15V systems. Amplifier noise, offset, and drift are also more troublesome in today's low-voltage (5V or less) single-supply systems because they, in addition to the voltage swing performance, limit the system's dynamic range.

Power supply current is also an issue in the selection of IC components because most single-supply systems are also portable and battery powered. Accordingly, the operating and standby currents of ICs are among the most important specs in these systems.

Op amp users must understand that noise and grounding problems become more pressing as the supply voltage and signal ranges decrease. Quality of the pc-board

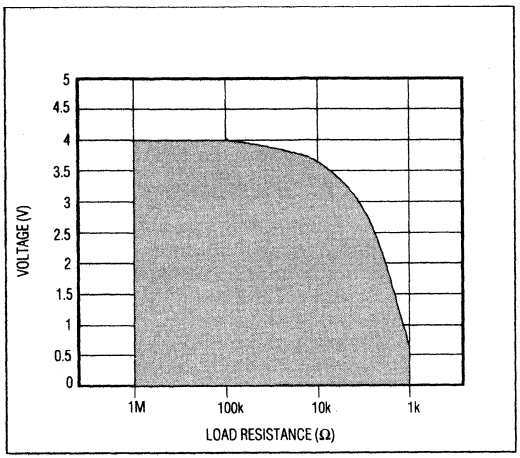


Figure 9. MAX406 Unity Gain Buffer Output Range

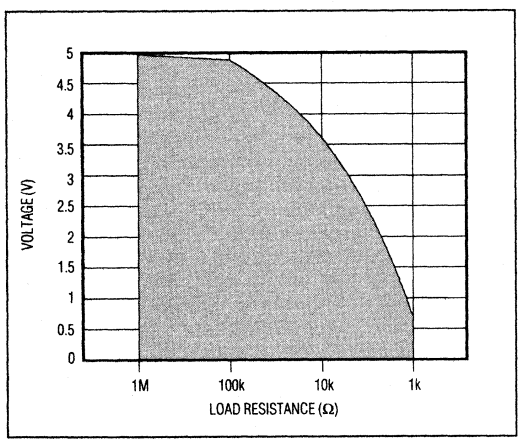


Figure 10. MAX406 Output Voltage Range (A_{VCL} = +2)

ground is much more important in a single-supply system because the signal ground is identical with the power return to the negative rail. In a split-supply system, most supply current flows (for example) from 15V to -15V. "Ground" acts as a reference but carries little current; the ground potential therefore remains unaffected by supply current to the components. The negative rail's separation from ground helps reduce noise, oscillation, and interference. Because single-supply systems lack this advantage over split supplies, they require a more careful layout.

Benefit of Micropower CMOS

The extremely low input bias current of CMOS op amps is an advantage if the input signal's source impedance is large; the low bias current produces minimal voltage errors across the resistance. In most micropower applications, the source impedance is very large (typically 1MΩ to 10MΩ) in order to keep power consumption as low as possible. The MAX406's 0.1pA input bias current virtually eliminates any unwanted currents that would be multiplied by the source impedance to produce an error voltage. For example, 0.1pA multiplied by a 5MΩ source impedance produces an error of only 50μV.

Low-Power Light-Detector Alarm Circuit

In photodiode current-to-voltage applications where very small current changes must be resolved (several nanoamps), the op amp must have a significantly lower input bias current than the magnitude of the current being measured. The battery-powered photodiode circuit shown in Figure 11 sounds an alarm when it detects light. If the door to a secured area is opened, for example, light triggers the alarm and it remains on even if the door should close, until the reset is actuated. The circuit requires an op amp with low supply current and fairly low bias current, and the MAX406 fits that description—its supply current is 1.2μA max and its bias current is typically less than 0.1pA.

The MAX406 operates as a comparator and as a latch. Photocurrent resulting from light on the photodiode flows through the parallel combination of R_2 and R_3, adding

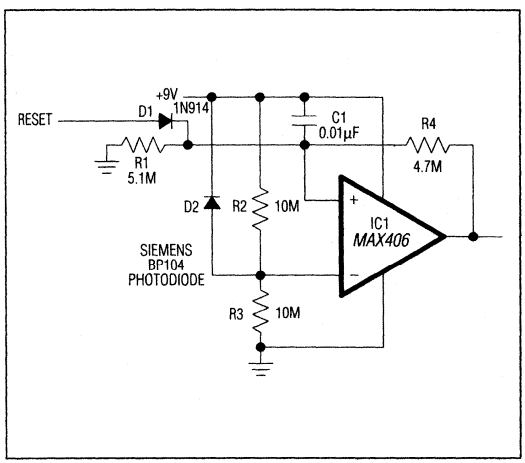


Figure 11. Low-Power Light Detector Alarm Circuit

Getting High Performance From Low Power

voltage to the 4.5V already present at the op amp's inverting input. When this voltage exceeds the non-inverting level (4.7V) the output goes low and pulls the non-inverting voltage to 0V, well below that of the inverting input. The output remains low when light is removed; otherwise the alarm would cease. To reset the circuit, raise the anode of D_1 to at least 5.2V.

A similar connection that provides a low output level in the inactive state is not recommended because the MAX406 draws higher supply current (30µA) when overdriven to the negative rail.

Capacitor C_1 assures that voltage on the non-inverting input exceeds that of the inverting input when you apply voltage to the circuit. A fast rise in the supply voltage at turn-on may call for a larger capacitor. Thus, the capacitor assures that the output does not go low (and stay there) during power-up with no light present.

A 4-Channel, 1.3A Sample-and-Hold

Sample/hold circuits often require op amps with low bias current such as the battery-powered application shown in Figure 12. In this case—a system that samples four transducer signals for the input of an A/D converter—the op amp and the analog switch both should have low bias current and low supply current.

Supply current to the analog switch should be comparable to that of the op amp (1.0µA typical). But the switch shown draws 150µA with ±15V supplies. Though lower when operating with a 9V battery, this current is not in the required range unless a simple step is taken: Digital-logic levels applied to the switch-select inputs must swing to the supply rails—from near ground to near 9V in this case. Driving the digital inputs in that manner turns off current-hungry level translators in the switches, thereby lowering the IC's supply current to only 100pA (typical).

Because the op amp's input bias current is typically less than 0.1pA and the switch leakage current is typically 0.1pA, the hold-capacitor value can be relatively small, reducing the acquisition time while minimizing droop. The worst-case current (0.2pA), drawn from a 100pF hold capacitor, causes a droop of only 2µV over a hold time of 1msec. Hold capacitors with dielectrics of polypropylene or polystyrene are recommended for low dielectric-absorption error as well as low leakage.

Low-Frequency Applications

Op amps with low input bias current are useful in low-frequency applications such as filters, oscillators, and integrators. The low bias current allows use of higher-valued resistors, which in turn enables the use of smaller and therefore less expensive capacitors.

A "Switching" Op Amp

The MAX425/426 op amps boast precision specs that attribute largely to the unique input switching stage. By swapping inputs and outputs at approximately 300Hz, this stage nulls internal errors such as thermal drift, input offset, low-frequency (1/f) noise, and power-supply sensitivities. Common-mode errors that vary slowly with respect to 300Hz are dramatically reduced as well.

Because low-frequency noise appears to the correction circuitry as a slowly varying offset, this noise is removed (about $300nV/\sqrt{Hz}$ at 1Hz before switching) in the same way as offset. The amplifier's primary noise contribution, therefore, is wideband noise at the switching frequency. After demodulation, this wideband noise appears as low-frequency output noise—typically $17nV/\sqrt{Hz}$ at 300Hz for the MAX425/426. Wideband noise in the 1kHz to 100kHz bandwidth range is typically $2.5\mu V_{rms}$, which corresponds to a noise voltage density of $8nV/\sqrt{Hz}$ throughout the band.

The switching amplifier's differential input stage swaps its input and output connections repeatedly, at the clock frequency. The example of Figure 13a assumes a 1mV offset (mismatch) between MOSFETs P1 and P2. This offset generates an output of:

$$V_{OUT} = 100(V_{IN}-1mV) = 100V_{IN}-100mV.$$

When the inputs and outputs of P1 and P2 are interchanged (Figure 13b), the output voltage becomes $100V_{IN}+100mV$. Switching the connections thus changes the polarity of the offset but not that of the input signal. For a 50% duty cycle, the output averages to 100mV while the offset averages to zero.

The amplifier output then consists of the desired signal plus a small superimposed square wave whose amplitude is the internal offset voltage. This amplitude in the MAX425/426 is reduced by digital autozeroing to less than 1µV.

Reference

"Grounding and shielding techniques in instrumentation" by Ralph Morrison, Wiley and Sons, is thorough, practical, and strongly recommended as a readable and realistic treatment of this subject.

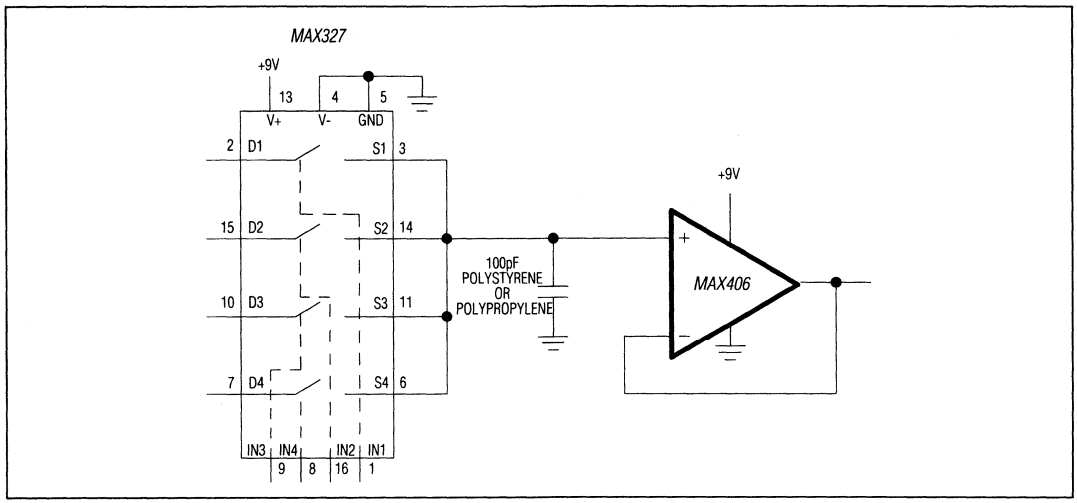


Figure 12. Four Channel, 1.3µA Sample-and-Hold

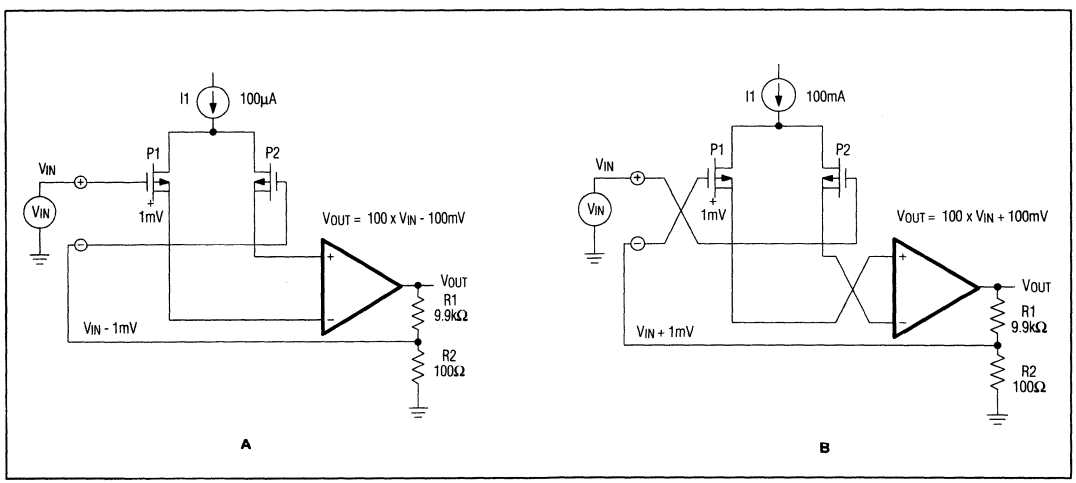


Figure 13. Switching-Amplifier Operation. In Figure A, offset voltage appears as -100mV at the output of the amplifier; in Figure B, it is +100mV. If the duty cycle of each state is 50%, the offset voltage at the output averages zero.

19-3786; Rev 0; 6/91

MAXIM

High-Speed, Micropower Op Amps

General Description

The MAX402/MAX403 high-speed, micropower op amps are fabricated with Maxim's high-frequency complementary bipolar process. These devices feature a combination of high-speed performance and low-power operation that offers significant improvement over other available op amps.

The MAX402 guarantees a 5V/µs slew rate and 1.4MHz bandwidth while drawing only 75µA of supply current. For applications requiring increased speed, the MAX403 guarantees a 25V/µs slew rate and 7MHz bandwidth while drawing a maximum supply current of 375µA. These micropower op amps have excellent load-driving capability: ±3.6V into a 10kΩ load for both amplifiers, and ±3.3V into a 2kΩ load for the MAX403. Both op amps are unity-gain stable and operate from ±3V to ±5V supplies, or a single supply from +6V to +10V.

The combination of high speed and low power makes the MAX402/MAX403 ideal for high-speed, battery-powered applications.

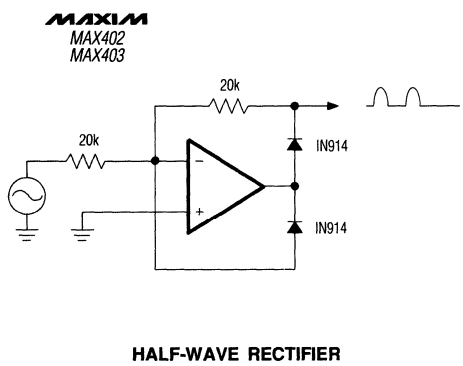
Applications

Low-Power Signal Processing

Portable Instruments

Remote Sensors

Typical Application Circuit



HALF-WAVE RECTIFIER

Features

MAX402

- **1.4MHz Min Unity Gain Bandwidth**
- **5V/µs Min Slew Rate**
- **75µA Max Supply Current**

MAX403

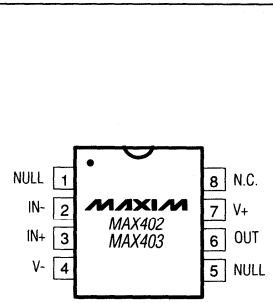
- **7MHz Min Unity Gain Bandwidth**
- **25V/µs Min Slew Rate**
- **375µA Max Supply Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX402CPA	0°C to +70°C	8 Plastic DIP
MAX402CSA	0°C to +70°C	8 SO
MAX402C/D	0°C to +70°C	Dice*
MAX402EPA	-40°C to +85°C	8 Plastic DIP
MAX402ESA	-40°C to +85°C	8 SO
MAX403CPA	0°C to +70°C	8 Plastic DIP
MAX403CSA	0°C to +70°C	8 SO
MAX403C/D	0°C to +70°C	Dice*
MAX403EPA	-40°C to +85°C	8 Plastic DIP
MAX403ESA	-40°C to +85°C	8 SO
MAX403MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications and military temperature range availability.*

Pin Configuration



DIP/SO

High-Speed, Micropower Op Amps

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ to V-) 12V
Input Voltage Range ..... (V+ +0.3V) to (V- - 0.3V)
Differential Input Voltage ..... V+ to V-
Short-Circuit Current Duration ..... Indefinite
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +25°C)
8-Pin Plastic DIP 375mW
8-Pin CERDIP 500mW
8-Pin SO 471mW

Operating Temperature Ranges:
MAX40_C_ _ ..... 0°C to +70°C
MAX40_E_ _ ..... -40°C to +85°C
MAX403MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to packaged parts only, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402			MAX403			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.5	2		0.5	2	mV
Offset Voltage Tempco $\Delta V_{OS}/\Delta T$	TCV_{OS}	$T_A = T_{MIN}$ to T_{MAX}		25			25		µV/°C
Input Bias Current	I_B			±2	±5		±10	±25	nA
Input Voltage Range	IVR		±3.5	±3.8		±3.5	±3.8		V
Differential Input Resistance	R_{IN} (DIFF)			90			18		MΩ
Common-Mode Input Resisitance	R_{IN} (CM)			1			1		GΩ
Input Noise Voltage Density	e_n	f_O = 10Hz		43			33		nV/√Hz
		f_O = 1000Hz		26			14		
Input Noise Current Density	i_n	f_O = 10Hz		0.06			0.25		pA/√Hz
		f_O = 1000Hz		0.03			0.07		
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	75	95		66	80		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	56	65		60	70		dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	68	75			80		dB
		R_L = 2kΩ				68	75		
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.6	±3.9		±3.6	±3.9		V
		R_L = 2kΩ				±3.3	±3.6		
Short-Circuit Output Current	I_{SC}			3			5		mA
Slew Rate	SR	10kΩ | | 20pF load	5	7		25	40		V/µs
Gain Bandwidth	GBW	10kΩ | | 20pF load	1.4	2		7	10		MHz
Quiescent Current	I_Q		40	50	75	200	250	375	µA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402C_A			MAX403C_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				4			4	mV
Input Bias Current	I_B				±10			±50	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	70			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	54			60			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	66						dB
		R_L = 2kΩ				66			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.5			±3.5			V
		R_L = 2kΩ				±3.2			
Slew Rate	SR	10kΩ I I 20pF load	4.5			22.5			V/µs
Gain Bandwidth	GBW	10kΩ I I 20pF load	1.3			7			MHz
Quiescent Current	I_Q		35		90	175		450	µA

ELECTRICAL CHARACTERISTICS

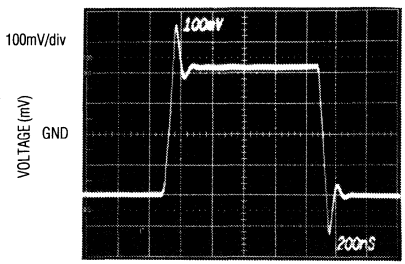
(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402E_A			MAX403E_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				5			5	mV
Input Bias Current	I_B				±20			±100	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	68			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	52			58			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	63						dB
		R_L = 2kΩ				63			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.4			±3.4			V
		R_L = 2kΩ				±3.0			
Slew Rate	SR	10kΩ I I 20pF load	4.0			20			V/µs
Gain Bandwidth	GBW	10kΩ I I 20pF load	1.2			6			MHz
Quiescent Current	I_Q		30		95	150		475	µA

High-Speed, Micropower Op Amps

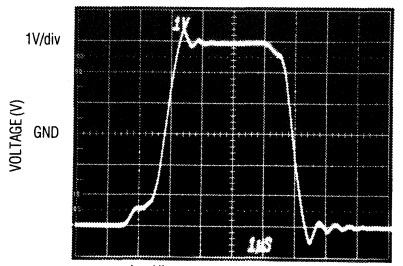
Typical Operating Characteristics

MAX402 SMALL-SIGNAL TRANSIENT RESPONSE



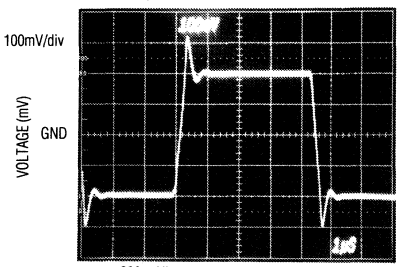
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 10kΩ//10pF

MAX402 LARGE-SIGNAL TRANSIENT RESPONSE



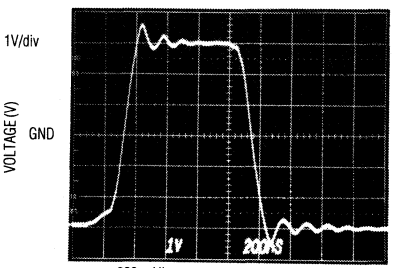
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 10kΩ//100pF

MAX403 SMALL-SIGNAL TRANSIENT RESPONSE



NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 2kΩ//10pF

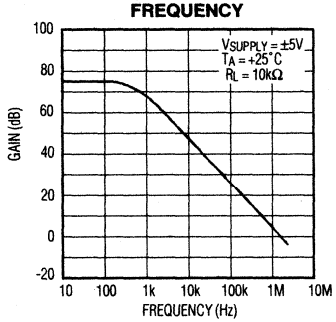
MAX403 LARGE-SIGNAL TRANSIENT RESPONSE



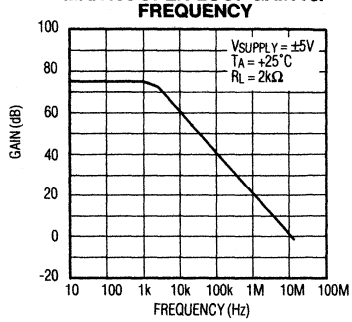
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 2kΩ//100pF

Typical Operating Characteristics (continued)

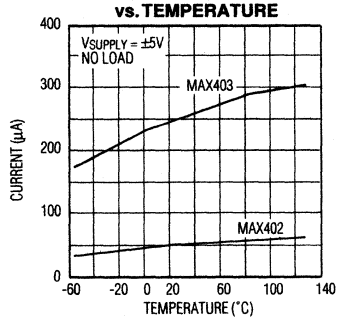
MAX402 OPEN-LOOP GAIN vs. FREQUENCY



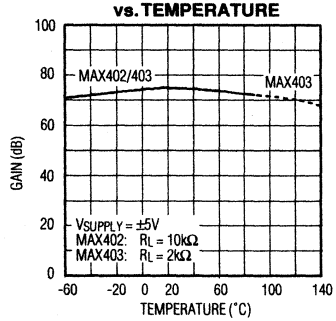
MAX403 OPEN-LOOP GAIN vs. FREQUENCY



SUPPLY CURRENT vs. TEMPERATURE



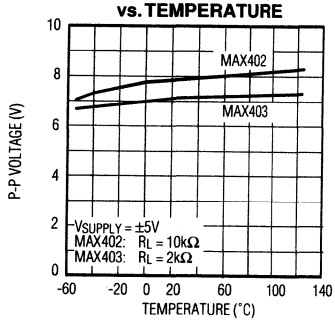
OPEN-LOOP GAIN vs. TEMPERATURE



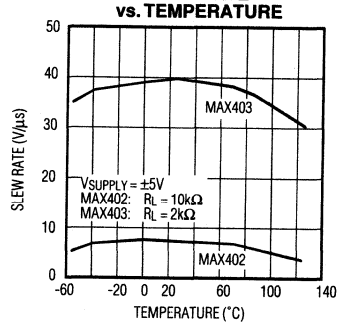
High-Speed, Micropower Op Amps

Typical Operating Characteristics (continued)

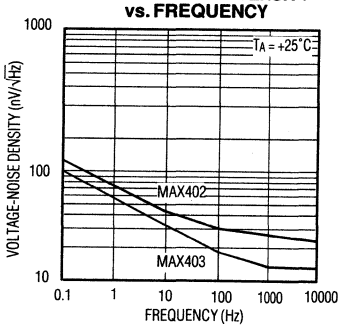
PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs. TEMPERATURE



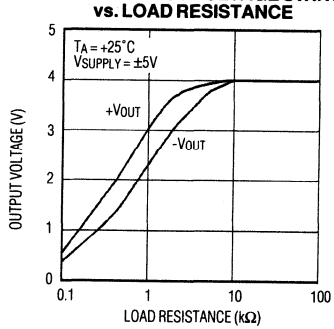
SLEW RATE vs. TEMPERATURE



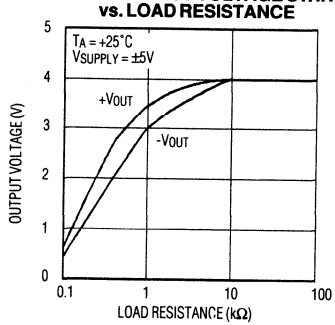
VOLTAGE-NOISE DENSITY vs. FREQUENCY



MAX402 OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



MAX403 OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



Pin Description

PIN	NAME	FUNCTION
1, 5	NULL	Offset-Voltage Adjustment
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V-	Negative Power Supply
6	OUT	Amplifier Signal Output
7	V+	Positive Power Supply
8	N.C.	No Connect

Applications Information

Input Offset-Voltage Adjustment

Pins 1 and 5 (NULL) null the input offset voltage. To adjust amplifier offset, connect a potentiometer between the two NULL pins with the wiper connected to V-, as shown in Figure 1. A 10kΩ potentiometer should be used with the MAX402, while a 2kΩ potentiometer is recommended with the MAX403. The offset voltage can be adjusted approximately ±6mV with these trim potentiometers.

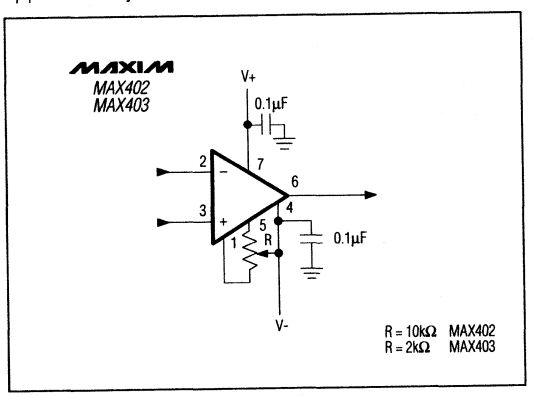


Figure 1. Offset-Voltage Adjustment

Operating Supply Voltage

The MAX402/MAX403 are specified with ±5V power supplies, but also operate with dual supplies down to ±3V or single supplies ranging from +6V to +10V. The input voltage range for normal amplifier operation is between V- + 1.5V and V+ -1.5V. For example, with a single +6V supply, the common-mode input voltage ranges between +1.5V and +4.5V.

Layout and Bypassing

The MAX402/MAX403 power-supply inputs should be bypassed with 0.1µF ceramic capacitors positioned as close to the power-supply pins as possible. To obtain maximum performance, a ground plane should be used. This is especially important for high-frequency applications. Minimize lead lengths in connections from the power-supply bypass capacitors to ground to further reduce inductance. Connections to the amplifier's input terminals should be as short and direct as possible, with a minimum of inductance.

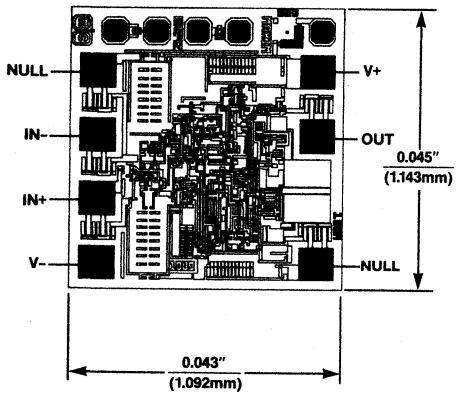
Overload Conditions

The MAX402/MAX403 inputs withstand differential voltages equal to the power-supply rails, without requiring external clamp diodes or input current-limiting resistors. Schottky diodes, used internally throughout the devices, prevent saturation of the internal transistors and allow the amplifiers to recover quickly from overload conditions.

The output stages of the MAX402/MAX403 employ a current-limit circuit that prevents damage to the amplifier in the event of a fault condition. The output may be shorted to either power supply or ground for an indefinite time without damage.

High-Speed, Micropower Op Amps

Chip Topography



Ultra-Low Power CMOS Operational Amplifier

General Description

The MAX406 is a low-voltage, micropower, precision op amp designed for battery-operated systems. It features a 1µA quiescent current that is relatively constant over the entire supply range in both unity-gain stable and high-speed modes of operation. This represents a significant improvement in supply current over industry-standard micropower op amps. A unique design technique allows the device to operate at ultra-low quiescent current while maintaining linearity under loaded conditions. The output is capable of sourcing 2mA when powered by a 9V battery and driving smaller loads from a 3V battery. The MAX406 common-mode input-voltage range extends from the negative supply rail to within 1.1V of the positive supply, and the output stage swings rail-to-rail. The MAX406 maintains good DC characteristics, minimizing the input referred errors.

The MAX406 has two modes of operation: unity-gain stable mode and high-speed mode. When BW (pin 8) is left floating or connected to V-, the amplifier is in the unity-gain stable mode with a 5V/ms typical slew rate and a gain-bandwidth of 8kHz. Connecting BW to the positive rail puts the MAX406 into the high-speed (uncompensated) mode with a 20V/ms typical slew rate and a 40kHz gain-bandwidth ($A_{VCL} \geq 2V/V$).

Applications

Battery-Powered Systems
Medical Instruments
Electrometer Amplifiers
Intrinsically Safe Systems
Photodiode Pre-Amps
pH Meters

Features

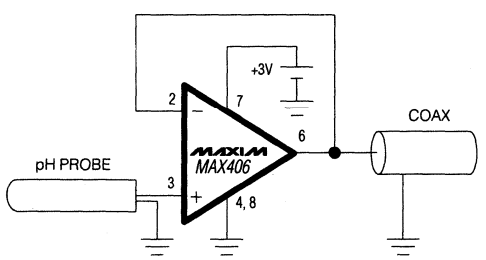
- **1.2µA Max Quiescent Current**
- **+2.5V to +10V Supply Range**
- **0.5mV Max Offset Voltage (MAX406A)**
- **< 0.1pA Typical Input Bias Current**
- **Output Swings Rail-to-Rail**
- **Input-Voltage Range Includes Negative Rail**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX406ACPA	0°C to +70°C	8 Plastic DIP
MAX406BCPA	0°C to +70°C	8 Plastic DIP
MAX406ACSA	0°C to +70°C	8 SO
MAX406BCSA	0°C to +70°C	8 SO
MAX406BC/D	0°C to +70°C	Dice*
MAX406AEPA	-40°C to +85°C	8 Plastic DIP
MAX406BEPA	-40°C to +85°C	8 Plastic DIP
MAX406AESA	-40°C to +85°C	8 SO
MAX406BESA	-40°C to +85°C	8 SO
MAX406AMJA	-55°C to +125°C	8 CERDIP
MAX406BMJA	-55°C to +125°C	8 CERDIP

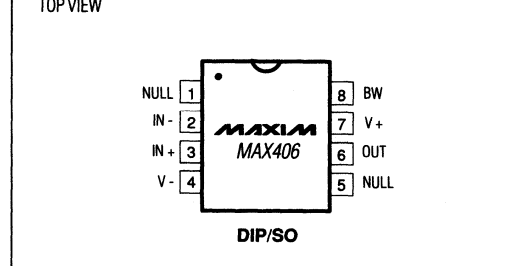
** Contact factory for dice specifications.*

Typical Operating Circuit



REMOTE-SENSOR BUFFER OPERATES FROM 3V BATTERY

Pin Configuration



Ultra-Low Power CMOS Operational Amplifier

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V+ to V-) 12V
Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Continuous Current Pins 2 and 3 ..... 10mA
Continuous Current Pins 1, 5, 6, and 8 ..... 50mA
Short-Circuit Duration ..... Indefinite
Continuous Total Power Dissipation (T_A = +70°C)
8-pin Plastic DIP (derate 6.9mW/°C above +70°C) ... 552mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
8-pin CERDIP (derate 8.0mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX406_CPA/CSA/BCD ..... 0°C to +70°C
MAX406_EPA/ESA ..... -40°C to +85°C
MAX406_MJA ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.5V, V- = -2.5V; T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MAX406A			MAX406B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.25	0.5		0.75	2	mV
Input Bias Current	I_B	V_{CM} = 0V (Note 2)		<0.1	10		<0.1	10	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	200	1000		100	500		V/mV
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V	10	40		10	40		
Gain Bandwidth	GBW	Unity-Gain Stable Mode	4	8		4	8		kHz
		High-Speed Mode	20	40		20	40		
Input-Voltage Range	IVR		-2.5		1.4	-2.5		1.4	V
Output-Voltage Swing	V_O	R_L = 1MΩ	±2.47	±2.49		±2.47	±2.49		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.5V to +1.4V	70	80		54	65		dB
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = +2.5V to +7.5V		70	100		170	300	µV/V
Slew Rate	SR	Unity-Gain Stable Mode	3	5		3	5		V/mSec
		High-Speed Mode	12	20		12	20		
Supply Current	I_{SY}		0.8	1.0	1.2		1.0	1.2	µA
Output Sink Current	I_{OSink}	V_{OUT} = 0V	100	200		100	200		µA
Output Source Current	$I_{OSource}$	V_{OUT} = 0V	300	600		300	600		µA
Supply Voltage (V+ to V-)	V_S		2.5		10	2.5		10	V
Input Noise Voltage	e_n	f_O = 1kHz		150			150		nV/√Hz
		f_O = 0.1 to 10Hz		6			6		µVp-p

Note 2: Production-automated test equipment cannot resolve input bias currents below 1pA.
Lab equipment has shown the MAX406 typical input bias current to be approximately 0.01pA.

ELECTRICAL CHARACTERISTICS

(V+ = +2.5V, V- = -2.5V; T_A = 0°C to +70°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MAX406A			MAX406B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 3)			0.95			3.0	mV
Offset-Voltage Tempco	TC_{VOS}				10				µV/°C
Input Bias Current	I_B	V_{CM} = 0V			20			20	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	100			50			V/mV
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = +5V, V- = -5V	10			10			
Output-Voltage Swing	V_O	R_L = 1MΩ	±2.45			±2.45			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.5V to +1.4V	66			50			dB
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V- = 0V V+ = +2.5V to +7.5V			150			450	µV/V
Supply Current	I_{SY}				1.6			1.6	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	50			50			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	250			250			µA

ELECTRICAL CHARACTERISTICS

(V+ = +2.5V, V- = -2.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MAX406A			MAX406B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 3)			1.10			3.0	mV
Offset-Voltage Tempco	TC_{VOS}				10				µV/°C
Input Bias Current	I_B	V_{CM} = 0V			50			50	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	50			25			V/mV
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = +5V, V- = -5V	10			10			
Output-Voltage Swing	V_O	R_L = 1MΩ	±2.45			±2.45			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.5V to +1.4V	66			50			dB
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = +2.5V to +7.5V			150			450	µV/V
Supply Current	I_{SY}				1.7			1.7	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	40			40			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	250			250			µA

Note 3: MAX406A: Calculated from guaranteed drift spec. and maximum offset voltage at room temperature. The 10µV/°C drift limit is 100% tested.
MAX406B: Guaranteed 100% tested limit.

Ultra-Low Power CMOS Operational Amplifier

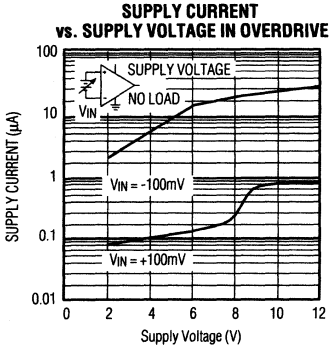
ELECTRICAL CHARACTERISTICS

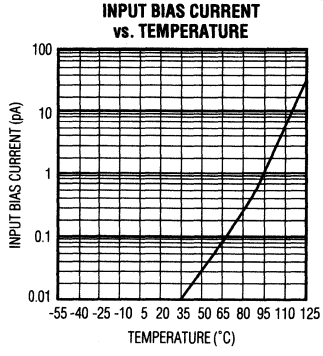
(V+ = +2.5V, V- = -2.5V; T_A = -55°C to +125°C, unless otherwise specified.)

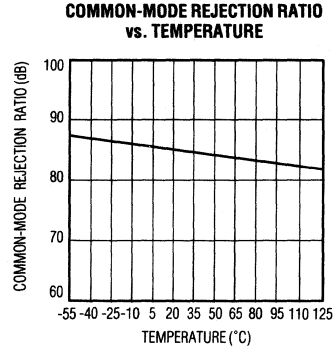
PARAMETER	SYMBOL	CONDITIONS	MAX406A			MAX406B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 3)			1.5			4	mV
Offset-Voltage Tempco	TC_{VOS}				10				µV/°C
Input Bias Current	I_B	V_{CM} = 0V			1.0			1.0	nA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	20			10			V/mV
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = +5V, V- = -5V	10			10			
Output-Voltage Swing	V_O	R_L = 1MΩ	±2.45			±2.45			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.5V to +1.4V	66			50			dB
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = +2.5V to +7.5V			150			450	µV/V
Supply Current	I_{SY}				2.0			2.0	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	20			20			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	200			200			µA

Note 3: MAX406A: Calculated from guaranteed drift spec. and maximum offset voltage at room temperature. The 10µV/°C drift limit is 100% tested.
MAX406B: Guaranteed 100% tested limit.

Typical Operating Characteristics

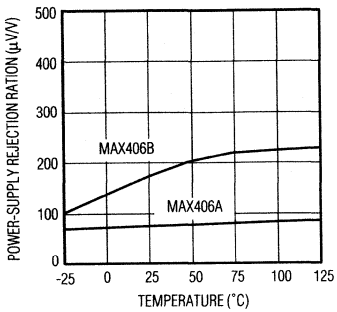




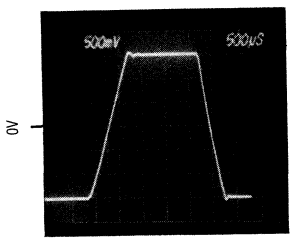


Typical Operating Characteristics (continued)

POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE

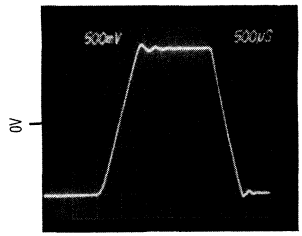


LARGE-SIGNAL TRANSIENT RESPONSE (UNITY-GAIN STABLE MODE)



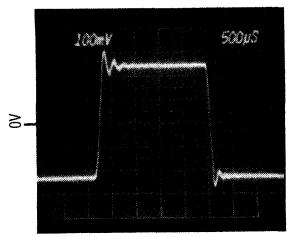
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//250pF

LARGE-SIGNAL TRANSIENT RESPONSE (UNITY-GAIN STABLE MODE)



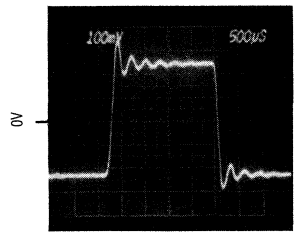
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//1000pF

SMALL-SIGNAL TRANSIENT RESPONSE (UNITY-GAIN STABLE MODE)



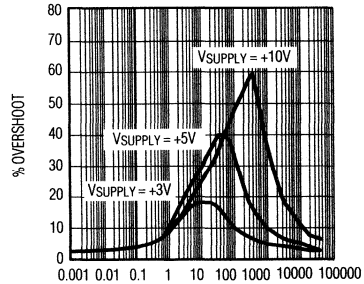
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//250pF

SMALL-SIGNAL TRANSIENT RESPONSE (UNITY-GAIN STABLE MODE)

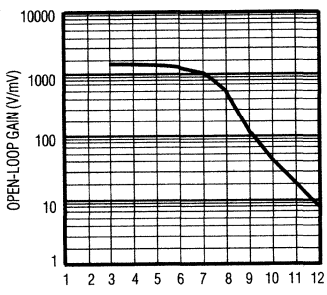


NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//1000pF

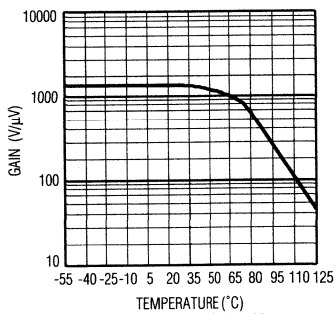
% OVERSHOOT vs. CAPACITIVE LOAD (UNCOMPENSATED MODE)



OPEN-LOOP GAIN vs. SUPPLY VOLTAGE

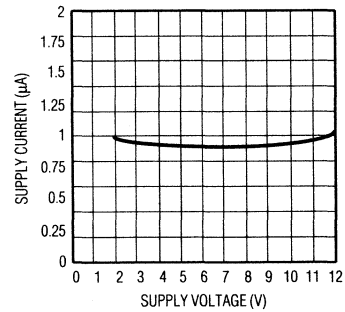


LARGE-SIGNAL GAIN vs. TEMPERATURE



V_{SUPPLY} = ±2.5V, LOAD = 1MΩ

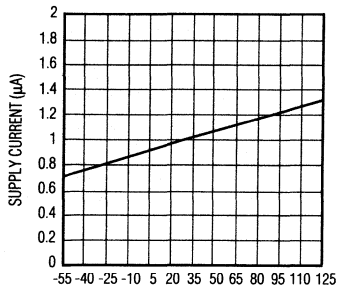
SUPPLY CURRENT vs. SUPPLY VOLTAGE T_A = 25°C, NO LOAD



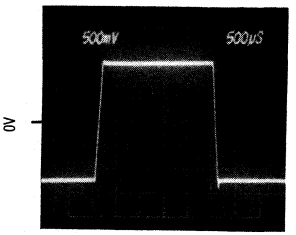
Ultra-Low Power CMOS Operational Amplifier

Typical Operating Characteristics

SUPPLY CURRENT vs. TEMPERATURE NO LOAD

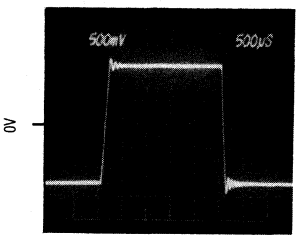


LARGE-SIGNAL TRANSIENT RESPONSE (HIGH-SPEED MODE)



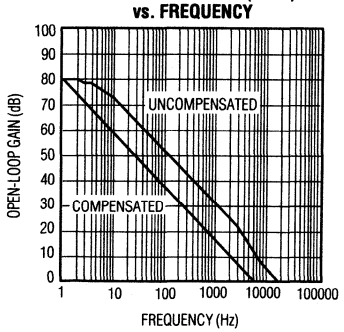
VSUPPLY = ±2.5V, AVCL = 2V/V, LOAD = 1MΩ//15pF

LARGE-SIGNAL TRANSIENT RESPONSE (HIGH-SPEED MODE)

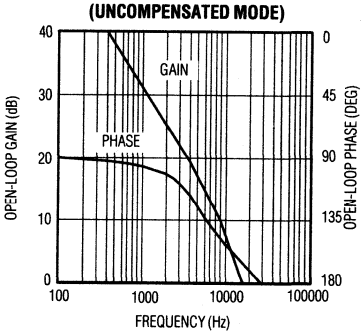


VSUPPLY = ±2.5V, AVCL = 2V/V, LOAD = 1MΩ//250pF

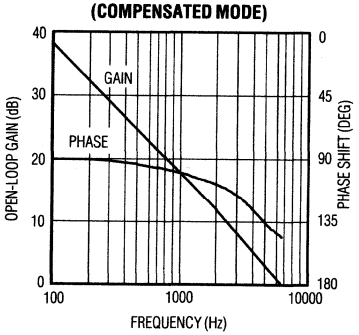
CLOSED-LOOP GAIN (80dB) vs. FREQUENCY



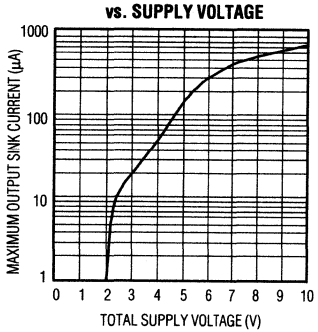
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (UNCOMPENSATED MODE)



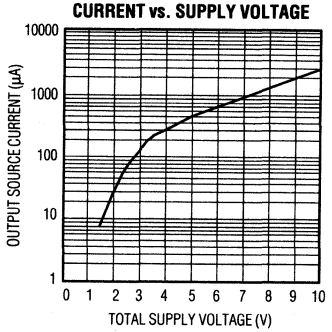
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMPENSATED MODE)



MAXIMUM OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE



Ultra-Low Power CMOS Operational Amplifier

Pin Description

PIN	NAME	FUNCTION
1	NULL	Nulling. Connect to one end of 100kΩ pot for voltage-offset nulling.
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V-	Negative Power-Supply Pin. Connect to (-) terminal of power supply or ground.
5	NULL	Nulling. Connect to other end of 100kΩ pot for voltage-offset trim (connect wiper to V+.)
6	OUT	Output
7	V+	Positive Supply Pin. Connect to (+) terminal of power supply.
8	BW	Bandwidth Selection Pin. Leave floating, connect to V- for unity-gain stability or connect to V+ for high speed.

Application Hints

Trimming Voltage Offset

The MAX406's typical input offset voltage is between 0.25mV and 0.75mV. If the application requires additional offset adjustment, connect a 100kΩ trimpot between pins 1, 5, and 7, as shown in Figure 1.

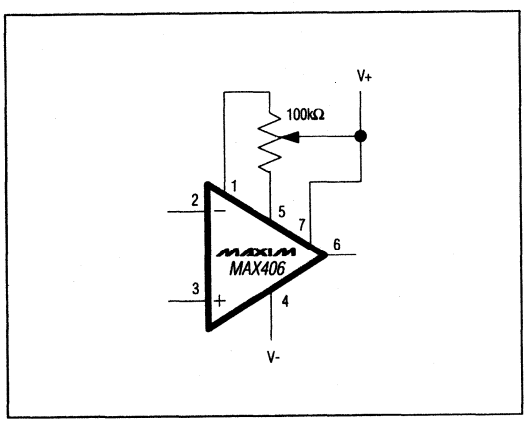


Figure 1. Offset-Voltage Adjustment

Input Overdrive Vs Supply Current

The supply current of the MAX406 remains relatively constant over the supply range as long as the amplifier output is not overdriven to the negative supply rail. For example, when connecting the amplifier as a comparator and applying a -100mV input, supply current rises above the 1μA typical value and varies with supply voltage. This can be seen in the Supply Current Vs Supply Voltage in Overdrive graph in the Typical Operating Characteristics.

Total Supply-Voltage Considerations

Although the MAX406 can operate with supply voltages between 2.5V and 10V, its best performance is achieved with supply voltages below 7V. The Open-Loop Gain vs Supply Voltage graph in the Typical Operating Characteristics shows that the open-loop gain is reduced with supply voltages in excess of 7V.

Unity-Gain Operation

The MAX406 is stable in its unity-gain mode, even while driving heavy capacitive loads, and it functions well as a buffer to slowly moving signals. Input-voltage range limitations (V- to V+ -1.1V) will limit the maximum voltage swing at the output in unity-gain configuration.

Bandwidth

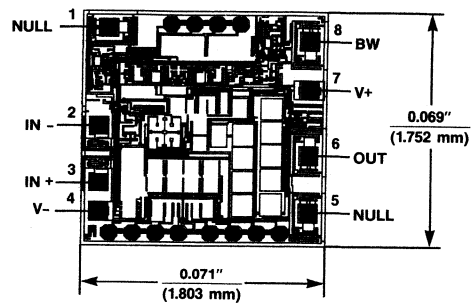
The MAX406 can be placed in two modes of operation by BW (pin 8). Connecting BW to V-, or left floating, internally compensates the amplifier which allows unity-gain stable operation. Connecting BW to V+ (uncompensated) allows the amplifier to be used at higher speed and stabilizes the amplifier for closed-loop gains of 2V/V or greater.

High-Speed Stability

In low-power applications, feedback resistors are likely to be very high values (megohm or greater). This can result in significant phase shift at the summing node which may cause instability in the high-speed mode. A small capacitor (5pF-10pF) in parallel with the feedback resistor (between the output and IN-) will improve stability. The high-speed mode Large-Signal Transient Response photographs show the stability achieved from a 10pF capacitor in parallel with the feedback resistor.

Ultra-Low Power CMOS Operational Amplifier

Chip Topography



Note: Substrate is connected to V+.

ADVANCE INFORMATION

Specifications Based on Evaluation of Limited Number of Devices

MAXIM

Dual, Low-Noise, Low-Voltage Precision Op Amp

General Description

The MAX412 dual operational amplifier sets a new standard for noise performance in low-voltage systems. Input voltage noise density is 100% tested and is guaranteed to be less than 2.4nV/√Hz at 1kHz. A unique design not only combines low noise with ± 5V operation, but also consumes less than 2.5mA supply current per amplifier. Low voltage operation is assured with a guaranteed output voltage swing of ±3.6V into 2kΩ. The MAX412 also operates from supply voltages between ±2.4V and ±5V for greater supply flexibility.

Unity-gain stability, 28MHz bandwidth, and 4.5V/µs slew rate ensure low noise performance in a wide variety of wideband and measurement applications. The MAX412 is available in 8-pin DIP and SO packages in the industry-standard dual op amp pin configuration.

Features

- ♦ **100% Tested Voltage Noise: 2.4nV/√Hz Max at 1kHz**
- ♦ **2.5mA Supply Current Per Amplifier**
- ♦ **Low Supply Voltage Operation: ±2.4V to ±5V**
- ♦ **28MHz Unity-Gain Bandwidth**
- ♦ **4.5V/µs Slew Rate**
- ♦ **250µV Max Offset Voltage**
- ♦ **115dB Min Voltage Gain**
- ♦ **2 Amplifiers in One 8-Pin DIP/SO**

Applications

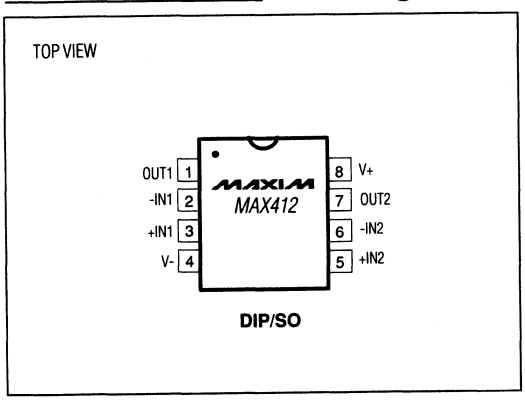
Low Noise-Frequency Synthesizers
Infrared Detectors
High-Qualitiy Audio Amplifiers
Accelerometer and Gyro Amplifiers
Magnetic Search Coil Amplifiers
Ultra-Low Noise Instrumentation Amplifiers
Bridge Signal Conditioning

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX412CPA	0°C to +70°C	8 Plastic DIP
MAX412CSA	0°C to +70°C	8 SO
MAX412C/D	0°C to +70°C	Dice*
MAX412EPA	-40°C to +85°C	8 Plastic DIP
MAX412ESA	-40°C to +85°C	8 SO
MAX412MJA	-55°C to +125°C	8 CERDIP

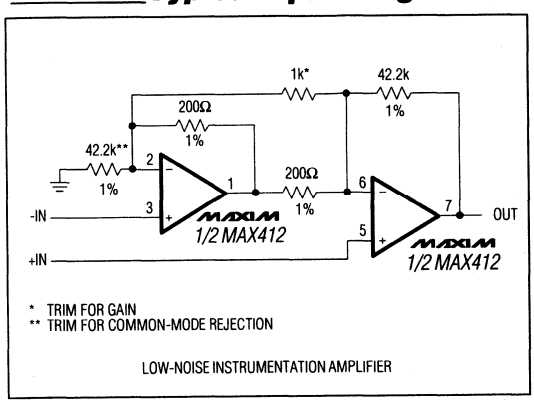
** Dice are specified at T_A = 25°C, DC parameters only.*

Pin Configuration



DIP/SO

Typical Operating Circuit



* TRIM FOR GAIN
** TRIM FOR COMMON-MODE REJECTION

LOW-NOISE INSTRUMENTATION AMPLIFIER

Dual, Low-Noise, Low-Voltage Precision Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Differential Input Current (Note 1) ..... ±20mA
Differential Input Voltage ..... V+ to V-
Common-Mode Input Voltage ..... (V+ +0.3V) to (V- -0.3V)
Short-Circuit Current Duration ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 6.9mW/°C above +70°C) .. 552mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.0mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX412C _ A ..... 0°C to +70°C
MAX412E _ A ..... -40°C to +85°C
MAX412MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1.0V are applied, input current should be limited to 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±120	±250	µV
Input Bias Current	I_B			±80	±150	nA
Input Offset Current	I_{OS}			±40	±80	nA
Differential Input Resistance	R_{IN}(Diff)			20		kΩ
Common-Mode Input Resistance	R_{IN}(CM)			150		MΩ
Input Capacitance	C_{IN}			4		pF
Input Noise-Voltage Density	e_n	f_O = 10Hz		7		nV/√Hz
		f_O = 1000Hz (100% tested)		2	2.4	
Input Noise-Current Density	i_n	f_O = 10Hz		2.6		pA/√Hz
		f_O = 1000Hz		1.2		
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	115	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	96	103		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.7V	115	122		dB
		R_L = 600Ω, V_O = ±3.5V	110	120		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.7	+3.7 -3.8		V
Short-Circuit Output Current	I_{SC}			35		mA
Slew Rate	SR	10kΩ//20pF load		4.5		V/µs
Unity-Gain Bandwidth	GBW	10kΩ//20pF load		28		MHz
Settling Time	t_S	to 0.1%		1.3		µs
Channel Separation	CS	f_O = 1kHz		135		dB
Operating-Supply Voltage Range	V_S		±2.4		±5.25	V
Supply Current	I_S	Both amplifiers		5	5.25	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±150	±350	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±100	±200	nA
Input Offset Current	I_{OS}			±80	±150	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	121		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	97		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.6	110	120		dB
		R_L = 600Ω, V_O = ±3.5V	90	119		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±3.6	±3.7		V
Supply Current	I_S	Both amplifiers			6.5	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±200	±400	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = +3.6V to -3.5V	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.5	+3.7 -3.6		V
Supply Current	I_S	Both amplifiers			6.5	mA

Dual, Low-Noise, Low-Voltage Precision Op Amp

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±200	±400	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = +3.6 to -3.5	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.5	+3.7 -3.6		V
Supply Current	I_S	Both amplifiers			7	mA

ADVANCE INFORMATION

Based on Evaluation of Limited Number of Devices
Contact Factory For Product Update

MAXIM

Ultra High-Precision CMOS Op Amps

General Description

The MAX425/MAX426 precision CMOS amplifiers provide input offset and noise specifications superior to chopper-stabilized amplifiers while using no external capacitors. Two independent error-correction schemes operate on-chip: A unique input switching design reduces input offset voltage (V_{OS}) to 0.5µV, while offsets inside the amplifier are removed with digital correction to reduce common-mode errors and minimize clock ripple. The MAX425 is unity-gain stable with a 350kHz gain-bandwidth product. The MAX426 has a 15MHz gain-bandwidth product, and is stable for closed-loop gains of 30dB (30V/V) or greater.

The error-correction design of the MAX425/MAX426 is completely different from chopper-stabilized amplifiers. Ultra-low V_{OS} is achieved with negligible clock noise, fast overload recovery, improved high-frequency performance, and reduced 1/f noise. 1Hz bandwidth noise is typically $100nV_{p-p}$. The amplifiers are ideal for precision measurement applications where large, accurate gains and low noise are required. The MAX426 is also ideal when wide bandwidth is required.

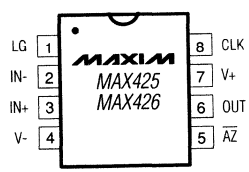
Signal input and power-supply connections conform to the standard op amp pin configuration. Both devices operate from ±2.5V to ±7.5V or from single supplies ranging from +5V to +15V. They are offered in 8-pin DIP and 16-pin wide SO packages.

Applications

Low-Noise DC Amplifier
Weigh Scales
Thermocouple Amplifiers
Strain-Gauge Vibration Analysis

Pin Configurations

TOP VIEW



DIP

Wide SO on page 12

Features

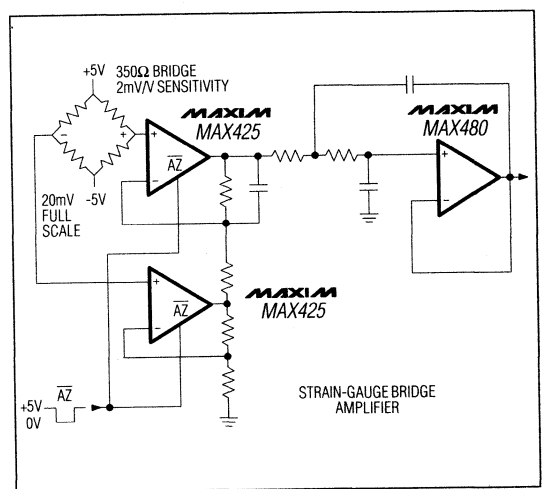
- ♦ **$250nV_{p-p}$ Noise (0.1Hz to 10Hz BW)**
- ♦ **0.5µV Typ V_{OS}**
- ♦ **0.01µV/°C Typ Offset Drift**
- ♦ **No External Components**
- ♦ **Controllable Auto-Zero**
- ♦ **190dB Open-Loop Gain**
- ♦ **15MHz Gain Bandwidth (MAX426)**
- ♦ **Unity-Gain Stable (MAX425)**
- ♦ **Rail-to-Rail Output Swing**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX425C/D	0°C to +70°C	Dice*
MAX425EPA	-40°C to +85°C	8 Plastic DIP
MAX425EWE	-40°C to +85°C	16 Wide SO
MAX425MJA	-55°C to +125°C	8 CERDIP
MAX426C/D	0°C to +70°C	Dice*
MAX426EPA	-40°C to +85°C	8 Plastic DIP
MAX426EWE	-40°C to +85°C	16 Wide SO
MAX426MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Ultra High-Precision CMOS Op Amps

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) ..... +18V
Input Voltage Range ..... (V+ +0.3) to (V- -0.3) V
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin (except pins 2 and 3) 50mA
Current into Pins 2 and 3 ..... 10mA
Continuous Total Power Dissipation (any package) ... 300mW

Operating Temperature Ranges:
MAX42_EPA/EWE ..... -40°C to +85°C
MAX42_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V; $T_A = T_{MIN}$ to T_{MAX}; LG = 0V; Auto-Zero activated after power-up, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1, 2)	V_{OS}	T_A = +25°C	After auto-zero, CLK off		0.5	5	µV
			Before auto-zero, CLK off		50	500	
Offset Tempco (Note 3)	$\Delta V_{OS}/\Delta T$	After auto-zero, CLK off			0.005	0.05	µV/°C
		No auto-zero, CLK on			0.01	0.05	
Offset Tempco	$\Delta V_{OS}/\Delta T$	Auto-zero off, CLK off			0.5	10	µV/°C
Input Bias Current CLK Off (Note 4)	I_B	At IN+ and IN-, CLK off	T_A = +25°C		0.2	10	pA
			T_A = +85°C		5	100	
			T_A = +125°C		0.15	5	nA
Input Bias Current (Charge Injection) CLK On (Note 4)	I_B	At IN+ and IN-, CLK on	Internal CLK		120	200	pA
			External CLK		0.4		pA/Hz
Large Signal Gain	A_{VOL}	R_L = 10kΩ		140	190		dB
Output Voltage Swing		R_L = 2kΩ		±3.5	±4.4		V
		R_L = 10kΩ		±4.7	±4.9		
Common-Mode Voltage Range	CMVR	V+ = +5V	V- = -5V	+3/-4			V
			V- = 0V		+3/+1		
Common-Mode Rejection Ratio (Note 1)	CMRR	CMVR = -4V to +3V	With auto-zero at CMV	120	150		dB
			Internal CLK, auto-zero off		130		
			Auto-zero off, CLK off	70	85		
Power-Supply Rejection Ratio (Note 1)	PSRR	V_{SUP} = ±4.5V to ±5.5V	Auto-zero at both limits	120	150		dB
			Auto-zero off, CLK off	80	95		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V; T_A = T_{MIN} to T_{MAX}; LG = 0V; Auto-Zero activated after power-up, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Noise Voltage	e_N	T_A = +25°C; R_S = 100Ω; Internal CLK	In 0.1Hz to 1Hz BW		0.1		μV_{p-p}
			In 0.1Hz to 10Hz BW		0.25		
		T_A = +25°C; R_S = 100Ω; CLK off	In 0.1Hz to 10Hz BW		1.5		μV_{p-p}
			In 1kHz to 100kHz BW, Figure 10		2.5		μV_{RMS}
Gain-Bandwidth Product	GBWP	T_A = +25°C	MAX425	0.25	0.35		MHz
			MAX426	8	15		
Slew Rate	SR	T_A = +25°C	MAX425	0.25	0.4		V/µs
			MAX426	8	12		
Operating Supply Range				4.75		15.75	V
Supply Current	I_{SUP}	No load after auto-zero			1.2	1.4	mA
Short-Circuit Current	I_{SC}	T_A = +25°C; V_{OUT} = 0V		5	9	15	mA
Switching-Clock Frequency	f_C	T_A = +25°C; CLK pin open		200	300	450	Hz
CLK Input Current	I_{CLK}	External clock operation	V_{CLK} = V+		6	20	µA
			V_{CLK} = 0V		-35	-100	
$\overline{AZ}$ Input Logic Levels		LG = 0V, High level		2			V
		LG = 0V, Low level				0.8	
$\overline{AZ}$ Input Current					0.1	10	µA
LG Input Current					5	20	µA
$\overline{AZ}$ Input Pulse Width				10			µs
$\overline{AZ}$ Input Transition Time						0.25	µs
Auto-Zero Duration		MAX425			125	200	ms
		MAX426			31	50	

Note 1: V_{OS}, CMRR, and PSRR errors are all corrected during auto-zero operation.
Note 2: With CLK on and following an auto-zero cycle, the input offset voltage consists of a square wave with a typical amplitude of $1\mu V_{p-p}$.
Note 3: Specification is guaranteed by design and correlates with internal amplifier parameters. Thermocouple effects inherent in high-speed automatic test systems prevent measurement of these levels in a production environment.
Note 4: Input bias current is largely a leakage term and doubles every 8°C. Total input current also includes charge injection when internal CLK is operating, or if CLK is driven from an external source. See Input Bias Current with CLK on (Charge Injection) specification.

Ultra High-Precision CMOS Op Amps

Pin Description

8-PIN DIP	16-PIN SO	NAME	FUNCTION
1	1	LG	Auto-Zero Logic Ground—usually 0V.
–	2, 3, 6, 7, 11, 14, 15	N.C.	No Connect
2	4	IN-	Inverting Op Amp Input
3	5	IN+	Noninverting Op Amp Input
4	8	V-	Negative Power Supply
–	9	AZ STAT	Auto-Zero Status Output – open-drain p-channel FET. Pulled to V+ during auto-zero cycle. FET on resistance is typically 500Ω.
5	10	$\overline{AZ}$	Auto-Zero Control Input: Pulse low to start auto-zero cycle. Connect to V+ to turn off. Connect with LG to 0V to activate auto-zero cycles at 1 minute intervals.
6	12	OUT	Amplifier Signal Output
7	13	V+	Positive Power Supply
8	16	CLK	Clock Input. Leave open for 300Hz switching clock, connect to V+ to disable, or drive from clock source. With CLK pin open, CLK signal is 128 times faster than the input switch frequency.

Detailed Description

Auto-Correction Circuitry

The MAX425/MAX426 unique precision amplifier design employs two independent error-correction schemes. A switching input amplifier eliminates V_{OS} and minimizes 1/f noise, and digital auto-zeroing corrects all internal amplifier stage offsets to remove common-mode errors and clock ripple. Figure 1 shows a block diagram of the basic architecture. The amplifier can be set to use both, one, or none of these correction techniques. Table 1 outlines the op amp's characteristics with various auto-correction combinations.

"Switching" Op Amp

A 300Hz internal switching clock switches the inputs. Internal errors that vary slowly compared to 300Hz, such as thermal drift, input offset, low-frequency noise, power-supply sensitivities, and common-mode errors, are all dramatically reduced. Since low-frequency noise looks

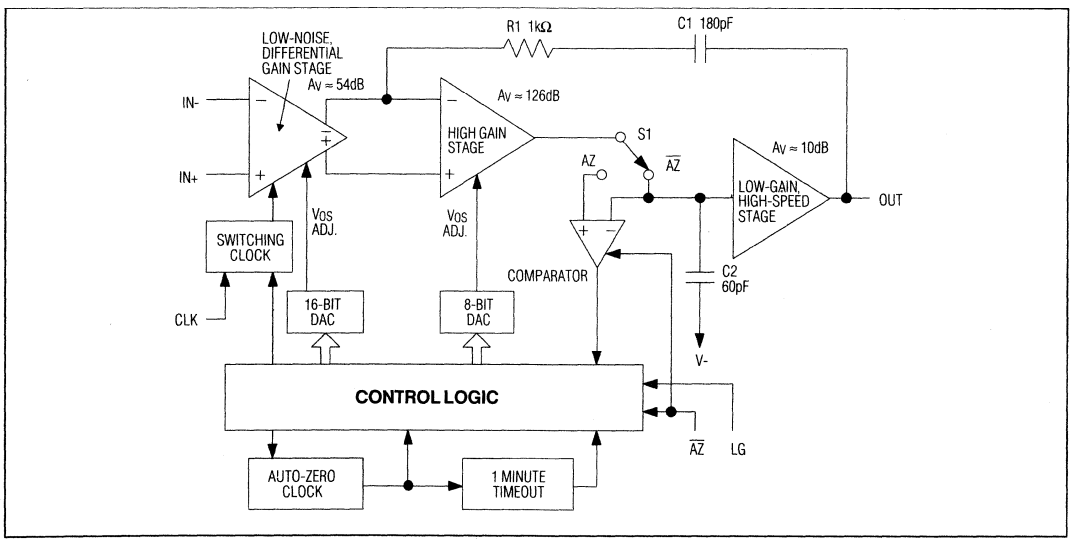


Figure 1. Block Diagram of MAX425 Op Amp

like a slowly varying offset signal, 1/f noise (about 300nV/√Hz at 1Hz before switching) is removed the same way as offset. The main noise contribution is from wideband noise at the input switching frequency, which is demodulated and appears as low-frequency noise at the output. In this case, the noise density at 300Hz is typically 17nV/√Hz. Wideband noise (1kHz to 100kHz) is typically 2.5μVRMS. This corresponds to a noise voltage density of 8nV/√Hz.

In a switching amplifier, the inputs and outputs of the differential input stage are periodically swapped. Figure 2 shows this type of amplifier configured with a closed-loop gain of 100. The example assumes a 1mV offset (mismatch) between P1 and P2. Figure 2A's circuit generates an output signal of 100(V_{IN} - 1mV), or 100V_{IN} - 100mV. When the inputs and outputs of P1 and P2 are interchanged, the output signal becomes 100V_{IN} + 100mV. Note: The offset error, but not the input signal, has changed polarity. Therefore, by switching back and forth with a 50% duty cycle, the output averages to 100V_{IN} while the offset error averages to zero. The output then consists of the desired signal with a small superimposed square wave whose amplitude is the internal offset voltage. The square-wave amplitude is negligibly small because digital auto-zeroing reduces the internal offset to less than 1μV.

Digital Auto-Zero

In addition to switched inputs, the MAX425/MAX426 also employ digital auto-zeroing circuitry. In conventional auto-zero schemes, capacitors store offset correction signals, but require frequent updating because leakage currents soon drain this information from the capacitors. The MAX425/MAX426 eliminate this problem by storing the corrections digitally. A 16-bit DAC, with 0.1μV resolution, supplies the actual error-correction voltage that cancels the amplifier's internal first-stage offset voltage. An 8-bit DAC performs a similar task in the second amplifier stage.

An auto-zero cycle can be initiated manually or at approximately 1 minute intervals by an internal clock. An auto-zero cycle lasts approximately 125ms for the MAX425 and 31ms for the MAX426. During this time, the $\overline{AZ}$ input is ignored, and the amplifier output remains fixed near the output level it had just prior to auto-zero. The amplifier returns to normal operation when the cycle ends.

Digital correction reduces the need for auto-zeroing. Hours can pass between auto-zero cycles without loss of DC accuracy. The only detrimental effect is slight changes in clock ripple as internal (but not input) offsets drift without correction. V_{OS} is still kept within specified limits by the input switching circuitry. In practice, the amplifier is typically auto-zeroed during other system calibration routines while the signal path is inactive.

Table 1. Auto-Correction Characteristics

$\overline{AZ}$	CLK	Correction Mode	Characteristics
⊓⊔	OPEN	Input Switching On, Manual Auto-Zero	V_{OS} = 0.5μV typ. Inputs switch at 300Hz or at external clock rate. One auto-zero cycle follows $\overline{AZ}$ going low. Auto-zero disables amplifier for 125ms (31ms – MAX426). Clock ripple drops to 1μV_{p-p} after auto-zero. Frequent auto-zero NOT required for 1μV V_{OS}.
0V	OPEN	Input Switching On, Internal Auto-Zero	V_{OS} = 0.5μV typ. Inputs switch at 300Hz or at external clock rate. Auto-zero cycles occur at approximately 1 minute intervals. Auto-zero disables amplifier for 125ms (31ms – MAX426).
⊓⊔	V+	Input Switching Off, Manual Auto-Zero	V_{OS} = 0.5μV typ. Input switching disabled. No clock ripple (clock off) V_{OS} nulled after auto-zero cycle. Auto-zero disables amplifier for 125ms (31ms – MAX426). Required auto-zero rate depends on thermal environment.
V+	V+	Input Switching Off, Auto-Zero Off	V_{OS} < 500μV max, 50μV typ. Auto-zero disabled Input switching disabled. No clock ripple (clock off). Lowest input bias current (0.2pA typ. at +25°C.) Works as an uncorrected CMOS op amp.

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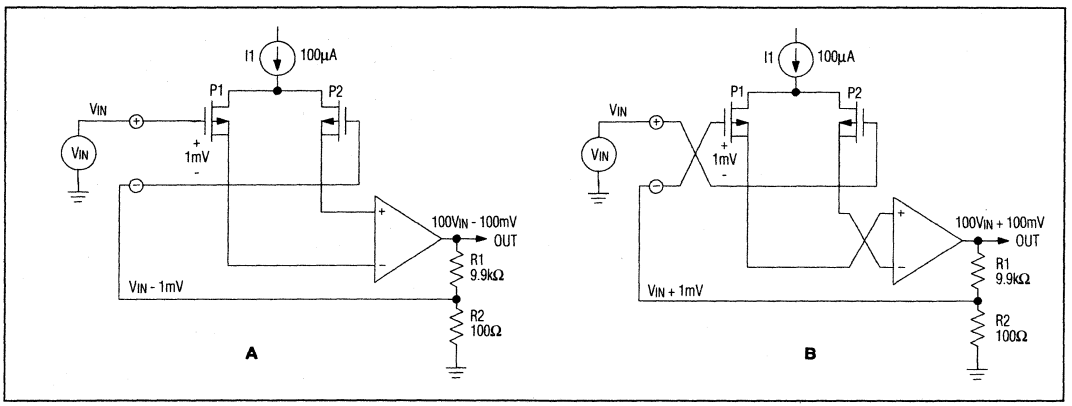

Figure 2. Switching-Amplifier Operation. In Figure A, offset voltage appears as -100mV at the output of the amplifier; in Figure B, it is +100mV. If the duty cycle of each state is 50%, the offset voltage at the output averages zero.

Only the internal DAC resolution and the inherent amplifier noise limit the repeatability of the digital auto-zero circuitry. Consequently, successive auto-zero cycles are repeatable to within 0.1µVRMS.

Overload Recovery

Since digital offset nulling also allows corrections to be stored digitally and not on capacitors, the MAX425/MAX426 recover almost immediately from an overload condition. The MAX425/MAX426 typically recover from overload in less than 10µs, compared to tens of milliseconds for most chopper-stabilized amplifiers. Figure 3 plots the overload recovery characteristic of the MAX426.

Auto-Zero Control Inputs

$\overline{AZ}$ controls auto-zero calibration. With LG at 0V, $\overline{AZ}$ can be driven with TTL or CMOS levels as long as V+ and V- are not exceeded. With ±5V operation, LG connects to supply ground and the op amp zeros when $\overline{AZ}$ is pulled within 0.8V of LG (Figure 4) for at least 10µs. The auto-zero cycle begins within 2µs and lasts about 125ms for the MAX425, 31ms for the MAX426. For single-supply operation, LG can be tied to V-. Again, when $\overline{AZ}$ is pulled to within 0.8V of LG, the amplifier zeros.

If $\overline{AZ}$ is tied low along with LG, an auto-zero cycle is internally triggered approximately once per minute. The input switching clock controls this interval, so CLK must not be disabled if auto-zero cycles are to be internally triggered. When an external clock source is used at the CLK input, the relation between this rate and the time between auto-zero cycles is: t_{AZ} (sec.) = 16,384/f_{CLK}. Although the time between cycles depends on CLK, the auto-zero cycle itself is timed by a separate

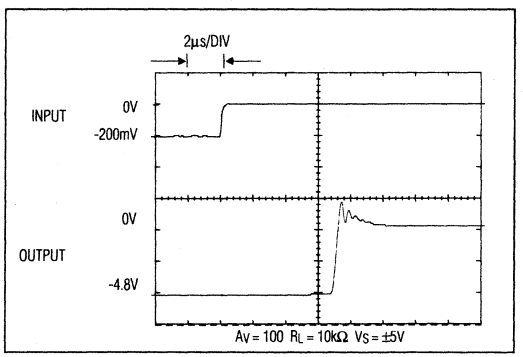

Figure 3. MAX426 Overload Recovery Time

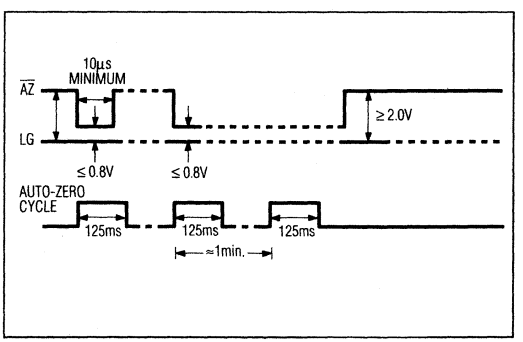

Figure 4. Auto-Zero Calibration Cycle Initiation – MAX425 cycle duration is 125ms and MAX426 is 31ms.

internal oscillator, independent from CLK, that runs only during auto-zero calibration.

During auto-zero, the amplifier's noninverting input remains connected to the input signal while the inverting input is internally shorted to the noninverting input. The output stage is held within 0.2V of its previous level. Since the amplifier is zeroed with both signal inputs shorted together at IN+, common-mode offset error is zeroed during calibration. Similarly, DC power-supply rejection error is auto-zeroed.

The auto-zero status function (AZ STAT) is available on pin 9 of the 16-pin small outline (SO) packages only. AZ STAT connects to the drain of a p-channel FET that is pulled to V+ while the device executes an auto-zero command. The typical FET on resistance is about 500Ω. By attaching a 47kΩ pull-down resistor from this pin to the system logic ground, the operator can monitor the device auto-zero cycle.

Amplifier Output

The MAX425/MAX426 feature 190dB of open-loop gain. Consequently, the amplifier's closed-loop DC gain error is negligible in even the most precise high-gain applications.

Outputs can swing from V+ to V- under lightly loaded conditions. Output impedance is typically 300Ω. Because the MAX425/MAX426 operate typically at 12mW, the chip temperature rises only 1°C to 2°C above ambient temperature. Such low self-heating minimizes thermocouple errors. Although optimized for 10kΩ loads, the MAX425/MAX426 drive a 2kΩ load to within a volt of each supply. However, such low-impedance loads are not recommended for precision applications, because changes in power dissipation within the op amp cause thermal gradients that limit performance. The current-limited output can withstand short circuits to either power supply or ground indefinitely.

Power Supply and Input Range

The MAX425/MAX426 are specified with a 10V (or ±5V) power supply, but will also operate with supplies ranging from 5V (±2.5V) to 15V (±7.5V). When operating with a 15V power supply, the amplifier's common-mode input voltage ranges from V- to V+ -2V. (Best common-mode and power-supply rejection are achieved with V_{IN} between V+ -2.5V and V- +1V.) A single 5V supply reduces the input common-mode voltage range to between 1V and 3V. As with most precision analog components, each supply should be bypassed at the amplifier with a 0.1µF ceramic capacitor.

The MAX425/MAX426 require 30ms on power-up to allow calibration circuits to initialize. However, the amplifier does NOT automatically auto-zero on power-up. The MAX425/MAX426 require a minimum supply of 4.5V to ensure the digital calibration circuit functions properly. The supply current is about 2.5mA until the first auto-zero cycle is initiated. Following the initial auto-zero cycle, the supply current typically drops to 1.2mA.

Input Bias Current

Two independent components comprise the input bias current: junction leakage current and charge injection current. The junction leakage current comes from the input protection diodes and the FET switches. The input protection diodes are very compact to minimize leakage currents. Thus, while still maintaining overvoltage protection, the leakage current is approximately 0.03pA at +25°C. Since package and printed circuit board leakage can add to this significantly, pay special attention to layout for accurate measurements.

The leakage current approximately doubles for every 8°C rise in temperature. This results in an input bias current of about 150pA at +125°C and 1.2nA at +150°C. This current tends to track in both input leads. For example, the offset current at +150°C is typically 20pA.

The second component of input bias current is charge injection current. This comes from the switching-clock circuitry. The bias current from charge injection is directly proportional to the clock frequency and varies with supply voltage. With ±5V supplies and a nominal 300Hz switching frequency, the charge injection current is about 120pA. This current flows into the IN+ terminal and out of the IN- terminal. At other clock frequencies, calculate the charge injection current by multiplying the switching-clock frequency by 0.4pA/Hz. If the switching clock is disabled, there is no charge injection input bias current. Charge injection current changes very little with temperature.

Below +125°C, charge injection current is the major component of the total input bias current. Above +125°C, the junction leakage current dominates the total input bias current.

In order to cancel the bias current-induced input offset voltage, circuit designers often add extra resistors to match the equivalent resistance at each of the amplifier input terminals. This technique reduces the apparent input offset voltage of most op amps because the bias current usually matches in magnitude and direction between the two input terminals. Thus, assuming matched input bias currents, any voltage at the op amp input due to bias current appears as a common mode, not a differential input voltage.

Bias current cancellation resistors should NOT be used when the MAX425/MAX426 are operated with the switching clock. In this case, the charge injection component dominates the input bias current. The charge injection current flows in opposite directions in the

Ultra High-Precision CMOS Op Amps

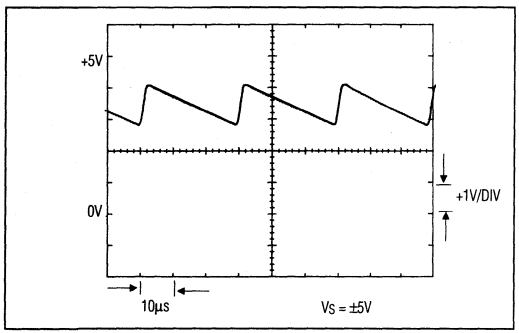

Figure 5. Typical Waveform at CLK Pin

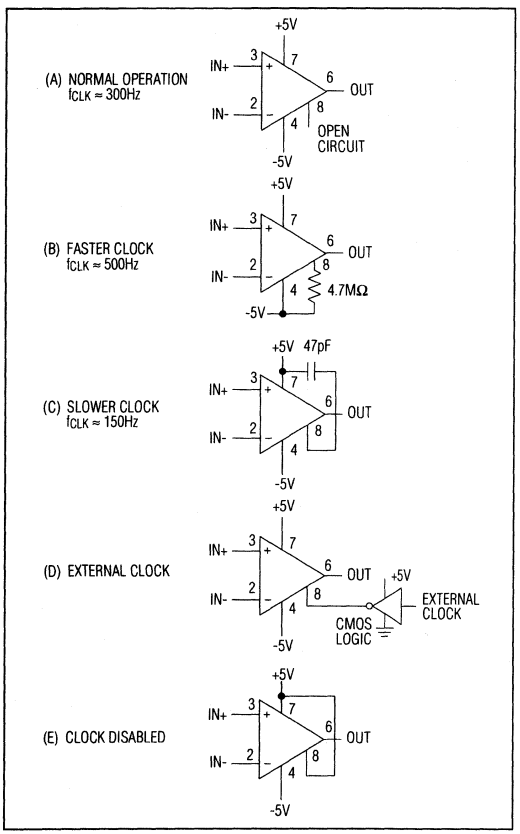

Figure 6. The oscillator frequency for the switching amplifier can be altered as shown in drawings (A) through (E).

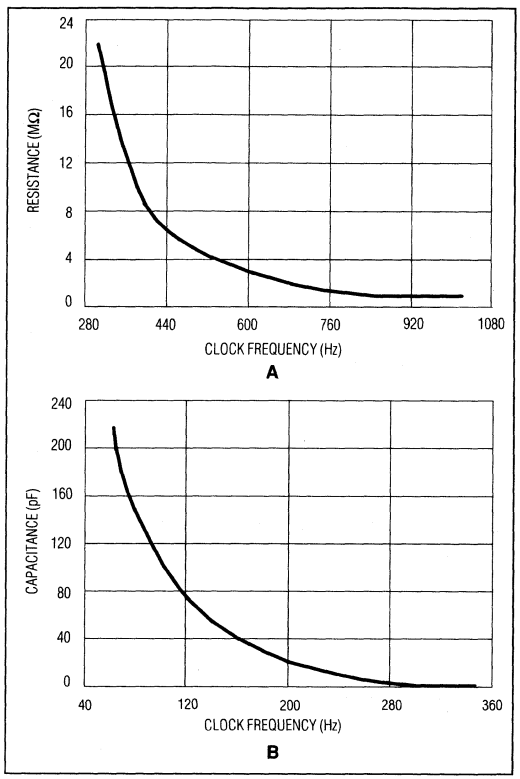

Figure 7. A: Clock Frequency vs. Resistance (Resistor to V-) B: Clock Frequency vs. Capacitance (Capacitor to V+)

MAX425/MAX426 input terminals. Thus, instead of cancelling offsets due to bias current flowing through resistors, the error signals add together and actually increase the apparent offset voltage.

In high-temperature applications (above +125°C) where the clock isn't used, the junction leakage current component dominates the input bias current. The junction leakage current flows into both amplifier inputs. When operating under these conditions, the circuit designer should match the resistance paths in both input leads to take advantage of the excellent matching of leakage currents. The input offset current of the MAX425/MAX426 is typically less than 2nA at +200°C.

Internal/External Clock

The MAX425/MAX426 internal switching clock free runs at about 38kHz with no external components connected to CLK and is internally divided by 128. A 300Hz input

switching frequency results. CLK connects directly to an internal 20pF timing capacitor where the signal oscillates between V+ -1V and V+ -2V. Figure 5 plots a typical waveform at CLK. The clock frequency can be adjusted or driven as shown in Figure 6.

To slow the internal clock, add a capacitor between CLK and V+. To increase clock rate, connect a resistor from CLK to V-. The frequency should not be increased by more than a factor of 3 using this technique. The oscillator can also be shut down by driving CLK to within 0.1V of V+ or below V+ -3.0V. Figure 6 shows all of the clock operating modes. Figure 7A shows the typical variation of the internal clock frequency vs. resistance between CLK and V-. Figure 7B shows the typical variation of the internal clock frequency vs. capacitance between CLK and V+.

When driving CLK from an external source, the input signal should swing within 0.1V of V+ and at least 3V below V+. Standard CMOS logic families do this reliably. These levels will override the internal oscillator AND the internal divider, so the external clock rate and the input switching frequency will be the same. When directly driving CLK, only a 50% duty-cycle square wave can be used for optimum offset correction. (The internal divider is disabled and cannot "square up" the waveform.) If necessary, a flip-flop or divider should be connected between the clock source and the CLK input to ensure a precise 50% duty-cycle.

Applications Information

Noise

The MAX425/MAX426 are the first offset-corrected op amps designed primarily for low-noise performance. Clock feedthrough, ripple, low frequency (1/f), and wideband noise are three to five times lower than present chopper-stabilized amplifiers. Figure 8A shows noise in a 10Hz bandwidth below 250nVp-p. Figure 8B shows noise in 1Hz bandwidth. Low noise is especially important where high-resolution measurements are made since such noise limits resolution and requires excess filtering. In Figures 9A and 9B, 10Hz and 1Hz noise are shown with the CLK disabled. This noise is greater than that shown in Figure 8 because the switching clock no longer removes the amplifier's 1/f noise. Figure 10 shows the wideband noise (1kHz to 100kHz) of a MAX426.

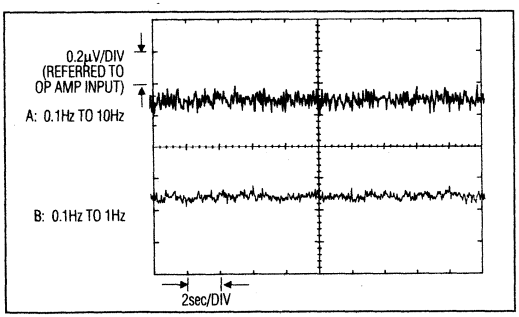

Figure 8. MAX425/MAX426 Noise in 10Hz and 1Hz Bandwidths (Switching Clock On)

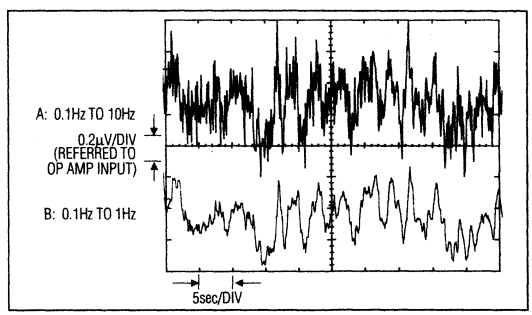

Figure 9. MAX425/MAX426 Noise in 10Hz and 1Hz Bandwidths (Switching Clock Off)

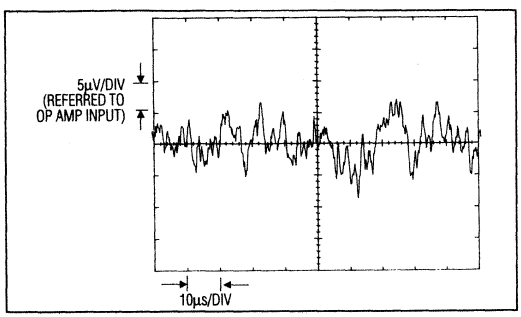

Figure 10. MAX425/MAX426 Wideband Noise (1kHz to 100kHz) (Swithching Clock Off)

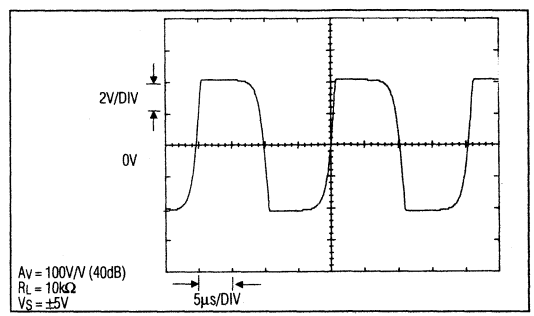

Figure 11. MAX426 Large Signal Response (Response to 80mVp-p, 50kHz Square-Wave Input)

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Switching-Clock Frequency

The clock-induced input bias current of the amplifier (due to the switching action) varies directly with the CLK frequency. This current is about 120pA with a 300Hz switching clock and increases at a rate of about 0.4pA/Hz. In applications where input bias current specification is critical (such as low-level current to voltage converters), operate with a low clock frequency or disable the clock. The input bias current with the clock disabled is typically 0.2pA at +25°C. Even without the clock, the MAX425/MAX426 input offset voltage and noise specifications exceed those of most CMOS op amps.

High-Frequency Applications - MAX426

With a midband voltage noise density of $8nV/\sqrt{Hz}$, the wideband MAX426 has the same broadband noise as a 3.9kΩ resistor. This, along with its 15MHz gain bandwidth, makes it a logical choice for high-precision, high-speed applications. Symmetric output drive capability also allows the MAX426 to perform out to its gain-bandwidth limit. The MAX426 is designed to be stable with a closed-loop gain of 30V/V (30dB) or greater. Figure 11 shows a MAX426 operating at a closed-loop gain of 100V/V (40dB). The input signal is an $80mV_{p-p}$ square wave at 50kHz. Note the high degree of symmetry at the amplifier output.

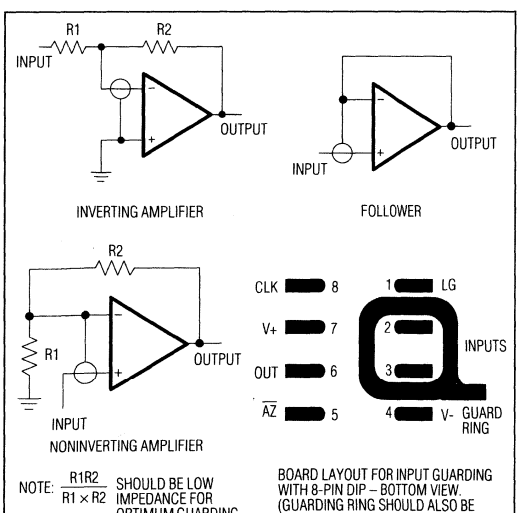


Figure 12. Input-Guard Connections

Working with Low-Level Signals

To take full advantage of the MAX425/MAX426 drift and offset capabilities when amplifying low-level signals, the circuit must be laid-out carefully. Unfortunately, in many low-level circuits, a schematic alone does not provide all the necessary information for a successful design. External characteristics that can degrade "ideal" performance include thermoelectric effects, noise pickup, board leakage, and improper grounding.

Thermoelectric potentials are created when wires/circuit board traces made from dissimilar metals are subjected to temperature gradients. The same principle works with thermocouples. When it occurs in the input of precision circuitry, the resulting voltage (often many microvolts) adds to temperature drift and offset errors. The most effective way to minimize this is to match the dissimilar metals or junctions in the circuit, remove the temperature gradient, or both.

Noise pick-up is best eliminated by minimizing the physical size of the input portions of the circuit. The summing input node (IN-) on high-gain stages is critical. Components connected to this point should have the shortest lead length on the amplifier side, and board traces should be as short as possible. If input lines must be long, use shielded wire.

Board leakage can degrade amplifier performance in high-gain stages that employ large resistances. Even low gain may be susceptible if signal source impedance is very high. In such applications, a guard ring (Figure 12) provides a low impedance point for external leakage currents to flow. Guard both sides of the board. The guard potential should be close to that of the inputs. Also remove flux and other residue from handling. Surface coating may be desirable for harsh environments, but take extreme care to ensure that contaminants are not trapped beneath the coating.

Single-point grounds are mandatory for low-level, high-gain circuits. The key is to ensure ground current from amplifier outputs do not generate ground differentials, which are seen by input stages in a way that makes them indistinguishable from real input signals.

High-Temperature Operation

Although the MAX425/MAX426 are not tested at temperatures above +125°C, input-switching and auto-zero functions will operate to about +150°C. At temperatures beyond +150°C, the internal clock will no longer function properly, and the amplifier cannot be auto-zeroed. But it still maintains operation as an unswitched, nonauto-zeroed CMOS op amp. At +200°C, input bias current is typically 50nA, and offset drift is about 0.5µV/°C. Plastic packaged parts should not be operated at ambient temperatures above +150°C.

Integrating Analog-to-Digital Converters

Because of their design flexibility, the MAX425/MAX426 can be used in many applications. For example, as the front-end integrator of a dual slope ADC, digital auto-zeroing nulls the offset of the amplifier as it discharges the integration capacitor. The switching clock may or may not be used during signal integration. The clock substantially reduces 1/f noise. Without the clock, input current (devoid of any switching spikes) is typically less than 1pA, which is orders of magnitude below the input bias current of bipolar amplifiers. During reference integration, the switching clock is held off to keep the output free of clock glitches. MAX425/MAX426 accuracy and noise performance allow a 20-bit dual slope ADC to be realized.

Weigh Scale

In the weigh-scale circuit of Figure 13, two amplifiers (A1 and A2) with appropriate gain resistors (R1 through R4), amplify the differential 20mV full-scale signal of the strain-gauge bridge by a factor of 300. This signal is then filtered and buffered by A3. The filter's approximate 3Hz bandwidth limits output noise to around 12μV_{RMS} (40nV_{RMS} referred to the input), which gives a signal-to-noise ratio of 114dB. Scale measurement to within a few parts per million is possible.

The two amplifiers A1 and A2 are auto-zeroed simultaneously. This only needs to be done occasionally (several minutes or more) because the effects of internal drift appear only as a small 300Hz ripple signal with an average value of zero. This ripple is removed by the 3Hz filter. Amplifiers A1 and A2 switching clocks free run to minimize 1/f noise. A3 1/f noise is not significant because of A3's low gain. Figure 13 assumes the strain gauge is loaded with a tare weight, so the output signal is always positive. Consequently, A3's output is always positive, so A1, A2, and A3 may all be powered from a single 10V supply. R7 and C4 keep the voltage across C3 to a minimum without affecting the performance of the filter. For optimal performance, guard traces on the top and bottom of the printed circuit board should surround both the sensitive nodes where R5, R6 and C2 connect and the IN+ node of the amplifier.

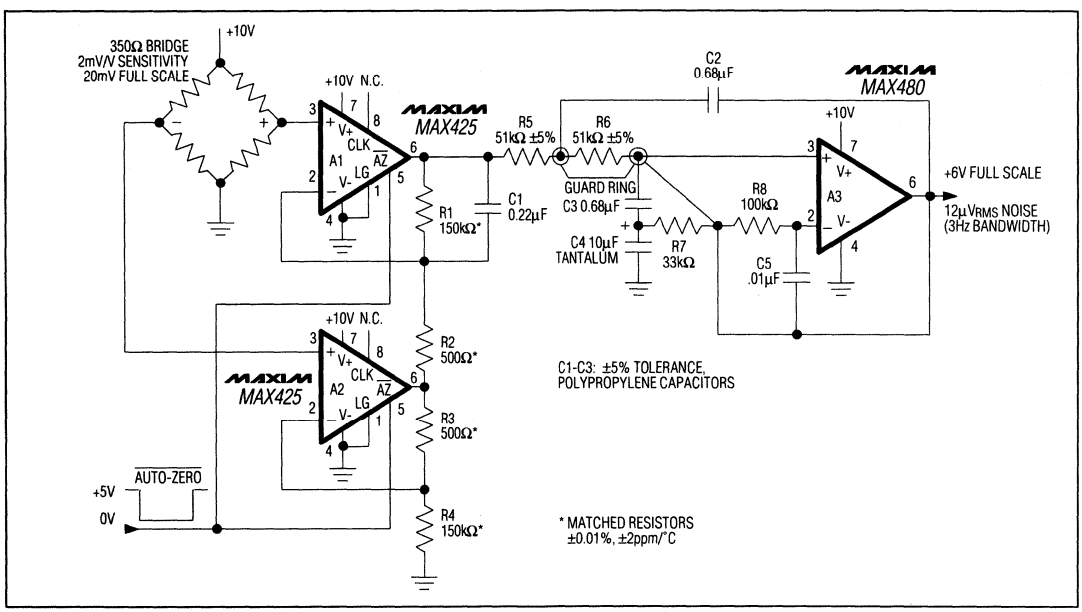
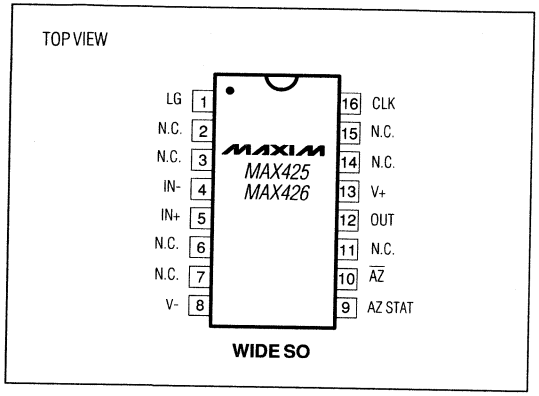


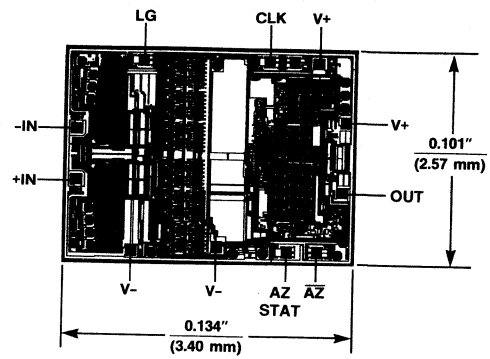
Figure 13. Weigh-Scale Circuit

Ultra High-Precision CMOS Op Amps

Pin configurations (continued)



Chip Topography



MAXIM

High-Precision, Low-Voltage, Micropower Operational Amplifier

General Description

Maxim's new MAX480 is a precision micropower operational amplifier with flexible power-supply capability and superior DC performance characteristics over the industry standard OP90. The MAX480's guaranteed 70μV maximum offset voltage (25μV typ) is the lowest of any other micropower op amp. This represents a better than two times improvement over the highest grade OP90A. Similarly, input bias current, input offset current and drift specifications are improved over the OP90 Family.

Both input and output voltage ranges include the negative supply rail, allowing maximum signal range capability in single-supply applications. The MAX480 operates with either single supplies ranging from +1.6V to +36V or dual supplies from ±0.8V to ±18V. The MAX480 consumes less than 20μA, allowing operation in excess of 10,000 hours from a 250mA-hr lithium coin cell. Even with a minimal quiescent current, the amplifier sinks or sources 5mA from its output.

The MAX480 is available in 8-pin DIP and Narrow Small Outline (SO) packages in commercial, extended and military temperature ranges.

Applications

Precision Micropower Amplifiers

Micropower Signal Processing

Battery-Powered Analog Circuits

Features

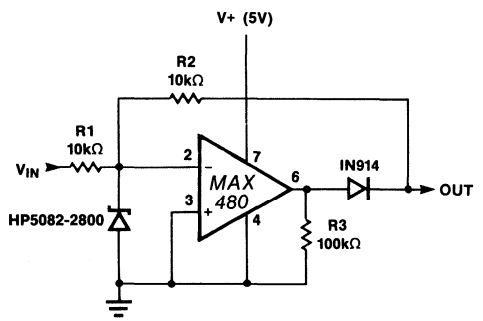
- **Single- or Dual-Supply Operation: +1.6V to +36V, ±0.8V to ±18V**
- **True Single-Supply Operation: Input and Output Voltage Ranges Include Ground**
- **1.5μV/°C Max Offset Voltage Drift**
- **20μA Max Supply Current**
- **5mA Min Output Drive**
- **70μV Max Input Offset Voltage**
- **3nA Max Input Bias Current**
- **700V/mV Min Open-Loop Gain**
- **Standard 741 Pin Out With Nulling to V-**
- **Improved OP90 Replacement**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX480CPA	0°C to +70°C	8 Plastic DIP
MAX480CSA	0°C to +70°C	8 Narrow SO
MAX480EPA	-40°C to +85°C	8 Plastic DIP
MAX480ESA	-40°C to +85°C	8 Narrow SO
MAX480MJA	-55°C to +125°C	8 CERDIP

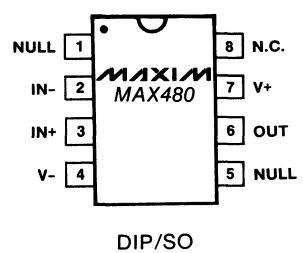
3

Typical Operating Circuit



SINGLE OP AMP FULL-WAVE RECTIFIER

Pin Configuration



High-Precision, Low-Voltage, Micropower Operational Amplifier

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ to V–) ..... ±18V
Internal Power Dissipation 500mW
CERDIP (J) — derate at 8.0mW/°C above +70°C
Plastic DIP (P) — derate at 6.9mW/°C above +70°C
Small Outline (S) — derate at 5.88mW/°C above +70°C
Differential Input Voltage ..... [(V–)-20V] to [(V+)+20V]
Common-Mode Input Voltage .... [(V–)-20V] to [(V+)+20V]
Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range
MAX480 (CPA, CSA) ..... 0°C to +70°C
MAX480 (EPA, ESA) ..... -40°C to +85°C
MAX480MJA ..... -55°C to +125°C
Junction Temperature (T_J) ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: Absolute maximum ratings apply to packaged parts, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±1.5V to ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX480			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			25	70	µV
Input Offset Current	I_{OS}	V_{CM} = 0V		0.2	1	nA
Input Bias Current	I_B	V_{CM} = 0V		1	3	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V R_L = 100kΩ R_L = 10kΩ R_L = 2kΩ	 700 350 125	 1200 600 250		V/mV
		V+ = 5V, V– = 0V, 1V<V_O<4V R_L = 100kΩ R_L = 10kΩ	 200 100	 400 180		
Input Voltage Range	IVR	V+ = 5V, V– = 0V V_S = ±15V (Note 2)	0/4 -15/13.5			V
Output Voltage Swing	V_O	V_S = ±15V R_L = 10kΩ R_L = 2kΩ	 ±14 ±11	 ±14.2 ±12		V
	V_{OH}	V+ = 5V, V– = 0V, R_L = 2kΩ	4.0	4.2		
	V_{OL}	V+ = 5V, V– = 0V, R_L = 10kΩ		100	500	µV
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V, 0V<V_{CM}<4V V_S = ±15V, -15V<V_{CM}<13.5V	90 100	110 130		dB
Power-Supply Rejection Ratio	PSRR			1.0	5.6	µV/V
Slew Rate	SR	V_S = ±15V	5	12		V/ms
Supply Current	I_{SY}	V_S = ±1.5V V_S = ±15V		9 14	15 20	µA
Capacitive Load Stability		A_V = +1 No Oscillations (Note 3)	250	650		pF
Input Noise Voltage	e_{np-p}	f_O = 0.1Hz to 10Hz, V_S = ±15V		3		$µV_{p-p}$
Input Resistance Differential Mode	R_{IN}	V_S = ±15V		30		MΩ
Input Resistance Common Mode	R_{INCM}	V_S = ±15V		20		GΩ

ELECTRICAL CHARACTERISTICS

(V_S = ±1.5V to ±15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

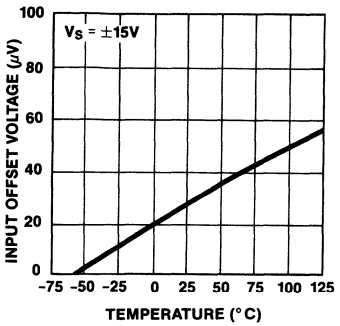
PARAMETER	SYMBOL	CONDITIONS	MAX480C			MAX480E			MAX480M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			40	100		50	150		70	200	µV
Input Offset Voltage Drift	TCV_{OS}			0.3	1.5		0.3	1.5		0.3	1.5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V		0.2	2.0		0.3	2.0		0.5	2.0	nA
Input Bias Current	I_B	V_{CM} = 0V		1	3		2	5		3	7	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V = ±10V R_L = 100kΩ R_L = 10kΩ R_L = 2kΩ	 500 250 75	 950 400 125		 500 250 75	 800 400 150		 225 125 50	 400 240 110		V/mV
		V+ = 5V, V- = 0V, 1V<V_O<4V R_L = 100kΩ R_L = 10kΩ	 150 75	 360 150		 150 75	 280 140		 100 50	 200 110		
Input Voltage Range	IVR	V+ = 5V, V- = 0V V_S = ±15V (Note 2)	0/3.5 -15/13.5			0/3.5 -15/13.5			0/3.5 -15/13.5			V
Output Voltage Swing	V_O	V_S = ±15V R_L = 10kΩ R_L = 2kΩ	 ±13.5 ±10.5	 ±14 ±11.8		 ±13.5 ±10.5	 ±14 ±11.8		 ±13.5 ±10.5	 ±13.7 ±11.5		V
	V_{OH}	V+ = 5V, V- = 0V R_L = 2kΩ	3.9	4.1		3.9	4.1		3.9	4.1		
	V_{OL}	V+ = 5V, V- = 0V R_L = 10kΩ		100	500		100	500		100	500	µV
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V- = 0V, 0V<V_{CM}<3.5V V_S = ±15V, -15V<V_{CM}<13.5V	90 100	110 120		90 100	110 120		85 95	105 115		dB
Power-Supply Rejection Ratio	PSRR			1.0	5.6		1.0	5.6		3.2	10	µV/V
Supply Current	Isy	V_S = ±1.5V V_S = ±15V		12 16	25 30		13 17	25 30		15 19	25 30	µA

Note 2: Guaranteed by CMRR test.
Note 3: Guaranteed by design.

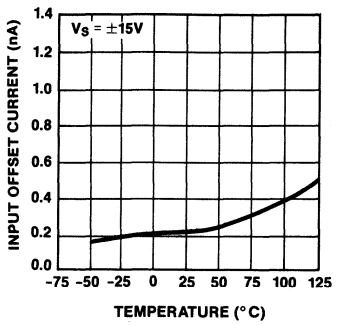
High-Precision, Low-Voltage, Micropower Operational Amplifier

Typical Operating Characteristics

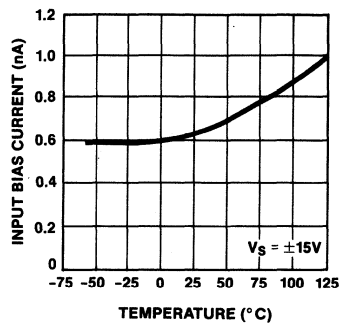
INPUT OFFSET VOLTAGE vs TEMPERATURE



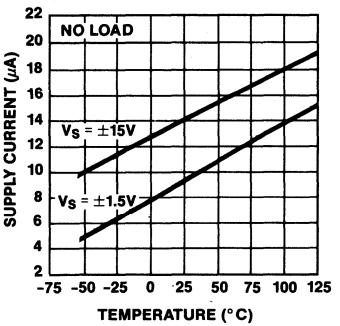
INPUT OFFSET CURRENT vs TEMPERATURE



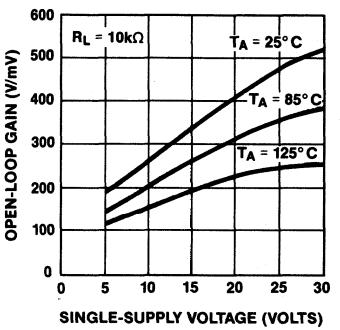
INPUT BIAS CURRENT vs TEMPERATURE



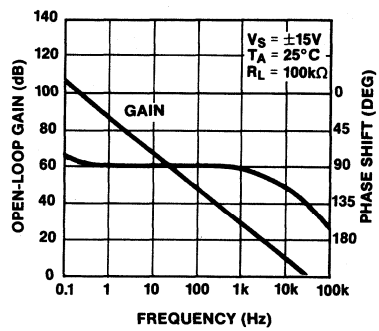
SUPPLY CURRENT vs TEMPERATURE



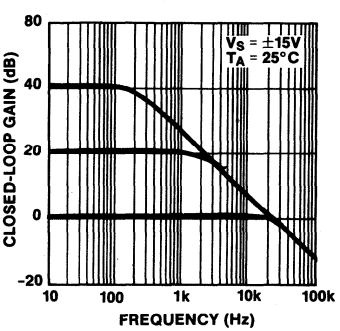
OPEN-LOOP GAIN vs SINGLE-SUPPLY VOLTAGE



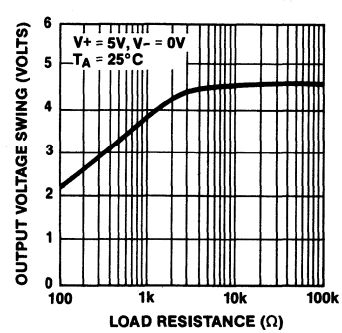
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



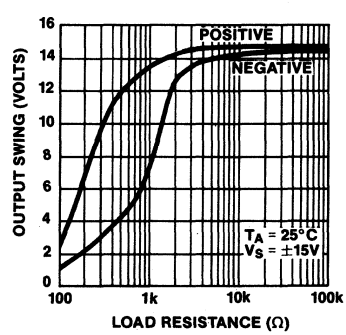
CLOSED-LOOP GAIN vs FREQUENCY



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



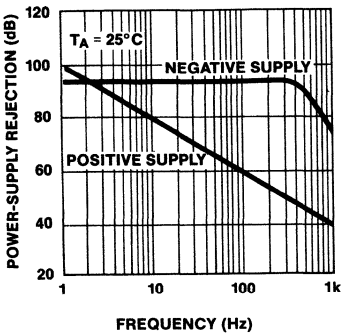
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



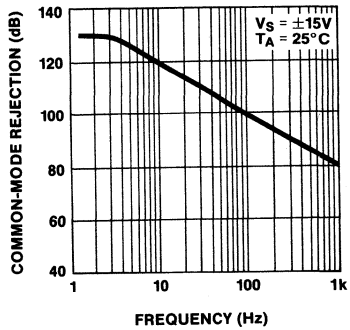
High-Precision, Low-Voltage, Micropower Operational Amplifier

Typical Operating Characteristics (continued)

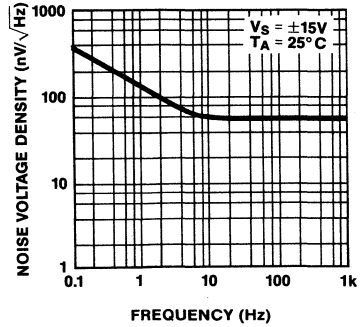
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



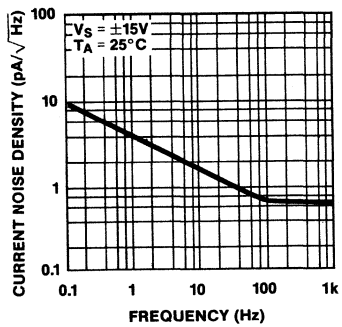
COMMON-MODE REJECTION RATIO vs FREQUENCY



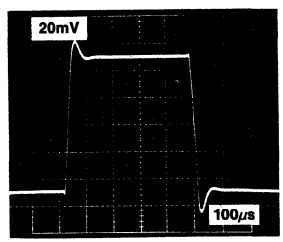
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

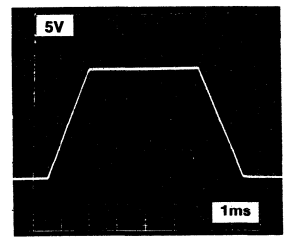


SMALL SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

LARGE SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

High-Precision, Low-Voltage, Micropower Operational Amplifier

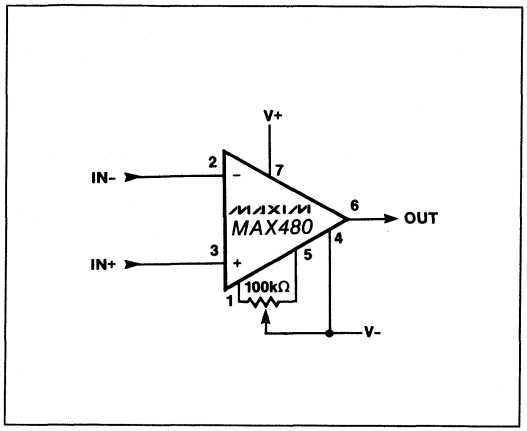


Figure 1. Offset Nulling Circuit

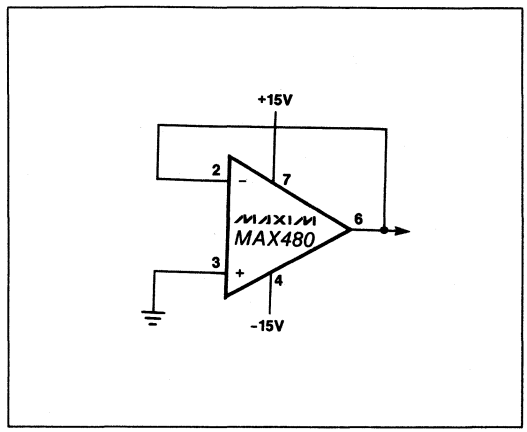


Figure 2. Burn-In Circuit

Power-Supply Circuits

+5V To ±15V DC-DC Converter Delivers 30W

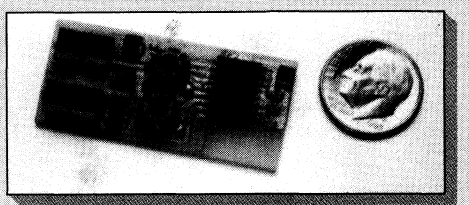
No Design Required—Just Drop It In

The MAX742/MAX743 DC-DC converters provide the simplest means available for generating ±12V or ±15V from a +5V supply. The MAX743, with internal MOSFETs, powers 3 watt loads, while the MAX742, with external MOSFETs, drives 30 watt loads.

These converter ICs offer dramatic price and performance advantages over DC-DC modules. A MAX743, for instance, achieves 78% efficiency while delivering ±100mA and offers 70% efficiency for loads as small ±10mA. The cost of the MAX743 and all major components is $8.20 (1000-up).

The 200kHz operating frequency and use of current-mode pulse-width modulation (PWM) allow use of small, lightweight external components. Inductors, rather than costly custom transformers, generate the positive and negative output voltages. Other features include undervoltage lockout, thermal overload protection, cycle-by-cycle current limiting, and soft-start.

The MAX742/MAX743 switching regulators are well-suited for DC-DC converter module replacement, distributed power systems, computer peripherals, and portable instruments. Printed-circuit layouts are included in the data sheets.



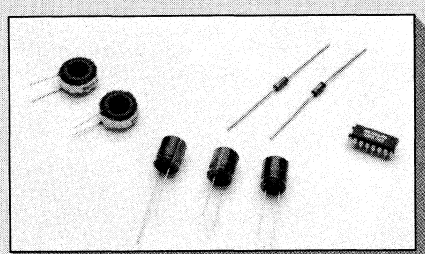
Operating with surface-mount components, the MAX743 DC-DC converter delivers 3W in less than half the board space required by the smallest converter modules. Power density is a high 18W per cubic inch.

Evaluation Kit Simplifies Prototyping

Maxim offers a through-hole evaluation kit (MAX743EVKIT) that considerably shortens breadboarding time for the MAX743. The unassembled kit contains a MAX743, a PC board, and all external components for a 3W dual-output DC-DC converter.

Production Kit Eases Procurement and Increases Reliability

Maxim offers commercial and extended-industrial temperature range production kits (MAX743CPEKIT & MAX743EPEKIT) that make designing with the MAX743 as simple and reliable as plugging in a module. Maxim has carefully selected the critical components and offers these parts in kits that include the MAX743, two low-loss inductors, three low-ESR capacitors, and two power rectifiers. By combining these selected parts with Maxim's proven board layout, you get a guaranteed output-voltage tolerance of ±4% over all temperatures, input voltages, and loads. The commercial temperature range production kit sells for $8.20 (1000-up), less than 1/3 the price of comparable modules.

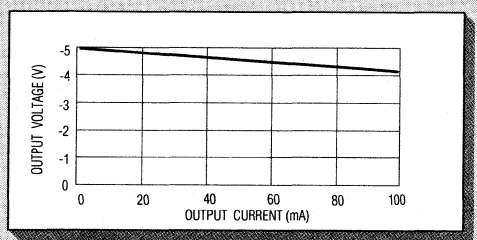


All the major components required for a complete 3 watt, +5V to ±15V or ±12V DC-DC converter can be purchased directly from Maxim in kit form.

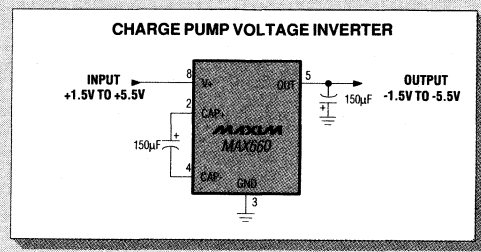
Charge-Pump Voltage Inverter Converts +5V to -5V, Delivers 100mA

High Power Inverter Eliminates Inductors– Uses Only Two Capacitors

Maxim's new MAX660 charge pump voltage inverter converts inputs of +1.5V to +5.5V to negative outputs of -1.5V to -5.5V. The charge pump's 100mA output replaces switching regulators, eliminating the need for inductors and their associated cost, size, and EMI. With a +5V input the MAX660 delivers 100mA at -4.35V.



The MAX660 charge pump voltage inverter delivers 100mA—10 times more current than the ICL7660.



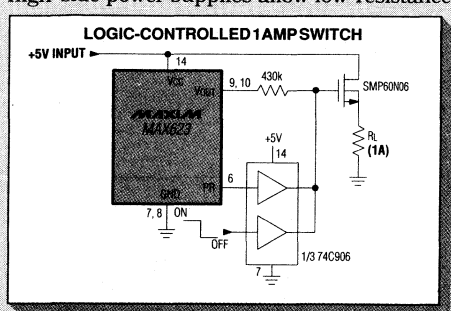
The 100mA-output MAX660 voltage inverter uses two low-cost capacitors, replacing switching regulators and their associated inductors.

The MAX660 comes in 8-pin DIP and SOIC packages. Greater than 90% efficiency, coupled with a typical operating current of only 200µA, provides ideal performance for both battery-powered and board-level voltage conversion. This device can also operate as a voltage doubler; with a +5V input, the MAX660 delivers 100mA at +9.35V.

High-Side Power Supply Allows Low Cost N-Channel MOSFETs

Regulated Charge Pump Boosts V_{IN} by 11V

The MAX622/623 CMOS charge pump converters generate a regulated output voltage 11V greater than the input supply, for powering "high-side" switching and control circuits. The MAX622/623 high-side power supplies allow low-resistance N-Channel MOSFETs to be used in circuits that normally require more-costly, less-efficient P-Channel MOSFETs and PNP transistors. The ICs also allow for the replacement of "logic-level" FETs in low-voltage switching circuits.



The MAX623 regulated high-side supply generates an output of V_{IN} + 11V, useful for controlling N-Channel MOSFETs in load management applications.

Their 50µA typical quiescent current and input range of +3.5V to +16.5V make them suitable for a wide range of line- and battery-powered switching and control applications for which efficiency is critical. These applications include high-side power control with N-Channel MOSFETs, low-dropout voltage regulators, battery-load management circuits, H-switches, and portable computers.

The MAX622 comes in 8-pin DIP and SOIC packages, and requires only three inexpensive external capacitors. The MAX623, in a 16-pin DIP, has the capacitors on chip and requires no external components.

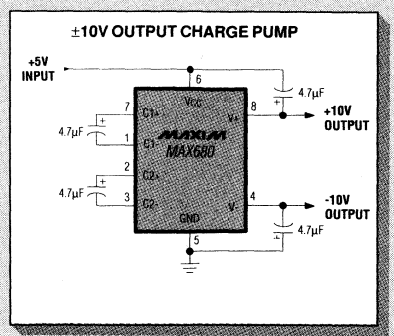
Convert +5V to ±10V with Only Four External Capacitors

Dual-Output Supply Powers 10mA Loads at 85% Efficiency

The MAX680/681 dual-output charge pump voltage converters provide positive and negative output voltages from a single positive supply. They feature 85% power-conversion efficiency and a quiescent current of only 1mA.

The MAX680/681 accept an input voltage of +2V to +6V, and provide an output voltage of ±2 times V_{IN}. The unregulated outputs supply 10mA. The MAX680/681 excel in low-power applications: generating ±10V from +5V supplies, and generating ±6V from +3V lithium batteries. These devices also function as voltage quadruplers, producing a positive or negative 12V output while operating from a lithium cell or other isolated +3V power source.

The MAX680 is useful for generating analog-supply voltages on predominantly digital circuit boards. Local conversion of +5V to ±10V for use by A/D converters, op amps, and other analog functions is far more economical, in low power applications, than routing analog supply voltages throughout the equipment. The MAX680 is available in 8-pin DIP and SOIC. The MAX681 has internal capacitors and is available in a 14-pin DIP package.



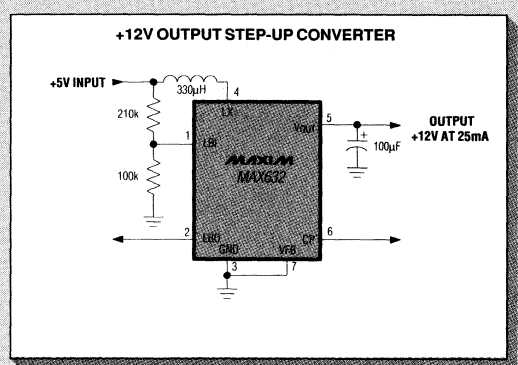
The MAX680 dual-output voltage converter delivers 10mA with 85% efficiency.

300mW Step-Up Converters Feature 87% Efficiency

Complete Solution for Flash EPROM Power Supplies

The MAX631/632/633 step-up converters offer high efficiency and unparalleled design simplicity for 5mW to 500mW applications. Their 135µA quiescent current, high efficiency, and space-saving 8-pin DIP and SOIC packages make the converters an excellent choice for battery-powered and board-level applications. The converters have preprogrammed output voltages of +5V, +12V, and +15V. The output may be set to other levels by adding an external resistor divider.

The MAX631/632/633 are simple to use: add an inductor and capacitor to build a complete power supply. Each converter includes a low-battery detector that monitors the input supply voltage. They also have a charge-pump output for generating additional positive or negative unregulated outputs.

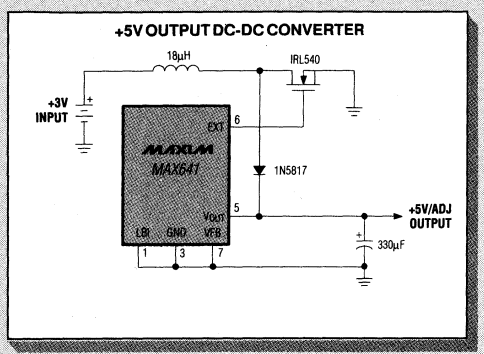


This MAX632 DC-DC converter is designed to operate as a flash-EPROM power supply. It delivers +12V at 25mA with 87% efficiency from a +5V source. The low-battery detector signals when the input voltage falls below +4V.

5W Step-Up Converters Have Low 135µA Supply Current

Switching Regulators Require Only Four External Components

The MAX641/642/643 switching regulators offer efficiency and convenience comparable to that of the MAX631 family and deliver up to 5W. Internal MOSFET drivers are included, and the devices' maximum output power is determined by external components instead of internal power switches. The converters have preprogrammed +5V, +12V, and +15V output voltages, and may be set to other levels with a resistor divider. The MAX641, MAX642 and MAX643 require only four external components: an inductor, diode, power MOSFET, and capacitor.

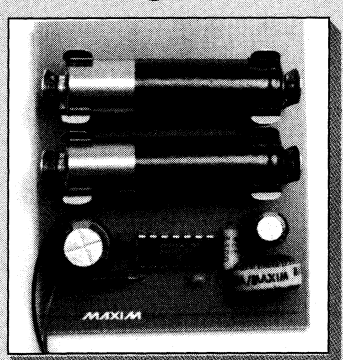


Low quiescent current allows the MAX641 to deliver greater than 80% efficiency over a wide range of load currents.

The low supply current (only 135µA typical in the MAX641) allows these devices to deliver greater than 80% efficiency over a wide range of load currents. In typical applications, the MAX641 provides power to computers, pocket pagers, and other portable equipment by producing +5V from two alkaline cells or a single lithium cell. The MAX641/642/643 provide a +12V/+15V analog supply voltage from a +5V digital supply.

Converters Step-Up to +5V from One or Two Cells

Boost Regulators Feature 1.15V Start-Up and 40µA Standby Mode



The MAX655 Evaluation Kit contains the MAX655 and all necessary components for building a +5V-output switching regulator that operates with two AA cells.

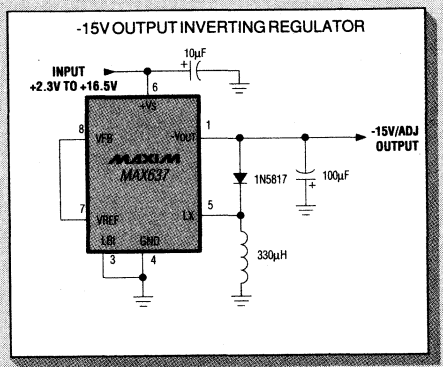
The MAX654-658 DC-DC converters provide a simple and compact means for generating +3V or +5V from one or two alkaline or NiCad cells or a single lithium cell. The MAX654/656/657 guarantee start-up at inputs as low as +1.15V, and they continue to operate even as the supply drops below +1V. The MAX654, with an internal MOSFET switch, supplies up to 40mA at +5V from a single NiCad cell. The MAX656, driving an external MOSFET switch, supplies output currents as high as 250mA from a single NiCad cell. The MAX655/658 are optimized for two-cell operation and are guaranteed to start-up at +1.5V.

An internal, auxiliary, low-power +12V converter provides bootstrapping, which guarantees start-up under load even when your battery is almost completely discharged. In the MAX656/658, this +12V supply also provides load switching via an external MOSFET—further extending battery life and allowing higher output current.

Each device includes a number of features that minimize external components. These include a low-battery detector and a 40µA quiescent current standby mode in which the +5V output supplies up to 500µA. Applications include battery-powered portable equipment, pagers, radios, telephones, remote sensing devices, and hand-held equipment in which size and efficiency are key parameters.

400mW Negative Output Regulators Require Only 4 External Components

Inverters Have Low 80µA Supply Current



The MAX637 inverting switching regulator delivers 400mW.

The MAX635/636/637 inverting DC-DC converters greatly simplify the generation of regulated negative voltages. The ICs require only an external inductor, diode, and two capacitors. 80µA quiescent current, 85% conversion efficiency, and a +2.3V to +16.5V input range simplify the design of battery-powered equipment and board-level DC-DC conversion. The converters deliver 400mW. A low-battery indicator monitors the input voltage. The parts are available in 8-pin DIP and SOIC packages.

The devices are preprogrammed for output voltages of -5V, -12V, or -15V, and may be adjusted to other levels by adding an external resistor divider.

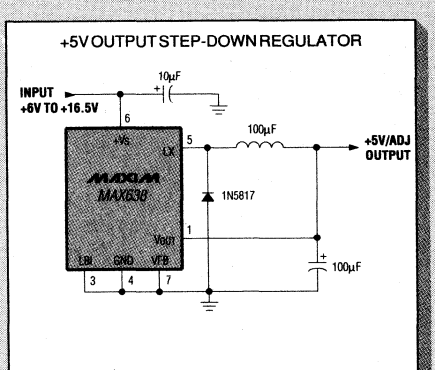
Applications for the MAX635/636/637 include battery- and solar-powered equipment such as test instruments, pocket pagers, laptop computers, and cameras. The converters are also useful in the local generation of negative voltages in line-powered equipment, as an alternative to busing negative voltages throughout the system.

375mW, 85%-Efficient Converter Steps-Down to +5V

135µA Quiescent Current and Adjustable Output

The MAX638 DC-DC step-down converter features 85% typical efficiency and minimal external components. You can design a high-efficiency regulated power supply by adding a diode, a low-cost inductor, and two capacitors. The MAX638 output voltage is preset to +5V and may be set to other voltages with an external resistor divider. With a +12V input, the device provides 75mA at +5V with 85% efficiency. A typical linear regulator, performing this function, dissipates over 1/2W with a conversion efficiency of only 42%.

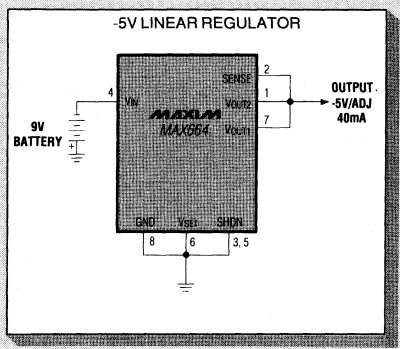
The MAX638 consumes only 135µA of quiescent current, making it well-suited for battery-operated equipment. An adjustable low-battery indicator is included on-chip. Applications include the efficient generation of +5V from +9V batteries, such as in portable instruments, pocket pagers, laptop computers, and mobile phones. The MAX638 is also valuable for on-card voltage conversion, as an alternative to busing multiple voltages throughout a line-powered system. The MAX638 is available in 8-pin DIP and SOIC packages.



The 85%-efficient MAX638 step-down converter extends battery life by offering much higher efficiency than linear regulators.

Linear Voltage Regulators Have 12µA Supply Current

Micropower Regulators Power 40mA Loads



The MAX664 linear voltage regulator has a low 12µA quiescent current.

The MAX663/664/666 are linear voltage regulators with very low quiescent current (12µA maximum). The MAX663/666 are positive regulators with a preset output of +5V, and the MAX664 negative regulator has a preset output of -5V. The output of the regulators may be set to any value between +1.3V and +15V (MAX663/666) or -1.3V to -15V (MAX664) using two external resistors. The MAX666 features an on-chip low-battery detector.

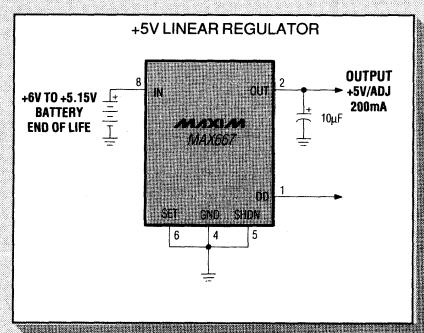
These regulators have an input range of +2V to +16.5V (MAX663/666) or -2V to -16.5V (MAX664) and an output capability of 40mA. They provide output-current limiting, shutdown, and a low (1V at 40mA typical) differential between the input and output voltages. The MAX663 has a temperature-proportional output whose temperature coefficient is +2.5mV/°C. This output is commonly used to generate temperature-compensated voltages for biasing multiplexed LCD displays.

Low-Dropout Linear Regulator Powers 200mA Loads With 150mV Dropout Voltage

1µA Maximum Shutdown Supply Current

The MAX667 is a low-dropout linear regulator with a preset output voltage of +5V. It delivers 200mA at +5V with an input of as low as +5.15V—a useful capability in +5V systems powered by 5-cell NiCad or 3-cell lead-acid batteries. The regulator is capable of supplying up to 250mA.

The MAX667 features a low-power shutdown mode in which supply current is cut to 1µA maximum. In normal mode, the no-load supply current is typically 20µA. The MAX667 operates as a fixed +5V regulator, or its output can be adjusted from +1.3V to +16V using two external resistors. In the fixed +5V mode, the output voltage is guaranteed to within ±4% over temperature. The regulator has a "dropout" indicator that signals when the internal series-pass PNP transistor is about to saturate. The MAX667 also features on-chip low-battery detection.



When powered with 5 NiCad cells, the MAX667 provides a regulated +5V output at 200mA even down to a 5.15V (fully discharged) input.

Part Number	Input Voltage (V)	Output Voltage (V)	Quiescent Supply Current (mA) max (typ)	Package* Options	Temp** Range	Comments	Price† 1000-up ($)
DUAL OUTPUT: STEP-UP/INVERTING SWITCHING REGULATORS							
MAX743	4.2 - 6.0	±12, ±15	30 (20)	DIP, SO	C, E, M	Internal power MOSFETs, evaluation kit and production kit available, 3W output	5.82
MAX742	4.2 - 6.0	±12, ±15	15 (8)	DIP, SO	C, E, M	Drives external MOSFETs, 30W output	5.82
LOW-POWER BOOST SWITCHING REGULATORS							
MAX630	2.0 - 16.5	$V_{OUT} > V_{IN}$	0.125 (0.070)	DIP, SO	C, E, M	Improved RC4193 2nd source	2.88
MAX4193	2.4 - 16.5	$V_{OUT} > V_{IN}$	0.200 (0.090)	DIP, SO	C, E, M	Improved RC4193 2nd source	1.74
MAX631	1.5 - 5.6	+5, Adj.	0.4 (0.135)	DIP, SO	C, E, M	Only 2 external components	2.45
MAX632	1.5 - 12.6	+12, Adj.	2.0 (0.5)	DIP, SO	C, E, M	Only 2 external components	2.45
MAX633	1.5 - 15.6	+15, Adj.	2.5 (0.75)	DIP, SO	C, E, M	Only 2 external components	2.45
HIGH-POWER BOOST SWITCHING REGULATORS							
MAX641	1.5 - 5.6	+5, Adj.	0.4 (0.135)	DIP, SO	C, E, M	Drives external MOSFET	2.45
MAX642	1.5 - 12.6	+12, Adj.	2.0 (0.5)	DIP, SO	C, E, M	Drives external MOSFET	2.45
MAX643	1.5 - 15.6	+15, Adj.	2.5 (0.75)	DIP, SO	C, E, M	Drives external MOSFET	2.45
LOW-VOLTAGE BOOST SWITCHING REGULATORS							
MAX654	1.15 - 5.6	+5	(0.08)	DIP, SO	C, E, M	Optimized for 1 cell	3.35
MAX655	1.5 - 5.6	+5	(0.04)	DIP, SO	C, E, M	Optimized for 2 cells, evaluation kit available	3.35
MAX656	1.15 - 5.6	+5	(0.08)	DIP, SO	C, E, M	Drives external MOSFET	3.35
MAX657	1.15 - 3.6	+3	(0.08)	DIP, SO	C, E, M	Optimized for 1 cell	3.35
MAX658	1.5 - 5.6	+5	(0.04)	DIP, SO	C, E, M	Drives external MOSFET	3.35
INVERTING SWITCHING REGULATORS							
MAX634	2.3 - 16.5	up to -20	0.15 (0.07)	DIP, SO	C, E, M	Improved RC4391 2nd source	2.61
MAX4391	4.0 - 16.5	up to -20	0.25 (0.09)	DIP, SO	C, E, M	Improved RC4391 2nd source	2.28
MAX635	2.3 - 16.5	-5, Adj.	0.15 (0.08)	DIP, SO	C, E, M	Only 3 external components	2.45
MAX636	2.3 - 16.5	-12, Adj.	0.15 (0.08)	DIP, SO	C, E, M	Only 3 external components	2.45
MAX637	2.3 - 16.5	-15, Adj.	0.15 (0.08)	DIP, SO	C, E, M	Only 3 external components	2.45

–Continued on the next page–

* Package Options: DIP = Dual-In-Line Package; SO = Small Outline; TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C; E = -40°C to +85°C; M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

DC/DC Converters (continued)

Part Number	Input Voltage (V)	Output Voltage (V)	Quiescent Supply Current (mA) max (typ)	Package* Options	Temp** Range	Comments	Price† 1000-up ($)
HIGH-VOLTAGE INVERTING SWITCHING REGULATORS							
MAX650	-10 to -56	+5	(0.85)	DIP, SO	C, E, M	Optimized for telecom applications	3.39
STEPDOWN SWITCHING REGULATORS							
MAX638	2.6 - 16.5	+5, Adj.	0.6 (0.135)	DIP, SO	C, E, M	Only 3 external components	2.45
CHARGE-PUMP CONVERTERS—UNREGULATED							
MAX660	1.5 - 5.5	+2 x V_{IN}, -V_{IN}	1.0 (0.6)	DIP, SO	C, E, M	I_{OUT} = 100mA	2.95
MAX680	2.0 - 6.0	± 2 x V_{IN}	2 (1)	DIP, SO	C, E, M	4 external capacitors	1.87
MAX681	2.0 - 6.0	± 2 x V_{IN}	2 (1)	DIP	C, E	No external components	4.64
ICL7660	1.5 - 10	-V_{IN}	0.175 (0.110)	DIP, SO, TO-99	C, E, I, M	Not regulated	1.34
ICL7662	4.5 - 20	-V_{IN}	0.6 (0.25)	DIP, SO, TO-99	C	Not regulated	1.80
Si7661	4.5 - 20	-V_{IN}	2 (0.3)	DIP, SO, TO-99	C	Not regulated	2.00
CHARGE-PUMP CONVERTERS—REGULATED HIGH-SIDE POWER SUPPLIES							
MAX622	3.5 - 16.5	V_{IN} + 11V	0.5 (0.07)	DIP, SO	C, E	3 external capacitors	1.99
MAX623	3.5 -1 6.5	V_{IN} + 11V	0.5 (0.07)	DIP	C, E	No external capacitors	3.95

MOSFET Drivers

Part Number	Output Resistance (Ω) max (typ)	Rise/Fall T_A = +25°C (ns) max	Rise Time Over Temp (ns) max	Fall Time Over Temp nsec max	Supply Voltage (V)	Package* Options	Temp** Range	Comments	Price† 1000-up ($)
MAX626	15 (4)	30	40	40	4.5 to 18	DIP, SO	C, E, M	Dual Inverting	1.57
MAX627	15 (4)	30	40	40	4.5 to 18	DIP, SO	C, E, M	Dual Non-Inverting	1.66
MAX628	15 (4)	30	40	40	4.5 to 18	DIP, SO	C, E, M	Inverting and Non-Inverting	1.66
TSC426	15 (10)	30	60	40	4.5 to 18	DIP, SO	C, I, M	Dual Inverting	1.06
TSC427	15 (10)	30	60	40	4.5 to 18	DIP, SO	C, I, M	Dual Non-Inverting	1.15
TSC428	15 (10)	30	60	40	4.5 to 18	DIP, SO	C, I, M	Inverting and Non-Inverting	1.15
ICL7667	See MAX626								

* Package Options: DIP = Dual-In-Line Package; SO = Small Outline; TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C; E = -40°C to +85°C; M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Linear Voltage Regulators

Part Number	Input Voltage (V)	Output Voltage (V)	Dropout Voltage	Quiescent Current (µA) max (typ)	Output Voltage Accuracy	Shutdown	Package* Options	Temp** Range	Price† 1000-up ($)
AC-DC REGULATORS									
MAX610	110/220VAC	Fixed +5 or +1.3 to +9	N/A	150 (70)	±4%	NO	DIP	C	2.58
MAX611	110/220VAC	Fixed +5	N/A	150 (70)	±4%	NO	DIP	C	2.58
MAX612	6 to 9 VAC	Fixed +5 or +1.3 to +9	N/A	150 (70)	±4%	NO	DIP	C	2.58
DC LINEAR REGULATORS - POSITIVE OUTPUT									
MAX663	+2 to +16.5	Fixed +5 or +1.3 to +15	1.5V @ 40mA	12 (6)	±5%	YES	DIP, SO	C, E, M	1.91
MAX666	+2 to +16.5	Fixed +5 or +1.3 to +15	1.5V @ 40mA	12 (6)	±5%	YES	DIP, SO	C, E, M	2.13
MAX667	+3.5 to +16.5	Fixed +5 or +1.3 to +15	0.3V @ 100mA	25 (12)	±5%	YES	DIP, SO	C, E, M	2.35
ICL7663	+1.5 to +16	+1.3 to +15	1.5V @ 40mA	10 (4)	±8%	YES	DIP, SO, TO-99	C, E, I	1.81
ICL7663A	+2.0 to +16	+1.3 to +15	1.5V @ 40mA	10 (4)	±1%	YES	DIP, SO, TO-99	C, E, I	1.99
ICL7663B	+1.5 to +16	+1.3 to +15	1.5V @ 40mA	10 (4)	±8%	YES	DIP, SO, TO-99	C, E, I	1.81
DC LINEAR REGULATORS - NEGATIVE OUTPUT									
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	1.5V @ 40mA	12 (6)	±5%	YES	DIP, SO	C, E, M	2.32
ICL7664	-2 to -16	-1.3 to -15	0.4V @ 30mA	10 (3.5)	±5%	YES	DIP, SO, TO-99	C, I	2.21
ICL7664A	-2 to -16	-1.3 to -15	0.4V @ 30mA	10 (3.5)	±1%	YES	DIP, SO, TO-99	C, I	2.65

* Package Options: DIP = Dual-In-Line Package; SO = Small Outline; TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C; E = -40°C to +85°C; M = -55°C to +125°C
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APPLICATION NOTE

MAXIM

A Designer's Guide to Maxim DC-DC Converters

Important Parameters in Power Supply Design: A Discussion of Key DC-DC Specifications

Maxim's DC-DC converter products target miniature on-card power supplies and battery-operated applications rather than heavy-duty supplies. Maxim offers solutions for extracting the last bit of useful energy from a dying NiCad cell or for squeezing a flash-EPROM programming supply onto a square inch of surface-mount board. For tips on low-power DC-DC designs and applications read on.

DC Accuracy

Output voltage accuracy specs include initial accuracy, load regulation, line regulation, and output-voltage drift due to temperature and time. Output-voltage accuracy is important because designers often rely on it for stable bias and reference voltages. Also, if DC levels at an equipment interface differ by more than a diode drop, large parasitic-diode currents may flow in the interface chips.

Maxim's capability for laser-trimming thin-film resistors serves as a routine and cost-effective means for adjusting active parameters in all types of ICs. For power-supply ICs, the commonly trimmed parameters include bias current, oscillator frequency, reference voltage and output voltage. Trimming not only assures DC accuracy; it provides consistent AC characteristics and a tight distribution for parameters such as the current-limit threshold level.

AC (Transient) Performance

Transient response is often overlooked in the design of power supplies, but it can be as important in some applications as DC accuracy. Bad transient response can compromise reliability, as demonstrated in the response of a low cost "generic" modular power supply (Figure 1). The overshoot in the output of this module—6V above the normal 5V output—will likely be high enough to destroy logic ICs.

An easy way to look at a circuit's transient performance is to step the load current from zero to full load—using an oscilloscope, a dummy load, and an NPN-transistor switch driven by a square-wave generator. Simply hook the switch between ground and the ground side of the load, and monitor the output voltage for overshoot and ringing. The circuit's AC compensation should provide a nice damped response (Figure 2), but avoid overdamping which allows output overshoots during power-up and during short-circuit recovery.

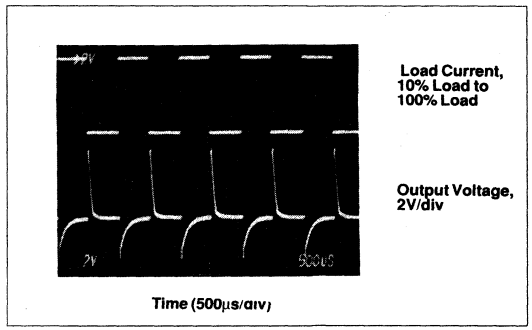


Figure 1. Load-transient response for a "Brand X" DC-DC converter shows high overshoot.

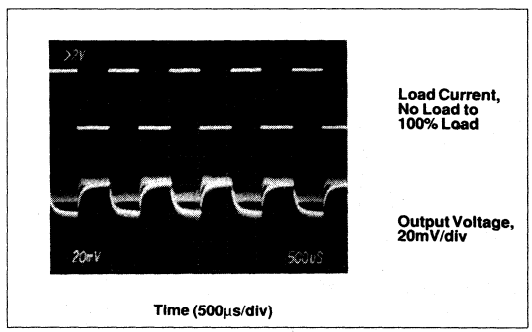


Figure 2. Properly compensated MAX742 regulator exhibits an RC-type damped response. ("Ghost" trace is due to switching ripple).

Output Noise and Reflected Ripple

Output noise is important for its effect on the system noise margins and on the performance of precision analog components. High-quality ceramic or low-ESR electolytic capacitors for both input and output filtering are crucial to noise reduction. Cheap output-filter capacitors can lower costs, but you must then expect more output ripple.

Output noise in a simple step-up, pulse-width modulation (PWM) regulator (Figure 3) takes several forms:

1) The most significant noise mechanism is the IR drop through the output filter capacitor's ESR (equivalent series resistance), which is caused by current pulses from the inductor.

2) Switching noise in the form of short spikes riding on the DC waveform has several sources: the filter capacitor's

A Designer's Guide to Maxim DC-DC Converters

equivalent series inductance (ESL), current spikes in the ground trace, rectifier turn-on transients, and extraneous EMI (electro-magnetic interference) picked up by the oscilloscope's ground lead.

3) The RC discharge of filter capacitor to load resistor, often undetectable, is seldom significant for converters operating above 20kHz.

An inductor in series with the output voltage is effective in eliminating switching spikes, even if the "inductor" is only a long PC trace terminated with a ceramic capacitor. To eliminate the output ripple's lower-frequency fundamental component as well, you must set the natural frequency of this LC output filter lower than the switching frequency (at least 10 times lower, preferably).

Reflected ripple is also important—it appears to originate in the source voltage that powers a DC-DC converter, but it's actually caused by the switching currents that are drawn by the converter circuit and passed through the

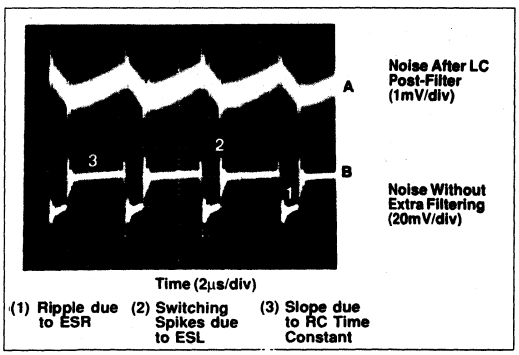


Figure 3. Noise mechanisms in a 200kHz buck-boost converter.

power-source impedance. Excessive noise on the supply bus often points to inadequate filtering at the DC-DC converter's input. If the input bypass capacitor is inadequate, a choke inductor can be placed in series with the input to provide better filtering. Avoid high-resistance chokes that will have excessive IR losses.

Maxim makes both PWM and PFM (pulse-frequency modulation) switching-regulator ICs. Most of the MAX6XX series are PFM types, including the MAX630 through MAX642 and the MAX654 family. Most of the MAX7XX series are PWMs, including the MAX730 family and the MAX742/743.

Most PWMs switch the power transistor at a fixed frequency without missing pulses. PFM controllers can skip pulses, switching less often, and thus require less supply

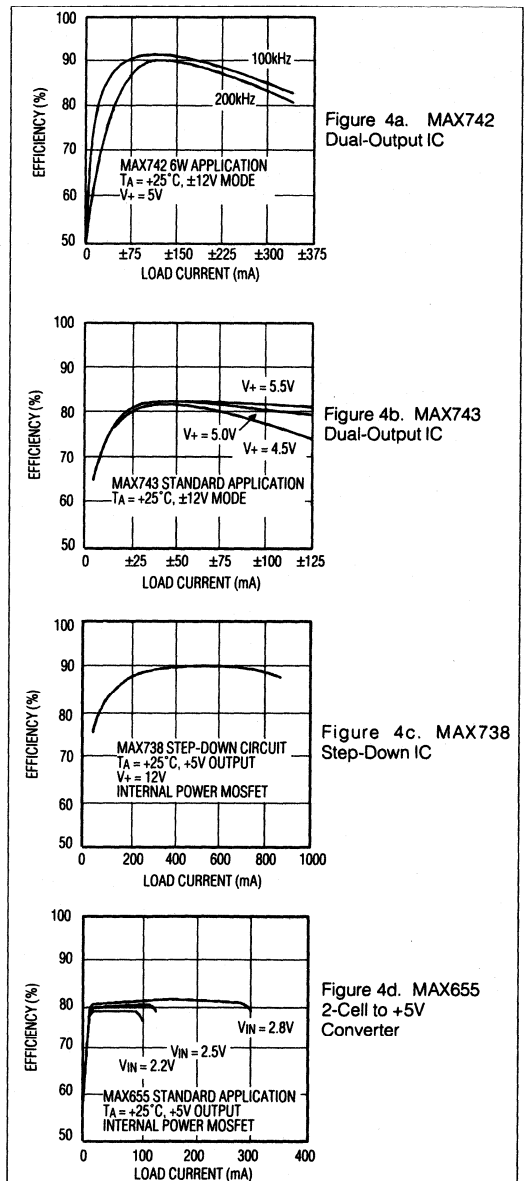


Figure 4a. MAX742 Dual-Output IC

Figure 4b. MAX743 Dual-Output IC

Figure 4c. MAX738 Step-Down IC

Figure 4d. MAX655 2-Cell to +5V Converter

Figure 4. Efficiency vs. load current varies as shown for different part types.

current, but in doing so they produce low-frequency noise that is difficult to filter. These differences lead to the fundamental trade-off between PWMs and PFMs: supply current vs. noise. In general, PWMs are best for applications of high output power or low output noise, and PFMs suit low-power (under 5W) or battery-powered applications.

Efficiency and Quiescent Current

Power efficiency—the ratio of output power to input power—is obviously critical in battery-powered applications. Even when deriving power from a wall socket, high efficiency can minimize heat build-up and eliminate bulky heatsinks. But selecting DC-DC converters based on their rated efficiency specs can be tricky—many products invite unrealistic assumptions by specifying efficiency at a single load current. To make a fair comparison of such products, inspect their efficiency at various operating points (Figure 4a-4d).

Linear regulators, for example, often regarded as inefficient because their regulating mechanism dissipates power, actually excel in many battery-powered systems because they draw very little quiescent current.

Some linear regulators maintain a regulated output while drawing as little as 20µA (Figure 5). No switching-regulator can match that performance. Thus, for applications that require a keep-alive voltage in the standby mode, linear regulators offer efficiency and simplicity (no magnetics).

They also excel as multiple regulators in load-management systems (Figures 6, 7).

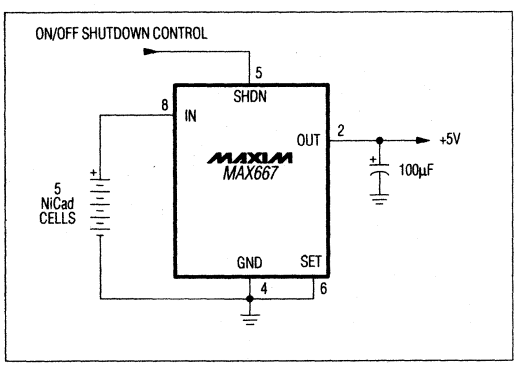


Figure 5. This low-dropout regulator circuit consumes only 20µA of quiescent current while supplying a +5V regulated output. In shutdown it draws only 0.2µA of quiescent current.

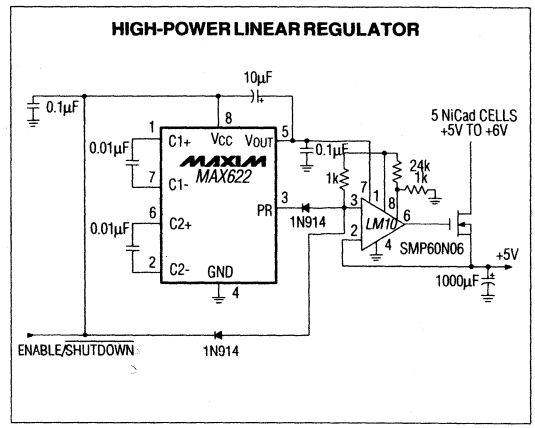


Figure 6. To drive (indirectly) the gate of an N-channel MOSFET source follower, this circuit's high-side regulated charge-pump IC (MAX622) generates a regulated DC voltage 11V higher than the input. The LM10 amplifier provides a reference and error-amplifier.

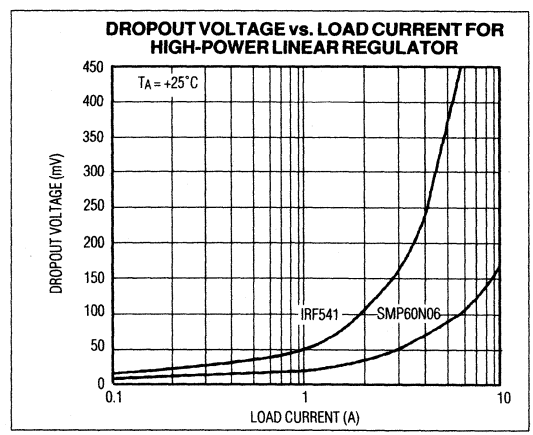


Figure 7. Extremely low dropout (less than 100mV at I_{LOAD} = 5A) enables this linear regulator to extract nearly all the energy from a stack of five NiCad cells.

Input Voltage Range

Though 2:1 or less is a typical max/min ratio for the input range of a regulator (lower ratios ease the design problem), many ICs from Maxim can operate over a range of 8:1 or more. The MAX641, for instance, can accept inputs between 1.8V and 16V.

A Designer's Guide to Maxim DC-DC Converters

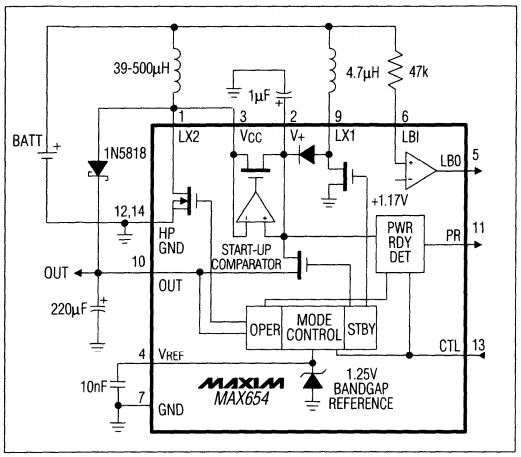


Figure 8. Designed for powering +5V logic in portable equipment such as pagers and remote data-collection systems, the MAX654 converts the output of one or two battery cells to outputs of +5V and +12V, with 82% efficiency.

A wide dynamic range is not the only issue when considering input voltage range. Also important is operation at the low end of the specified range. The MAX667 of Figure 5, for example, relies on low dropout voltage (the minimum input-output voltage differential) in determining end-of-life voltage for the battery. Extremes of the input-voltage range are important for switch-mode regulators as well, as illustrated by the low-voltage MAX654 and its relatives (Figure 8). The MAX654 cuts the size and weight of battery packs by generating +5V at 40mA from just one NiCad cell.

Charge pumps are also effective in low-voltage regulator applications (Figure 9). This circuit converts the output of a lithium cell to +5V at 100mA. Besides eliminating the inductor associated with switching regulators, the circuit capitalizes on the low dropout voltage of the MAX667 and the low input-voltage range and high current of the MAX660 (big brother to the popular ICL7660).

Miniaturization

As a system shrinks, power supply components occupy a greater percentage of the available space, which draws attention to these components and provides designers with a motivation to reduce their size. The need for size reduction often justifies compromises in efficiency, operating temperature range, output ripple and EMI.

Maxim DC-DC converters provide many choices in making such tradeoffs, allowing the designer to zero in on the

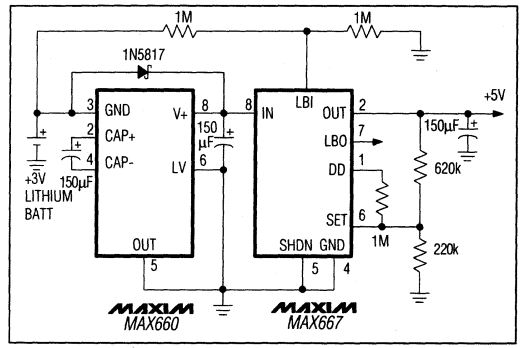


Figure 9. A MAX660 charge pump configured as a voltage doubler produces an output that varies from +6V to +5.15V over the life of the battery. This output, regulated to +5V by the MAX667 low-dropout regulator, supplies 40mA for more than 12 hours from a DL123A lithium cell.

optimum solution. Take a +5V to -5V regulator for a computer peripheral card as an example. Since it ultimately derives its power from a 117V wall outlet, efficiency is probably unimportant. However, in most computer gear, size is critical. This application would therefore be better served by a low-efficiency regulated charge pump, where tiny capacitors replace a bulky inductor.

Some power supply circuits, however, require magnetics to achieve galvanic isolation or high input/output ratios. Coiltronics' CTX-series parts are shown in the MAX655 and MAX742 SMT-board photos of Figures 10, 12. To obtain PC artwork and a parts list for these SMT applications, call Maxim Applications at (408) 737-7600.

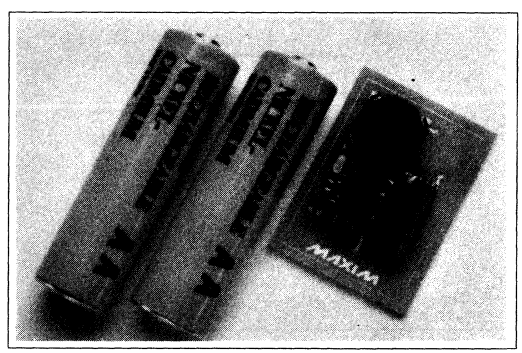


Figure 10. This MAX655 surface-mounted power supply features compact and high-energy SMT inductors.

A Designer's Guide to Maxim DC-DC Converters

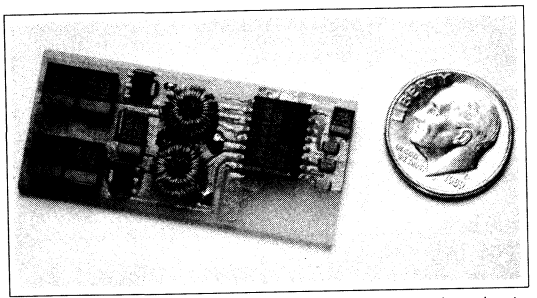


Figure 11. The MAX743's "web" type lead frame conducts heat from the IC through four center package leads, allowing the device to deliver its 3W dual rated output over the operating temperature range, in a SMT package.

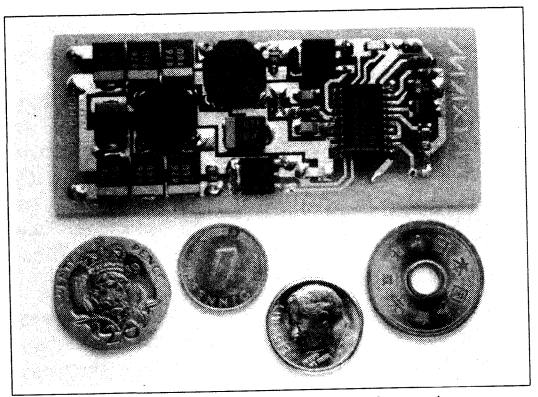


Figure 12. External power transistors and hefty passive components enable this MAX742 SMT board to provide 10W, 90% efficient, regulated dual outputs in only 3.0 in^2 of real estate.

Minimum Component Count

Reducing the component count in a circuit brings manifold benefits, including increased reliability, reduced assembly costs, and reduced board space. Therefore, any external component associated with a Maxim IC represents a lot of effort and discussion (and often a battle) during the IC's development cycle.

Some Maxim DC-DC converters, such as the MAX681 dual-output charge pump, require no external components at all. Others, such as the MAX743 dual-output PWM switching regulator, require magnetic components, available in production quantities from Maxim. Even simpler than the MAX743 is the MAX632 boost (step-up) switching regulator (Figure 13), which functions as a flash-EPROM supply using only two external components.

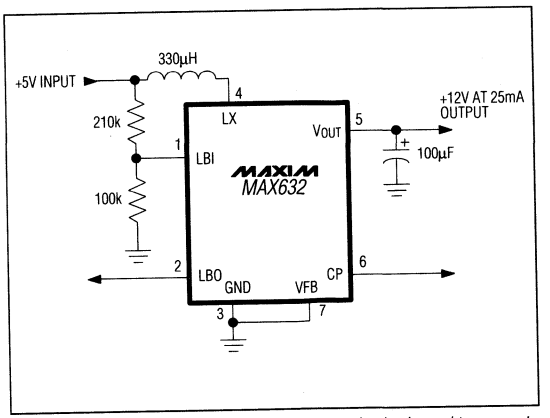


Figure 13. This MAX632 DC-DC converter is designed to operate as a flash-EPROM power supply. It delivers +12V at 25mA with 87% efficiency from a +5V source. The optional resistors are used to set the low-battery detector to signal when the input voltage falls below +4V.

Simple Design Procedures

Chip designers at Maxim have an unwritten law—no customer should need a PhD in the theory of switching regulators just to build a DC-DC converter on a system card. But customers want flexible designs. Sometimes they need a custom development, and often they prefer a state-of-the-art product. Balancing these diverse needs is Maxim's task as an IC supplier, while competing with the makers of one-size-fits-all modular DC-DC converters.

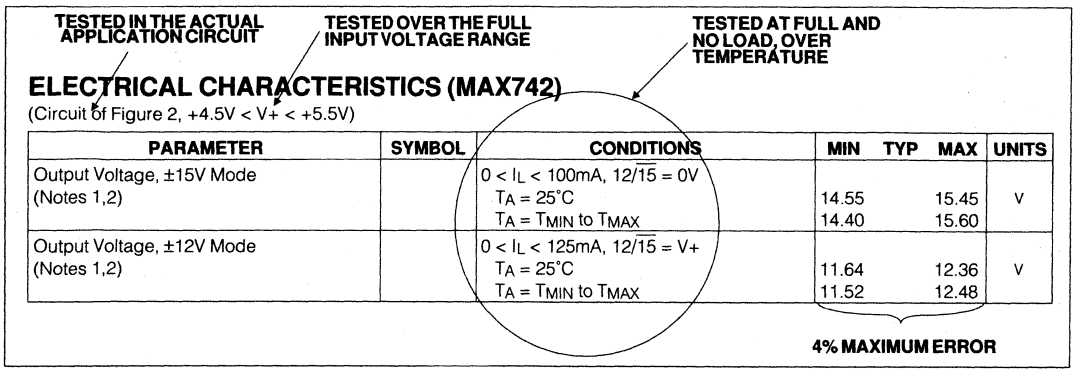
One way to simplify the design task is by offering canned-solution ICs with guaranteed performance for one or more mainstream applications. Small external-circuit changes can suit such chips to a wide range of applications, and the designer is assured that such Maxim ICs have been tested in an actual regulator similar to his own.

In-Circuit Testing Guarantees Performance

In-circuit testing means that a DC-DC converter is tested as a complete system; not as a collection of blocks. Though more difficult than testing the parameters of each block, the in-circuit test corresponds to actual use of the IC, and helps to weed out any parts with transient problems (Figure 14).

Another aid to designers is the ready availability of specialized external components such as low-ESR capacitors and high-Q inductors. Without them, prototype

A Designer's Guide to Maxim DC-DC Converters



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage, ±15V Mode (Notes 1,2)		0 < I_L < 100mA, 12/$\overline{15}$ = 0V				
		T_A = 25°C	14.55		15.45	V
		T_A = T_{MIN} to T_{MAX}	14.40		15.60	
Output Voltage, ±12V Mode (Notes 1,2)		0 < I_L < 125mA, 12/$\overline{15}$ = V+				
		T_A = 25°C	11.64		12.36	V
		T_A = T_{MIN} to T_{MAX}	11.52		12.48	

Figure 14. ***In-Circuit Testing Example*** *This specification is reprinted from the data sheet of a MAX742 switching-regulator IC. In-circuit testing assures high performance for the device, without an extensive worst-case design analysis.*

development could be delayed by the four-to-eight-week sample lead time offered by most suppliers of such parts. Maxim provides evaluation kits, production kits for volume manufacture, and samples of certain key components for rush prototyping. The evaluation kit simplifies the process of breadboarding and designing-in by providing a complete regulator circuit—the PC board, the IC, and all external components (Figures 15, 16). (These same external components are used for Maxim's in-circuit testing).

Reliability

Most DC-DC converter ICs fail from overvoltage or overcurrent stresses rather than excess power dissipation. Of the few chip failures observed in Maxim's Failure Analysis department, most were obvious cases of overvoltage (rupture of a thin dielectric or pn junction) or overcurrent (electromigration of the aluminum interconnect layer or bond wires) applied to the devices. In unusual cases, the IC had tell-tale signs of excess power—vast areas were blackened and destroyed.

These observations offer a lesson: The *Absolute Maximum Ratings* Section is the most important part of a data sheet. Working designs whose ICs run cool may nevertheless be in trouble if instantaneous currents exceed their ratings. Electromigration due to these current spikes can gradually erode the aluminum layer in such circuits.

The key to preventing this type of failure is an understanding of the forces at work. Peak currents in a switching regulator, for example, which depend on several operating conditions, may be well in excess of the DC load current. To relate these operating conditions to the max ratings table you must calculate component stresses for the regulator in question. Most of the switching-regulator data sheets from Maxim contain concise sets of worst-case design procedures for just that purpose.

DC-DC Reliability Tips

- Flog your design in the laboratory. Raise it to high temperature and then short the output, first to ground and then to the input. Increase the input voltage until smoke appears and then examine the circuit to see what fried. Punish it without mercy. Better to do it now, because field service technicians and others will certainly do it later.
- Tantalum capacitors are easily ruined by overvoltage and often short circuit upon failure; you should therefore derate tantalum filter capacitors by a minimum of double the nominal voltage (i.e., use 10V capacitors in a 5V circuit). Where drastic derating is not possible or in circuits that exhibit excessive transient spikes, add a zener clamp across the capacitor.
- Check for overvoltage transients under conditions of start-up and short-circuit recovery. Perhaps the worst thing a DC-DC converter can do is to produce an overvoltage that destroys everything downstream.

Multiple Outputs

Transformers, charge-pump taps, and multiple controllers are among the methods for generating multiple outputs from a switching regulator. The classic method involves multiple windings on a transformer and is very effective for designs that reach high-volume production or feature high levels of power. Either condition can justify the extra complexity of a transformer-based design.

Transformer drawbacks include poor regulation and the power loss resulting from less-than-perfect magnetic

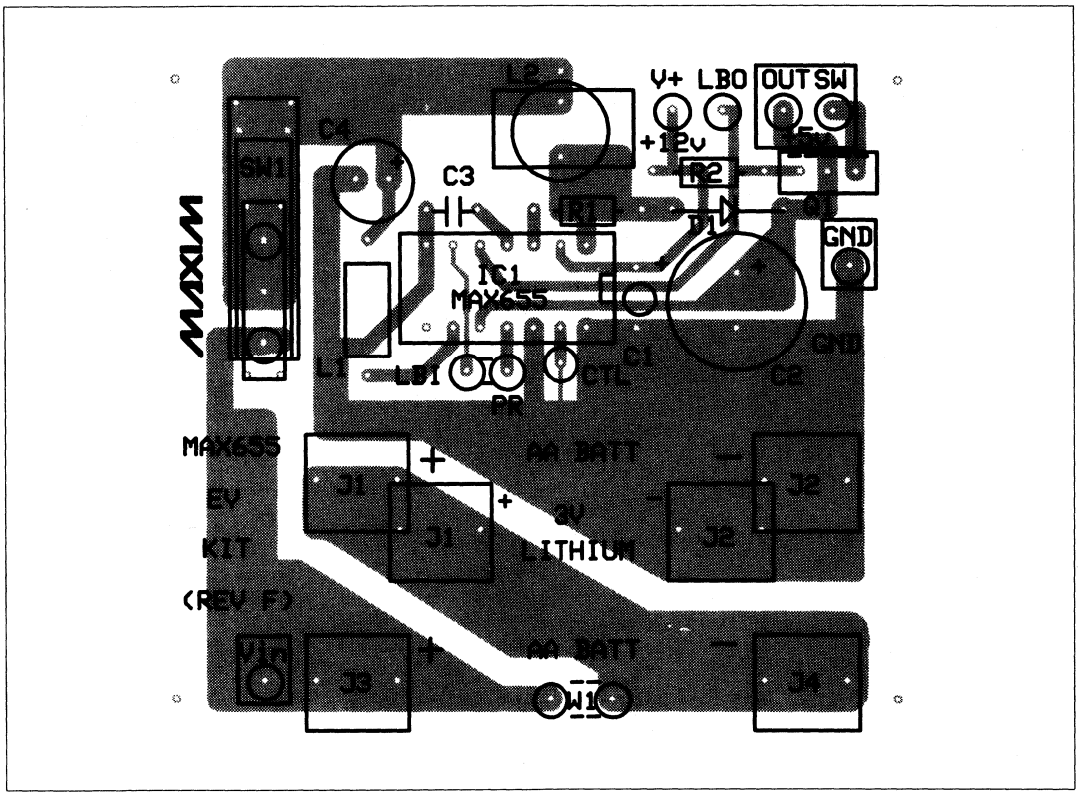


Figure 15. ***MAX655 Evaluation PC Board Layout*** *Designed for portable microprocessor-based systems and other battery-operated circuits, the MAX655 delivers +5V at 100mA with 82% efficiency from a 2-cell voltage source. The chip includes a +12V, low-current, high-side supply for load-switching applications. Standby current is 80µA.*

coupling. Without additional regulation by mag-amp reactors or linear post regulators, transformer-based designs are subject to problems of cross-regulation: one output voltage can be affected by load changes at another output.

Multiple-output switching regulators, on the other hand, require more active circuitry, but their independently regulated outputs are not subject to cross-regulation problems or efficiency loss due to post regulation.

You can implement a load-switching technique if multiple outputs have the same voltage. You could, for example, control a number of loads by combining a MAX622 regulated charge pump with a level-translator chip and external MOSFETs (Figure 17). High-side control in this circuit allows the use of N-channel MOSFETs, which, for a given value of on-resistance are much less expensive than the P-channel types. This power-management approach suits high-efficiency battery-operated systems.

Applications Engineering Support

A final note—If you don't see what you need in Maxim's catalogs or applications notes, call the Applications Engineering department at (408) 737-7600. Maxim introduces an average of 60 new products per year, and one of those products may fit your needs exactly. Or, a simple trick may adapt an existing IC for your purpose, saving you the trouble of reinventing the wheel.

A Designer's Guide to Maxim DC-DC Converters

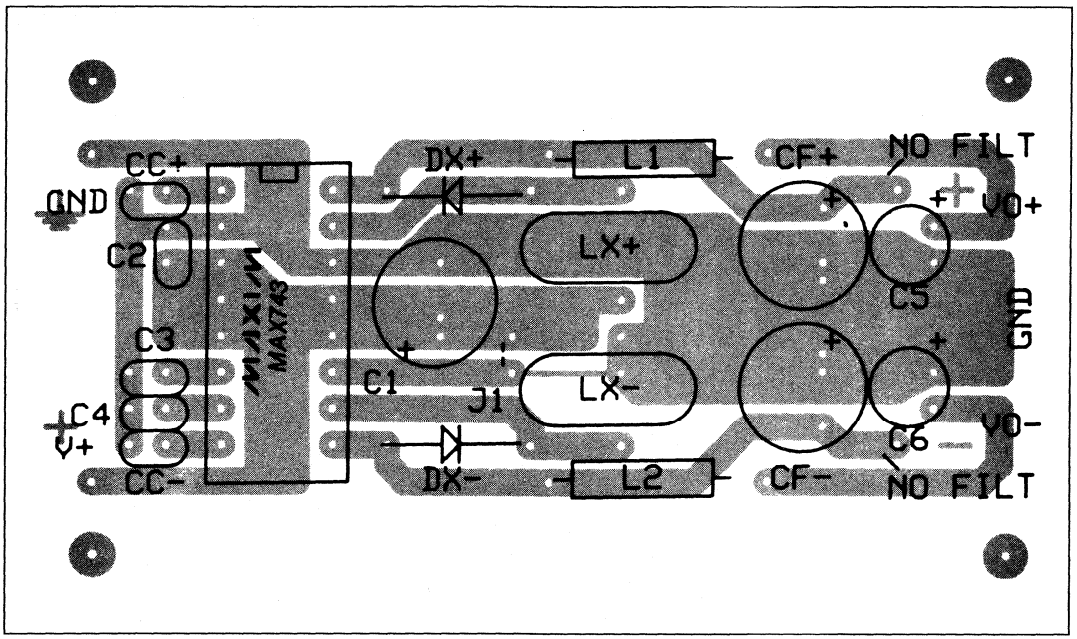


Figure 16. ***Evaluation PC Board For MAX743 Dual-Output PWM*** *Because it operates in the continuous-conduction mode and switches at a reasonably high frequency—200 kHz—the MAX743 is discomfited by plug-in plastic protoboards and wire-wrap construction methods. This evaluation-kit PC board helps minimize noise and grounding problems during prototyping.*

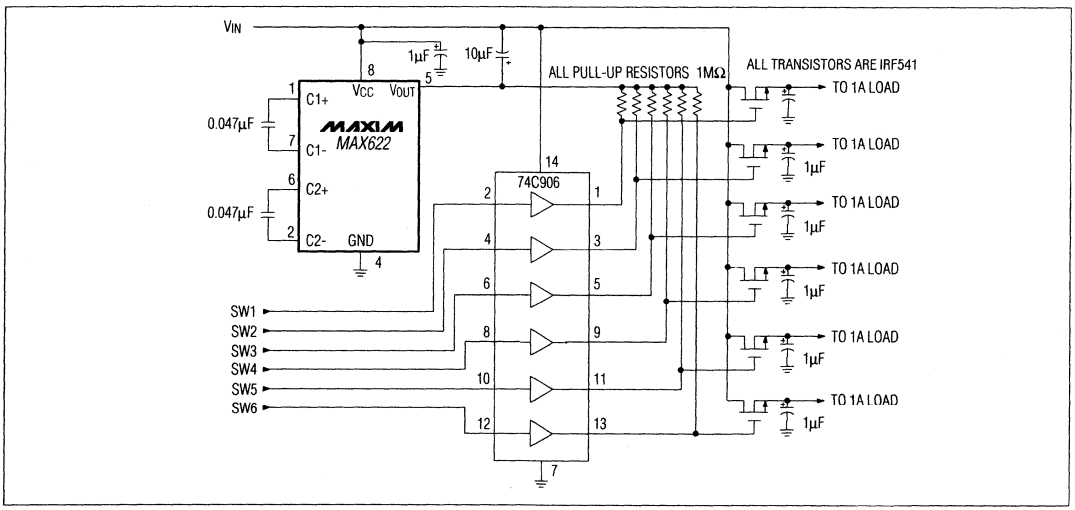


Figure 17. ***6 Amp Load Management Circuit*** *A charge-pump DC-DC converter (MAX622) generates a regulated voltage 10V above V_{IN}, for driving N-channel MOSFETs in high-side switching circuits.*

19-4325; Rev 0; 7/91

MAXIM

Quad, High-Side MOSFET Drivers

General Description

The MAX620/MAX621 incorporate four MOSFET drivers and a charge-pump high-side power supply to power high-side switching and control circuits. The charge pump delivers a regulated output voltage 11V greater than Vcc to the drivers, which then translate a TTL/CMOS input signal to a noninverted output that swings from ground to the high-side voltage. The outputs drive N-channel FETs in high-side or low-side switching applications, including a wide range of line- and battery-powered applications.

The MAX620/MAX621 are microprocessor compatible and feature undervoltage lockout capability. This lockout feature inhibits the FET driver outputs until the high-side voltage reaches the proper level, as indicated by a Power-Ready output.

The MAX620 requires three inexpensive charge-pump capacitors. The MAX621 has internal capacitors—no external components are needed.

Applications

Portable Computer Battery Load Management

High-Side Power, N-Channel MOSFET Switching

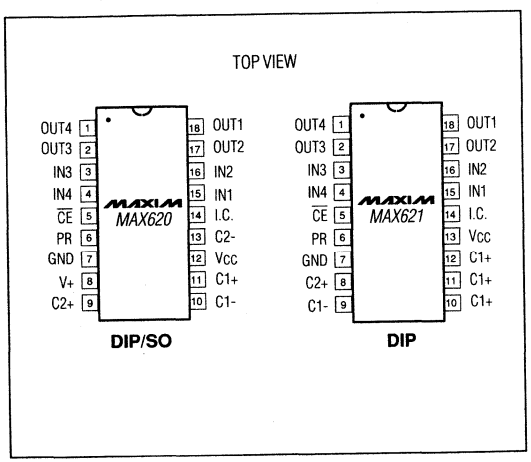
Low-Side Switching from Low Supply Voltages

Quad-Latching Level Translators

H-Bridge Motor Drivers

Stepper Motor Drivers

Pin Configurations



Features

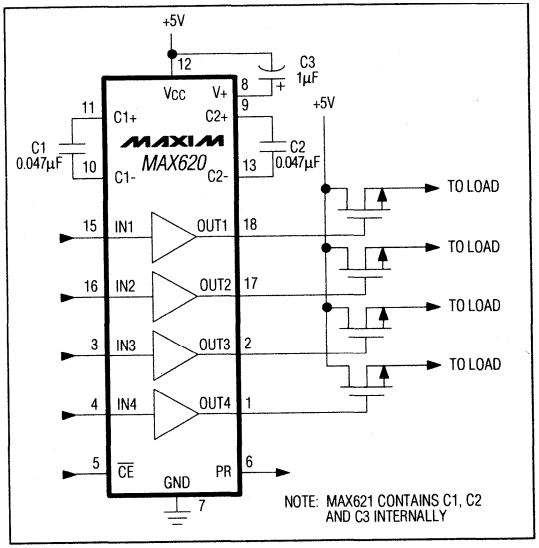
- ♦ Wide Operating Voltage Range
- ♦ Minimum Component Count
- ♦ Output Voltage Regulated to Vcc Plus 11V (Typ)
- ♦ Low Quiescent Current – 70µA (Typ)
- ♦ Undervoltage Lockout
- ♦ Power-Ready Output
- ♦ Internal Quad Latch

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX620CPN	0°C to +70°C	18 Plastic DIP
MAX620CWN	0°C to +70°C	18 Wide SO
MAX620C/D	0°C to +70°C	Dice*
MAX620EPN	-40°C to +85°C	18 Plastic DIP
MAX620EWN	-40°C to +85°C	18 Wide SO
MAX620MJN	-55°C to +125°C	18 CERDIP
MAX621CPN	0°C to +70°C	18 Plastic DIP
MAX621EPN	-40°C to +85°C	18 Plastic DIP

*Contact factory for dice specifications.

Typical Operating Circuit



Quad, High-Side MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} 17V
V+ to GND 30V
Inputs and Driver Outputs ..... (GND-0.3V) to (V+ + 0.3V)
PR Output ..... (GND-0.3V) to (V_{CC} + 0.3V)
Continuous Driver Output Current 25mA
V+ Output Current (MAX620 Only) 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8mW/°C above +70°C) 640mW
Wide SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX62 _ C _ _ ..... 0°C to +70°C
MAX62 _ E _ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			4.5		16.5	V
High-Side Voltage (Note 1)	V+	I_{OUT} = 0, V_{CC} = 4.5V C1 = C2 = 0.047µF, C3 = 1µF		14.5	15.5	17.5	V
		I_{OUT} = 0, V_{CC} = 16.5V C1 = C2 = 0.01µF, C3 = 1µF (Note 2)		26.5	27.5	29.5	
		I_{OUT} = 250µA, V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF		15	16	18	
		I_{OUT} = 500µA, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)		26.5	27.5	29.5	
Power-Ready Threshold	PRT	I_{OUT} = 0 (Note 3) (Note 4)		12.0	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA (Note 4)		3.8	4.7	5.0	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA (Note 4)			0.1	0.4	V
Switching Frequency	f_O	I_{OUT} = 0, T_A = +25°C			70		kHz
Quiescent Supply Current	I_Q	MAX620	V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0		70	500	µA
		MAX621	V_{CC} = 5V, T_A = +25°C, I_{OUT} = 0				
		MAX620	V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0 (Note 5)		50	350	
		MAX621	V_{CC} = 16.5V, T_A = +25°C, I_{OUT} = 0				

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

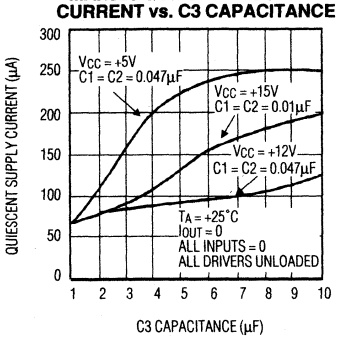
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE DRIVERS						
Input Threshold Low	V_{TL}				0.8	V
Input Threshold High	V_{TH}		2.4			V
Input Bias Current	I_B	0V < V_{IN} < 5V	-100		100	nA
Chip Enable Threshold Low	CE_{LO}				0.8	V
Chip Enable Threshold HIgh	CE_{HI}		2.4			V
Minimum $\overline{CE}$ Pulse Duration	T_{CE}		100	50		ns
Pull-Down Current	I_{CE}			10		µA
Data-Hold Time	T_{DH}			-10	10	ns
Data Set-Up Time	T_{SU}			50	100	ns
Data-Delay Time	T_{OD}	V_{CE} = 0V, C_L = 12pF		150		ns
Driver Output Rise Time	T_R	C_L = 1000pF		1.7		µs
Driver Output Fall Time	T_F	C_L = 1000pF		2.5		µs

Note 1: High-Side Voltage (V+) is available only on the MAX620 and is measured with respect to GND. V+ on the MAX621 is measured at an unloaded output. Capacitor values listed in the test conditions apply to the MAX620 only.
Note 2: For V_{CC} > +13V, on the MAX620 only, use C1 = C2 = 0.01µF, C3 = 1µF.
Note 3: Power-Ready Threshold is the voltage with respect to GND at V+ when PR switches high (PR_{OH} = V_{CC}).
Note 4: For the MAX621, the Power-Ready levels are tested at wafer sort only.
Note 5: The MAX620 is tested for quiescent current at +16.5V using C1 = C2 = 0.047µF to minimize test time. In normal operation above +13V, C1 and C2 must not exceed 0.01µF.

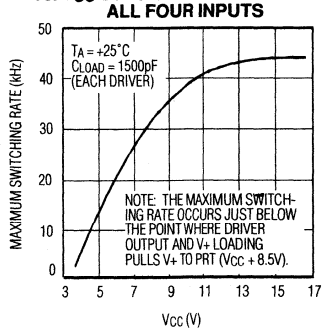
4

Typical Operating Characteristics

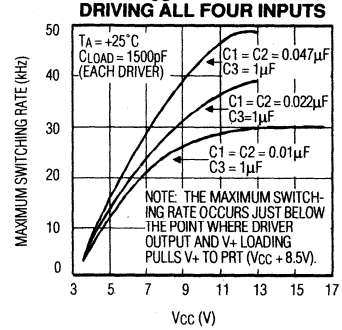
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITANCE



MAX621 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS



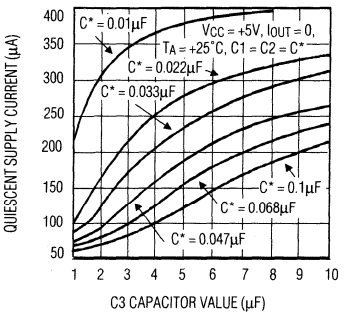
MAX620 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS



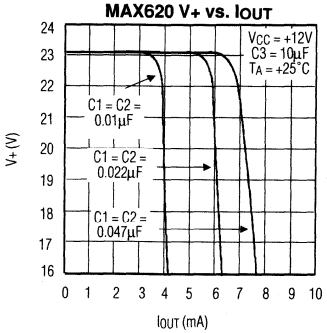
Quad, High-Side MOSFET Drivers

Typical Operating Characteristics (continued)

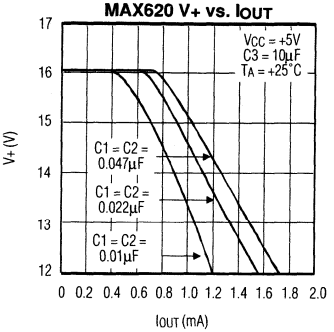
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITOR VALUE



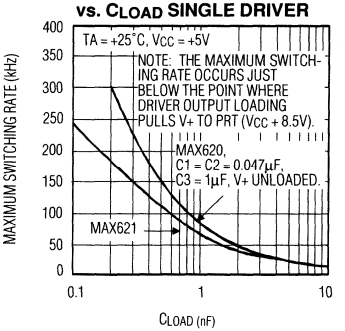
MAX620 V+ vs. IOUT



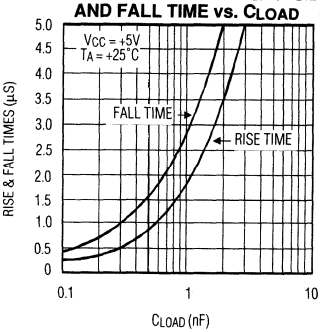
MAX620 V+ vs. IOUT



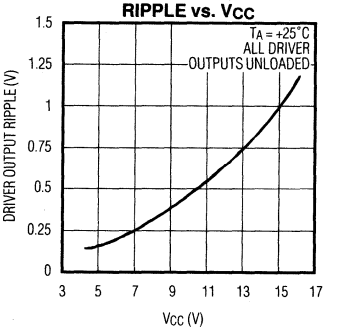
MAXIMUM SWITCHING RATE vs. CLOAD SINGLE DRIVER



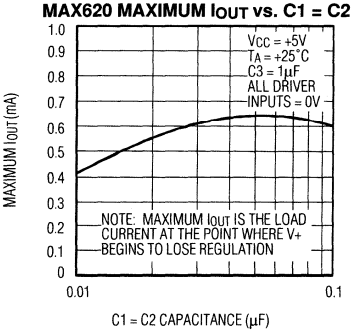
MAX620/MAX621 DRIVER RISE AND FALL TIME vs. CLOAD



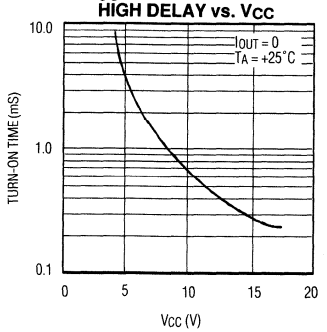
MAX621 DRIVER OUTPUT RIPPLE vs. VCC



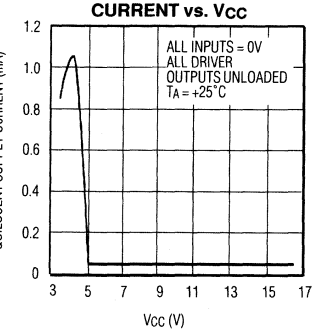
MAX620 MAXIMUM IOUT vs. C1 = C2



VCC TO POWER-READY HIGH DELAY vs. VCC

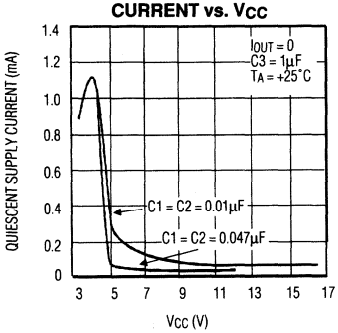


MAX621 QUIESCENT SUPPLY CURRENT vs. VCC

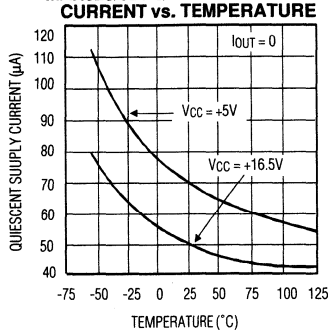


Typical Operating Characteristics (continued)

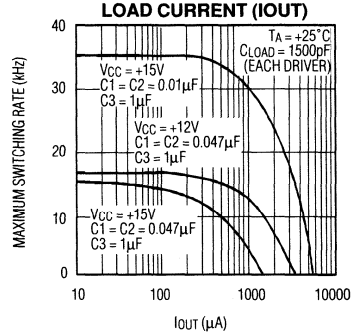
MAX620 QUIESCENT SUPPLY CURRENT vs. VCC



MAX620/621 QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

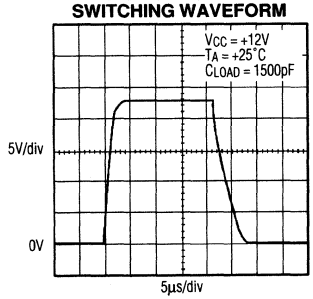


MAX620 MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (IOUT)

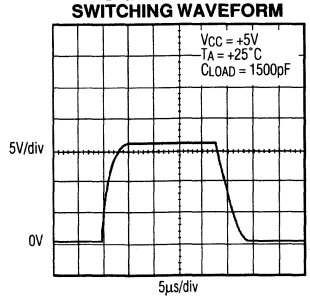


NOTE: THE MAXIMUM SWITCHING RATE OCCURS JUST BELOW THE POINT WHERE DRIVER OUTPUT AND V+ LOADING PULLS V+ TO PRT (VCC + 8.5V).

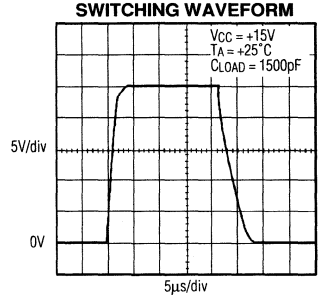
DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



Quad, High-Side MOSFET Drivers

Pin Description

PIN		NAME	FUNCTION
MAX620	MAX621		
1	1	OUT4	Driver Output 4
2	2	OUT3	Driver Output 3
3	3	IN3	TTL/CMOS Compatible Input to Driver 3. Connect to GND if unused.
4	4	IN4	TTL/CMOS Compatible Input to Driver 4. Connect to GND if unused.
5	5	$\overline{CE}$	Chip Enable. Logic high inhibits input data. Logic low transfers input data to the quad latch and driver outputs. $\overline{CE}$ pulse must be at least 100ns. Connect to GND for direct data transfer to driver outputs.
6	6	PR	Power-Ready Output is a logic high equal to V_{CC} when V+ ≥ (V_{CC} plus 8.5V).
7	7	GND	Ground
8		V+	High-side voltage out. Equal to approximately V_{CC} plus 11V.
	8	C2+	Internally connected to secondary charge-pump capacitor. Make no connection to this pin.
9		C2+	Positive terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	9	C1-	Internallly connected to primary charge-pump capacitor. Make no connection to this pin.
10		C1-	Negative terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	10-12	C1+	Internally connected to primary charge-pump capacitor. Make no connection to these pins.
11		C1+	Positive terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
12	13	V_{CC}	Supply Voltage. Connect to positive supply.
13		C2-	Negative terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
14	14	I.C.	Internal Connection. Make no connection to this pin.
15	15	IN1	TTL/CMOS Compatible Input to Driver 1. Connect to GND if unused.
16	16	IN2	TTL/CMOS Compatible Input to Driver 2. Connect to GND if unused.
17	17	OUT2	Driver Output 2
18	18	OUT1	Driver Output 1

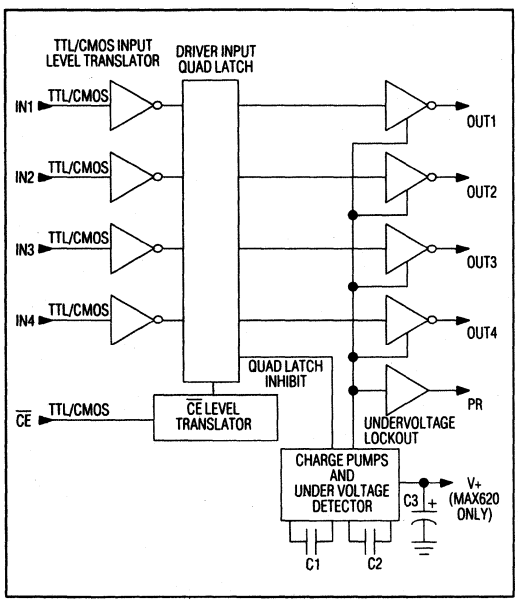


Figure 1. MAX620/MAX621 Functional Diagram

Detailed Description

Figure 1 shows the MAX620/MAX621 functional diagram. A regulated multi-stage charge pump supplies four MOSFET drivers with V_{CC} plus 11V for driving external MOSFETS (Figure 2). The logic inputs to the four drivers are stored in a quad latch. Data is latched by pulling $\overline{CE}$ high. An undervoltage lockout feature prevents the driver outputs from going high until V+ reaches the power-ready threshold (PRT) voltage (V_{CC} plus 8.5V) and V_{CC} is greater than +3V.

The Dual Charge Pump

The high-side voltage of approximately 11V above V_{CC} is generated by a multi-stage charge pump (Figure 2). Although the charge pump is capable of multiplying V_{CC} by up to four times, the output is regulated to V_{CC} plus 11V by an internal feedback circuit. The charge pump typically operates at 70kHz, but regulates by pulse-skipping. When V+ exceeds V_{CC} plus 11V, the charge pump shuts off. As V+ falls below V_{CC} plus 11V, the charge pump turns on.

The MOSFET Drivers

The four MOSFET drivers level shift TTL/CMOS input signals to output levels that switch between ground and V_{CC} plus 11V. These outputs can drive N-channel power MOSFETs in either high-side or low-side switching ap-

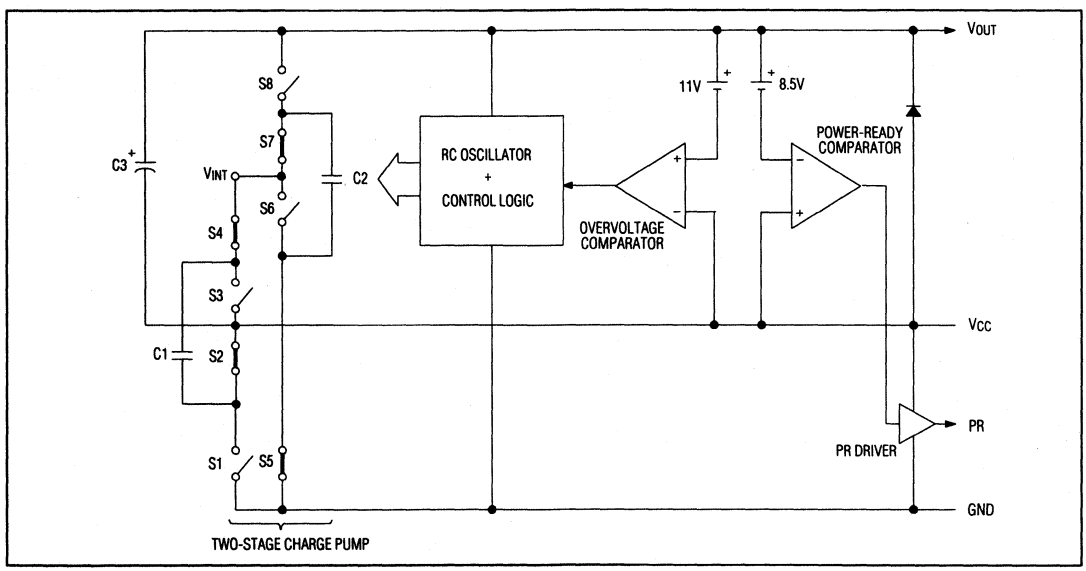


Figure 2. MAX620/MAX621 Charge Pump Block Diagram

plications (a bridge arrangement would contain two high-side and two low-side N-channel MOSFET switches—see Figure 4).

Data Input Latch

The driver outputs are separated from the data inputs by a quad latch. When $\overline{CE}$ is pulled low, the latch becomes transparent and data transfers directly to the outputs. When $\overline{CE}$ goes high, the latch enters hold mode and new input data is not transferred to the driver outputs.

Input data must be valid typically 100ns before the rising edge of $\overline{CE}$, and held for 10ns (max over temp). The minimum $\overline{CE}$ pulse width is 100ns (Figure 3). If latched operation is not required, connect $\overline{CE}$ to GND.

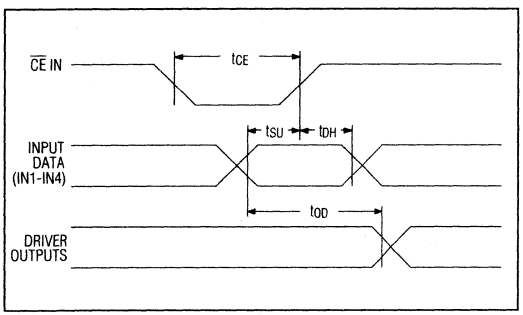


Figure 3. Digital Interface Timing Diagram

Undervoltage Latch Inhibit

If V_{CC} falls below +3V due to a power failure or while powering down, or V+ falls below V_{CC} plus 8.5V, the quad latch immediately resets, forcing the driver outputs low. The quad latch remains reset until V_{CC} rises above +3V with the high-side voltage present. This prevents the latch from being corrupted with erroneous data in a momentary power failure by ensuring that it will be reset.

Undervoltage Detector

The MAX620/MAX621 each contain an undervoltage detector, which forces all driver outputs low when the high-side voltage (V+) is less than the PRT or when V_{CC} is less than +3V. This ensures that the external N-channel MOSFET power transistors have sufficient gate drive to operate without dissipating excessive power. On power-up, the quad latch remains reset until the charge pump boosts the high-side voltage to the PRT. As soon as V+ reaches the PRT, the undervoltage lockout disables, the quad latch is enabled, and Power Ready (PR) goes high.

The undervoltage lockout feature also forces the driver outputs low if V+ is pulled below PRT, e.g., if the driver output(s) or V+ are overloaded.

Power-Ready Output

The MAX620/MAX621's PR output is a direct extension of the undervoltage lockout feature. When power is applied, PR remains a logic low until V+ reaches the PRT and V_{CC} exceeds +3V. The PR output high level is V_{CC}.

Capacitor Selection for the MAX620

Capacitor type is not critical for the MAX620. However, if operation with V_{CC} exceeding +13V is expected, C1 and C2 must be no greater than 0.01µF. Larger value capacitors, with V_{CC} above +13V, dissipate excessive energy in the internal switches during charge-pump cycles.

Sourcing Current From V+ (MAX620 Only)

A small amount of current may be sourced from V+ (pin 8) to drive other circuitry. The amount of current is a function of V_{CC}, the gate capacitance of all MOSFETs being driven, and the driver switching rate ("MAX620 Maximum Switching Rate vs. Additional V+ Load Current," *Typical Operating Characteristics*).

The MAX620 V+ output is not internally short-circuit protected. In applications where V+ is susceptible to short circuiting, external output short-circuit protection must be provided. Accomplish this by connecting a resistor between V+ and the load to limit the V+ current to less than 25mA. The resistor value is determined by the following formula:

$$R_{CL} \geq \frac{V_{CC}}{25mA}$$

Application Information

Data Input Transition Time

The MAX620/MAX621 are microprocessor compatible and easy to interface. However, the driver input voltage must not remain between V_{IL} and V_{IH} for more than 500ns. In clocked data-bus systems, this is most easily accomplished by setting data on the driver input lines before clocking $\overline{CE}$ low. However, most CMOS and TTL gates meet the 500ns transition speed requirement. Connect unused driver inputs to GND.

Maximum Driver Switching Rate

The maximum driver switching rate occurs when loading causes V+ to fall to the PRT (V_{CC} plus 8.5V) and the driver outputs go low. It is a function of the total gate capacitance of all MOSFETs being driven and the maximum available charge-pump output current at a given

supply voltage. For example, for V_{CC} = +5V with no external load on V+, the maximum switching rate while driving four 1500pF loads is 15kHz for the MAX620 (C1 = C2 = 0.047µF) and 14kHz for the MAX621 ("Maximum Switching Rate vs. V_{CC}," *Typical Operating Characteristics*).

Typical Application Circuits

H-Bridge Motor Driver

Figure 4 shows a MAX620 driving an H-bridge switch that controls the direction of a +5V DC motor. By toggling between the FORWARD and REVERSE inputs as shown, each MOSFET driver-output pair turns on its associated MOSFET pair, which passes current through the motor, causing rotation in the desired direction. In order to prevent all four MOSFETs from switching on at once, the FORWARD/REVERSE inputs should be updated before clocking $\overline{CE}$ low. Of course, FORWARD and REVERSE must not be asserted simultaneously. Do not use a supply voltage that will cause the gate drive to exceed the absolute maximum gate-to-source voltage of the low-side switch.

Stepper Motor Driver

A MAX620, clock source, pulse control network, and translator logic form a complete stepper motor driver (Figure 5). TTL/CMOS signals from the logic network are translated to high-side levels that drive four N-channel power MOSFETs, supplying current to each of four stepper motor phases. Diodes provide a discharge current path for the stepper motor windings.

Logic-Controlled, +5V Regulated Power Distribution

A MAX620, LM10 reference and op-amp combination, and an IRFZ40 N-channel MOSFET comprise an ultra-low dropout +5V regulator that supplies power to four IRFZ40 high-side switches (Figure 6).

When the power switch, S_P, is closed, V+ quickly pumps up to V_{CC} plus 11V. PR remains low and holds the output of the +5V regulator near zero until V+ has reached the PRT, (V_{CC} plus 8.5V--4ms typ). At the same time, the undervoltage lockout feature of the MAX620 forces the driver outputs low until the PRT is reached. Capacitor C4 suppresses load-switching transients. Its size depends on the largest load being switched. With C4 = 1000µF, the peak transient for a 1A switched load is less than 150mV.

The circuit provides a single continuous +5V output and four switched +5V supply lines. The regulator is capable of supplying several amps with a typical dropout voltage of 28mV at 1A (Q1=IRFZ40).

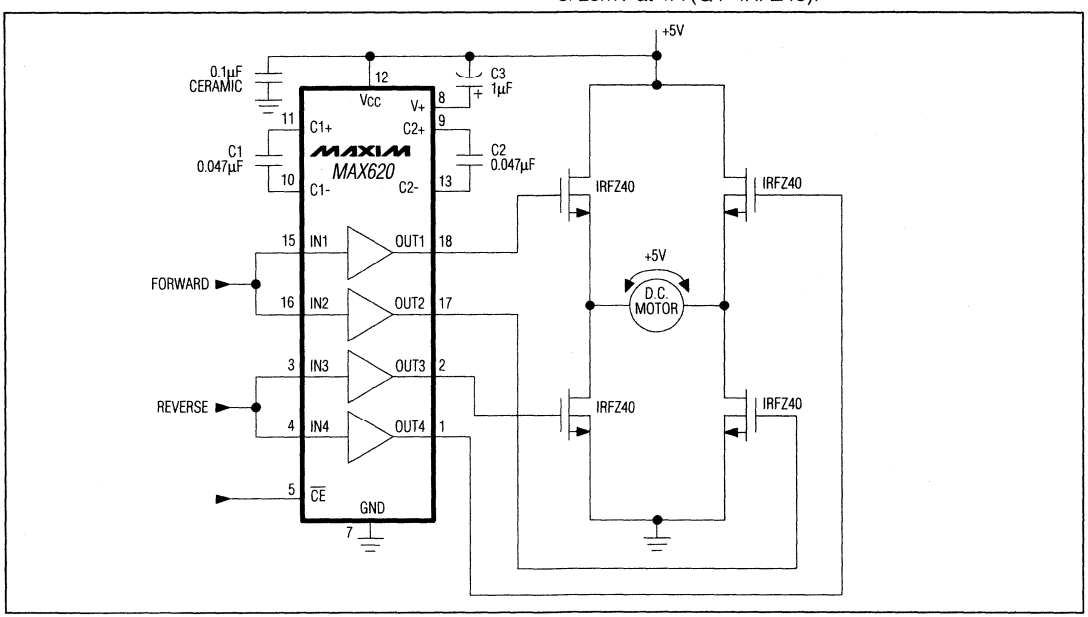


Figure 4. H-Bridge DC Motor Controller

Quad, High-Side MOSFET Drivers

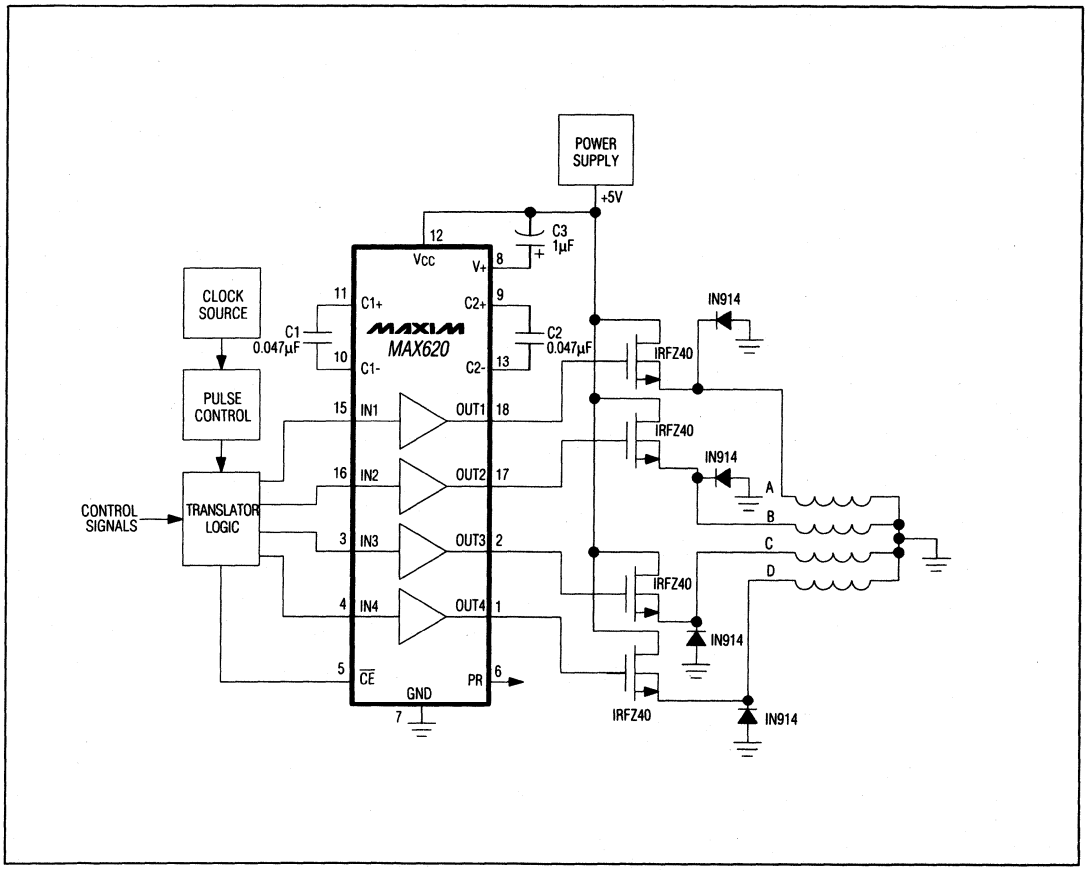


Figure 5. Four-Phase Stepper Motor Drive System

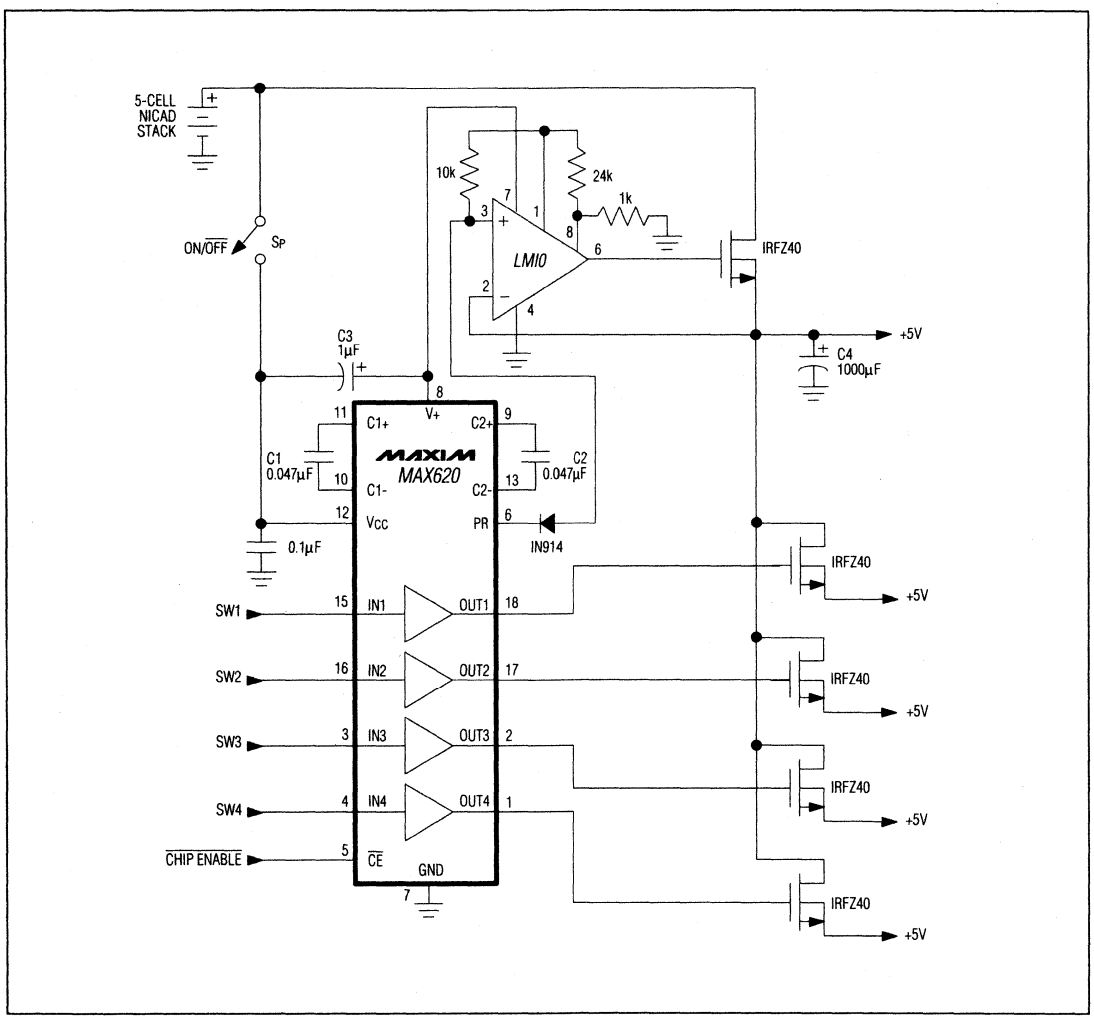
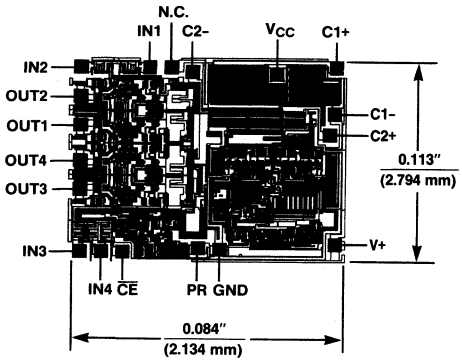


Figure 6. Logic-Controlled, +5V Regulated Power Distribution System

Quad, High-Side MOSFET Drivers

Chip Topography



NOTE: Connect substrate to V+.
MAX620 transistor count: 303

19-4022; Rev 0; 4/91

MAXIM

High-Side Power Supplies

General Description

The MAX622/MAX623 high-side power supplies, using a regulated charge-pump, generate a regulated output voltage 11V greater than the input supply voltage to power high-side switching and control circuits. The MAX622/MAX623 allow low-resistance N-Channel MOSFETs (FETs) to be used in circuits that normally require costly, less efficient P-Channel FETs and PNP transistors. The high-side output also eliminates the need for logic FETs in +5V and other low-voltage switching circuits.

A +3.5V to +16.5V input supply range and a typical quiescent current of only 70µA make the MAX622/MAX623 ideal for a wide range of line- and battery-powered switching and control applications where efficiency is crucial. Also provided is a logic-level Power-Ready Output (PR) to indicate when the high-side voltage reaches the proper level.

The MAX622 comes in 8-pin DIP and SO packages and requires three inexpensive external capacitors. The MAX623 is supplied in 16-pin DIPs only, but contains internal capacitors and requires no external components.

Applications

High-Side Power Control with N-Channel FETs

Low-Dropout Voltage Regulators

Power Switching from Low Supply Voltages

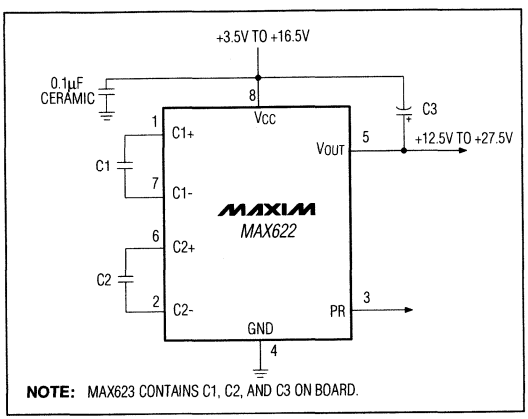
H-Switches

Stepper Motor Drivers

Battery-Load Management

Portable Computers

Typical Operating Circuit



NOTE: MAX623 CONTAINS C1, C2, AND C3 ON BOARD.

Features

- ♦ **+3.5V to +16.5V Operating Supply Voltage Range**
- ♦ **Output Voltage Regulated to V_{CC} + 11V (Typ)**
- ♦ **70µA Typ Quiescent Current**
- ♦ **Power-Ready Output**

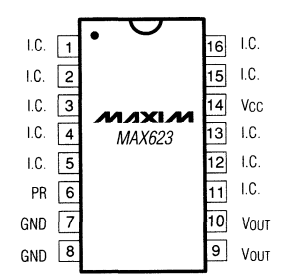
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX622CPA	0°C to +70°C	8 Plastic DIP
MAX622CSA	0°C to +70°C	8 SO
MAX622C/D	0°C to +70°C	Dice*
MAX622EPA	-40°C to +85°C	8 Plastic DIP
MAX622ESA	-40°C to +85°C	8 SO
MAX623CPE	0°C to +70°C	16 Plastic DIP
MAX623EPE	-40°C to +85°C	16 Plastic DIP

Contact factory for dice specifications.

Pin Configurations

DIP/SO



DIP

4

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +17V
V_{OUT} ..... +30V
I_{OUT} 25mA
Continuous Total Power Dissipation (T_A = +70°C)
8-pin Plastic DIP (derate 6.9mW/°C above +70°C) ... 552mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
16-pin Plastic DIP (derate 7.41mW/°C above +70°C) . 593mW

Operating Temperature Ranges:
MAX62_C_ _ ..... 0°C to +70°C
MAX62_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX622)

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.5		16.5	V
High-Side Voltage (Note 1)	V_{OUT}	I_{OUT} = 0, V_{CC} = 3.5V, C1 = C2 = 0.047µF, C3 = 1µF	11.5	12.5	16.5	V
		I_{OUT} = 0, V_{CC} = 4.5V, C1 = C2 = 0.047µF, C3 = 1µF	14.5	15.5	17.5	
		I_{OUT} = 0, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5	27.5	29.5	
		I_{OUT} = 50µA, V_{CC} = 3.5V, C1 = C2 = 0.047µF, C3 = 1µF	8.5	10.5	16.5	
		I_{OUT} = 250µA, V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF	15		18	
		I_{OUT} = 500µA, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5		29.5	
Power-Ready Threshold	PRT	I_{OUT} = 0 (Note 3)	12	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA	3.8	4.3	5	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA			0.4	V
Output Voltage Ripple	VR	C1 = C2 = 0.01µF, C3 = 10µF, I_{OUT} = 1mA, V_{CC} = 16.5V		50		mV
Switching Frequency	F_O			90		kHz
Quiescent Supply Current	IQ	I_{OUT} = 0, V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF, T_A = +25°C		70	500	µA
		I_{OUT} = 0, V_{CC} = 16.5V, C1 = C2 = 0.047µF, C3 = 1µF, T_A = +25°C		70	350	

ELECTRICAL CHARACTERISTICS (MAX623)

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.5		16.5	V
High-Side Voltage (Note 1)	V_{OUT}	I_{OUT} = 0, V_{CC} = 3.5V	11.5	12.5	16.5	V
		I_{OUT} = 0, V_{CC} = 4.5V	14.5	15.5	17.5	
		I_{OUT} = 0, V_{CC} = 16.5V	26.5	27.5	29.5	
		I_{OUT} = 50µA, V_{CC} = 3.5V	8.5	10.5	16.5	
		I_{OUT} = 250µA, V_{CC} = 5V	15		18	
		I_{OUT} = 500µA, V_{CC} = 16.5V	26.5		29.5	
Power-Ready Threshold	PRT	I_{OUT} = 0 (Note 3)	12	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA	3.8	4.3	5	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA			0.4	V
Output Voltage Ripple	VR	I_{OUT} = 500µA (Note 4)		100		mV
Switching Frequency	F_O			90		kHz
Quiescent Supply Current	IQ	I_{OUT} = 0, V_{CC} = 5V, T_A = +25°C		70	500	µA
		I_{OUT} = 0, V_{CC} = 16.5V, T_A = +25°C		70	350	

Note 1: High-Side Voltage measured with respect to ground.
Note 2: For V_{CC} > +13V on the MAX622, use C1 = C2 = 0.01µF.
Note 3: Power-Ready Threshold is the voltage with respect to ground at V_{OUT} when PR switches high (PR = V_{CC}).
Note 4: Output Voltage Ripple on the MAX623 may be reduced by adding an external 10µF reservoir capacitor.

4

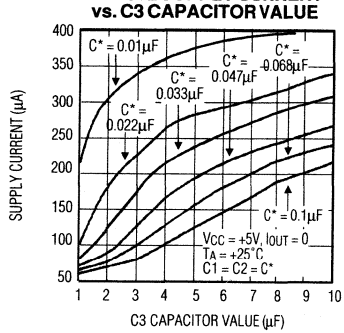
Pin Description

MAX622 8-PIN	MAX623 16-PIN	NAME	FUNCTION
1		C1+	Positive terminal to primary charge-pump capacitor.
	1-5, 11-13, 15, 16	I.C.	Internal Connection. Make no connection to this pin.
2		C2-	Negative terminal to secondary charge-pump capacitor.
3	6	PR	Power-Ready Output. High when V_{OUT} is ≥ V_{CC} + 8.5V with respect to GND.
4	7, 8	GND	Ground
5	9, 10	V_{OUT}	High-Side Voltage Out
6		C2+	Positive terminal to secondary charge-pump capacitor.
7		C1-	Negative terminal to primary charge-pump capacitor.
8	14	V_{CC}	Input Supply

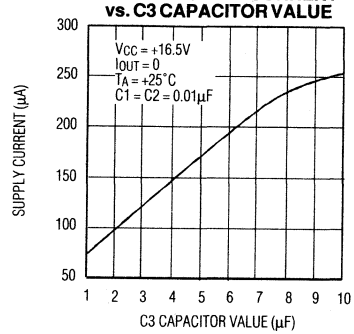
High-Side Power Supplies

Typical Operating Characteristics

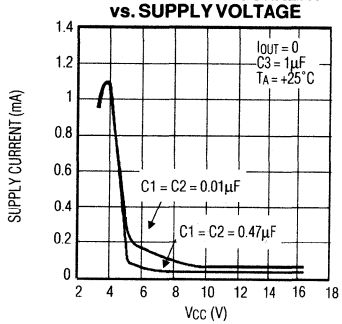
MAX622 SUPPLY CURRENT vs. C3 CAPACITOR VALUE



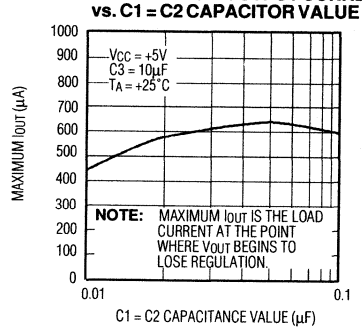
MAX622 SUPPLY CURRENT vs. C3 CAPACITOR VALUE



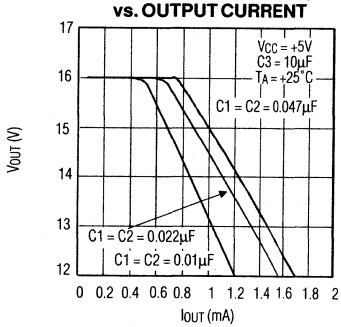
MAX622 SUPPLY CURRENT vs. SUPPLY VOLTAGE



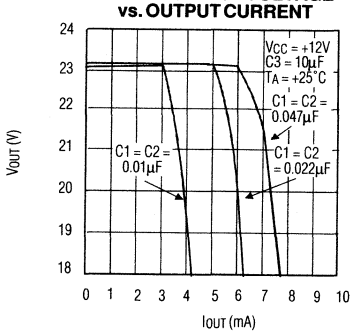
MAX622 MAXIMUM OUTPUT CURRENT vs. C1 = C2 CAPACITOR VALUE



MAX622 OUTPUT VOLTAGE vs. OUTPUT CURRENT

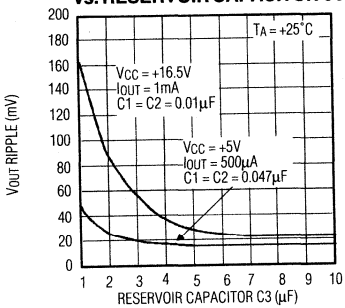


MAX622 OUTPUT VOLTAGE vs. OUTPUT CURRENT

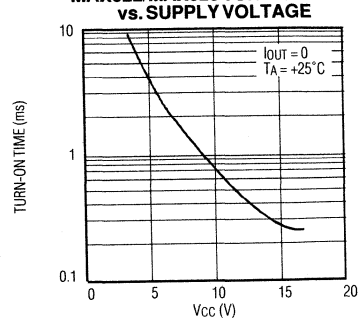


Typical Operating Characteristics (continued)

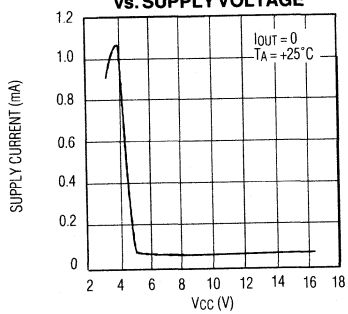
MAX622 OUTPUT VOLTAGE RIPPLE vs. RESERVOIR CAPACITOR C3



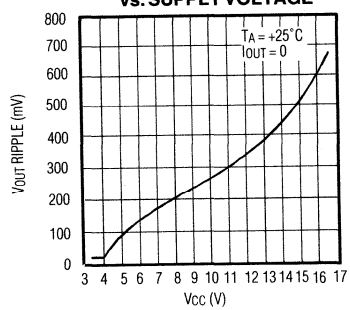
MAX622/MAX623 TURN-ON TIME vs. SUPPLY VOLTAGE



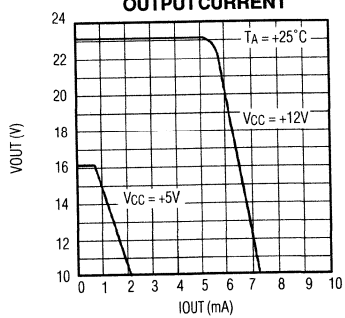
MAX623 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX623 OUTPUT VOLTAGE RIPPLE vs. SUPPLY VOLTAGE



MAX623 OUTPUT VOLTAGE vs. OUTPUT CURRENT



High-Side Power Supplies

Detailed Description

Charge-Pump Operation

The MAX622/MAX623 are multi-stage charge-pump power supplies. Although the charge pumps are capable of multiplying V_{CC} up to four times, the outputs are regulated to V_{CC}+11V by an internal feedback circuit for inputs above 4V. The charge pumps typically operate at 90kHz, but regulate by pulse-skipping. When V_{OUT} exceeds V_{CC}+11V, the oscillator shuts off. As V_{OUT} dips below V_{CC}+11V, the oscillator turns on.

Power-Ready Output

The Power-Ready Output (PR) signals control circuitry when the high-side voltage reaches a preset level. This feature can be used to protect external FET switches from excess dissipation and damage by preventing them from turning on, except when adequate gate drive levels are present. When power is applied, PR remains low until V_{OUT} reaches approximately V_{CC} +8.5V. PR also goes low if V_{OUT} falls below this level during operation, i.e. if the output is overloaded. The PR high level is V_{CC}.

Application Hints

Quiescent Supply Current

MAX622 quiescent supply current varies with V_{CC} and with the values of C1, C2, and C3 (*Typical Operating Characteristics*). Even with no external load, the device must still pump to overcome internal losses. Larger ratios between C3 and C1 or C2 require more charge-pump cycles to restore V_{OUT}. The MAX623 with internal capacitors is not subject to supply-current variations with capacitor ratio. As V_{CC} falls below 5V, quiescent current rises fairly rapidly to about 1mA at 4V (*Typical Operating Characteristics*). This rise occurs because V_{OUT} no longer pulse-skips to regulate at low input voltages; the oscillator runs continuously, so supply current is higher. Figure 2 shows the test circuits for the MAX622/MAX623 quiescent supply current.

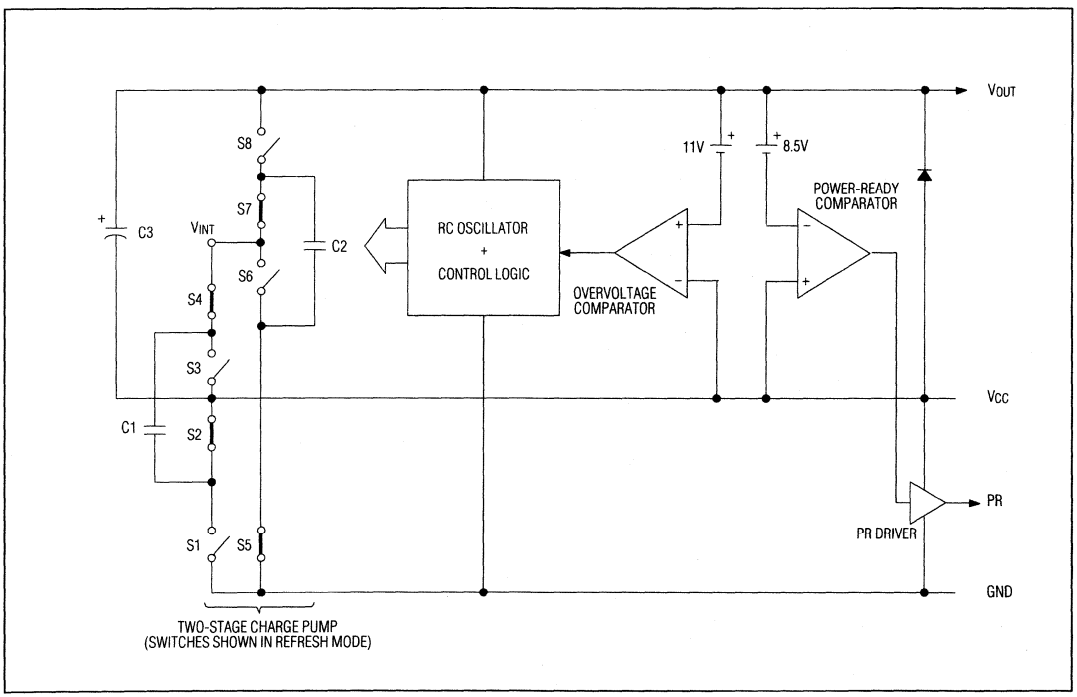


Figure 1. MAX622/MAX623 Block Diagram

Output Ripple

V_{OUT} ripple is typically 50mV peak-to-peak with V_{CC} = +5V, C1 and C2 = 0.047µF, and C3 = 1µF (*Typical Operating Characteristics*). Ripple can be reduced by increasing the ratio between the output storage capacitor C3 and C1 and C2. This is usually accomplished by increasing C3 and keeping C1 and C2 in the 0.01µF to 0.047µF range. For example, if C1 and C2 are 0.047µF (V_{CC} must not exceed 13V) and C3 is 10µF, output ripple typically falls to 15mV (*Typical Operating Characteristics*). Similarly, MAX623 output ripple is reduced by adding an external storage capacitor from V_{OUT} to V_{CC}.

Capacitor Selection

Capacitor type is unimportant when selecting capacitors for the MAX622. However, when V_{CC} exceeds 13V, C1 and C2 must be no greater than 0.01µF. Using larger value capacitors with input voltages above 13V causes excessive amounts of energy to pass through internal switches during charge-pump cycles. This may damage the device.

Output Protection

The MAX622/MAX623 are not internally short-circuit protected. In applications where the output is susceptible to short circuit, external output short-circuit protection must be provided. Accomplish this by connecting a resistor between V_{OUT} and the load to limit output current to less than 25mA. The resistor value is determined by the following formula:

$$R_{CL} \geq \frac{V_{CC}}{25mA}$$

Typical Applications

Simple Single-Load Switch

A single switch can be made with the MAX622/MAX623 and a MAX480 op amp configured as a comparator

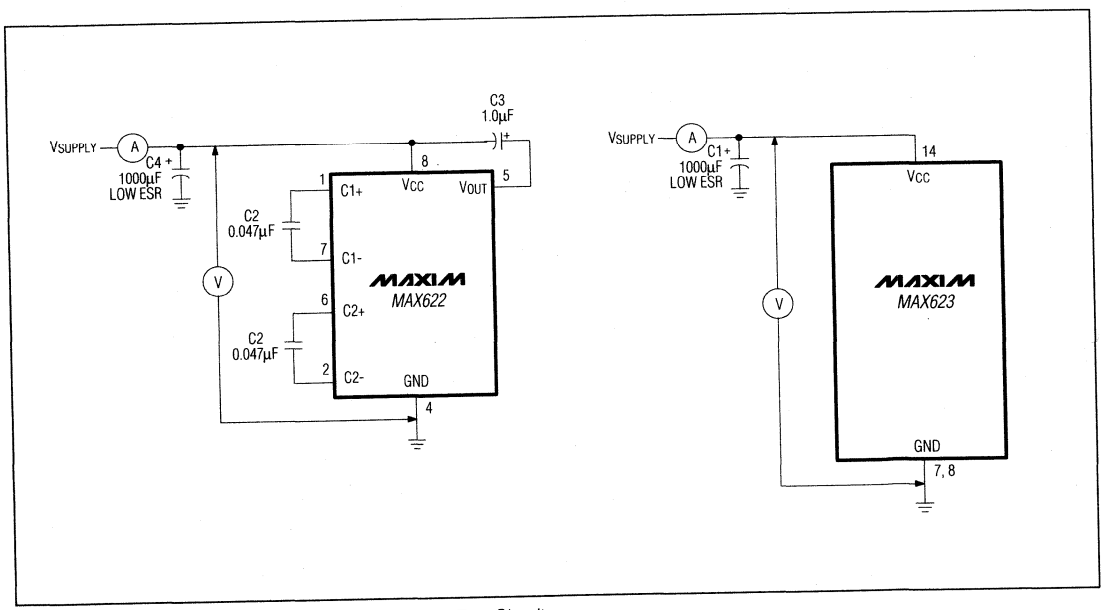


Figure 2. MAX622/MAX623 Quiescent Supply-Current Test Circuits

High-Side Power Supplies

(Figure 3). The switch is turned on by applying V_{BATT} to the ON/$\overline{OFF}$ input and turned off by pulling it to GND.

One MAX622 Drives Six High-Side Switches

Multiple subsystems or modules can be turned on and off using a single MAX622 and an open-drain hex buffer such as the 74C906 (Figure 4). The drains of all buffer outputs are pulled up through resistors to the MAX622's V_{OUT}. The pull-up resistance depends on the number of channels being used with the MAX622/MAX623 and power-dissipation limitations. The minimum pull-up resistor value is determined by the number of channels paralleled on each high-side power supply and the high-side output current from the MAX622/MAX623 at a given supply voltage, calculated as follows:

$$R_{MIN} = \frac{V_{OUT} \times (\text{number of channels})}{I_{OUT}}$$

where V_{OUT} is the high-side output voltage and I_{OUT} is the output current of the MAX622.

For example, assuming an output current of 1mA and six channels, as in Figure 4, the minimum pull-up resistor value that will not excessively load the MAX622 is about 100kΩ, assuming all six channels are pulled low at the same time. The value of the pull-up resistor also affects the turn-on time of each FET, and hence the amount of energy dissipated in the FET during turn on. The rate of rise of V_{GS} is limited by the RC time constant of the pull-up resistor and FET gate capacitance; waste power will be dissipated in the FET equal to $(I_{LOAD})^2 \times r_{DS}$ during the RC time period.

H-Bridge Motor Driver

An H-bridge motor driver is shown in Figure 5. The motor direction can be controlled by toggling between IN1 and IN2 of the DG303 analog switch. Each switch section turns on the appropriate FET pair which passes current through the motor in the desired direction.

Battery-Load Controller

In Figure 6, a MAX8211 undervoltage detector detects the battery's end-of-life, and a MAX622 high-side power supply turns the power FET switch on. During normal operation, the MAX8211 Hysteresis pin powers the MAX622, providing gate-drive to keep the FET off. When the battery reaches its discharge threshold (end-of-life), the MAX8211 output pulls the FET gate low, cutting off current to the load. At the same time, the Hysteresis pin goes low, turning off the MAX622. As a result, supply current is approximately 10µA in the load-disconnected condition.

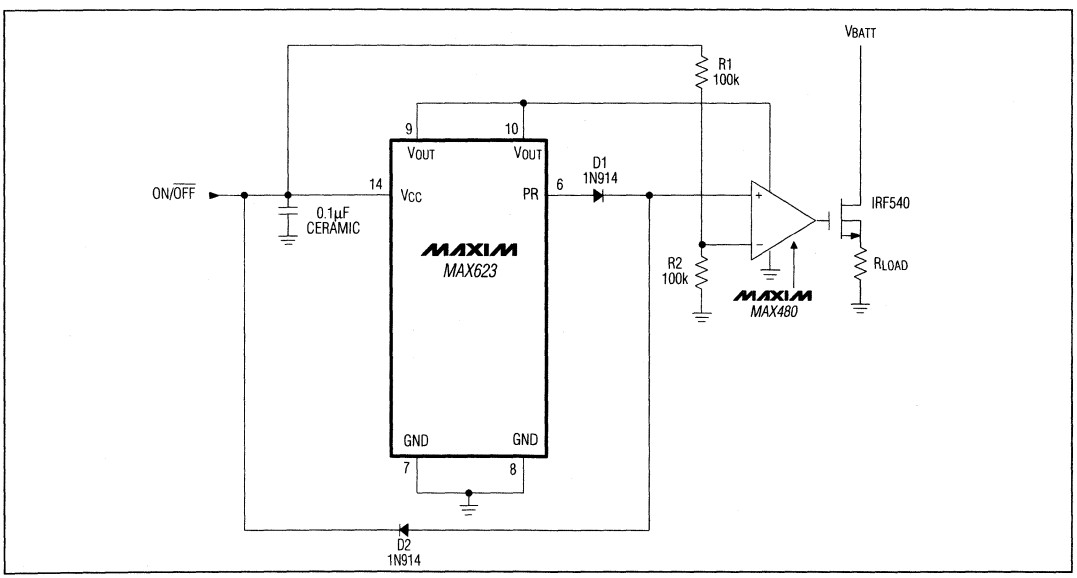


Figure 3. Single-Load Switch

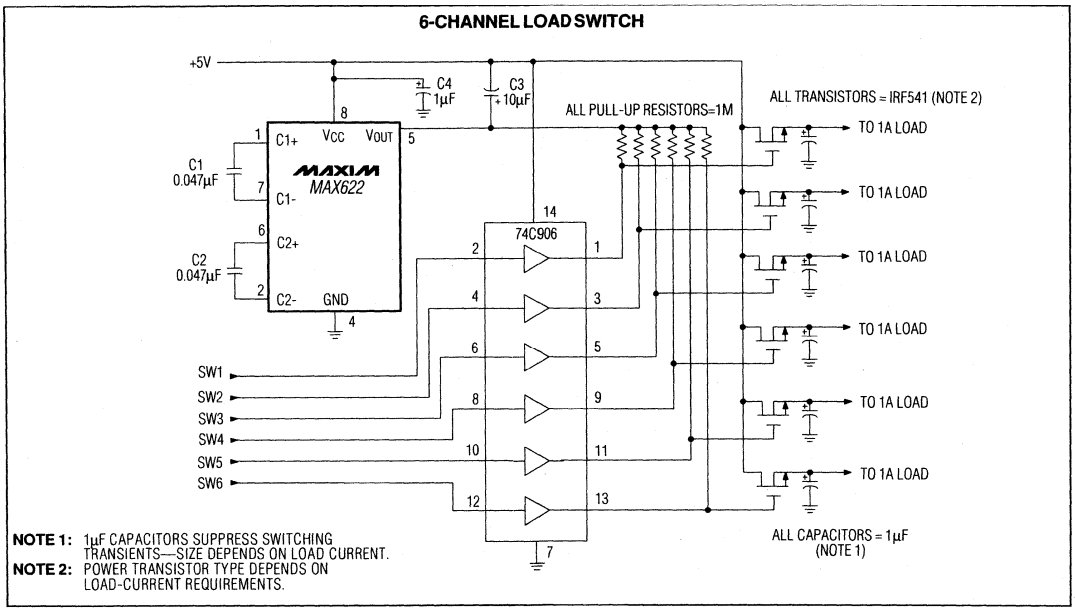


Figure 4. A Single MAX622 Drives Six High-Side Switches

4

4-Channel Load Switch With No Pull-Up Resistors

Multiple high-side switches can be driven from a single MAX622/MAX623 high-side power supply with no pull-up resistors on the FET gates. In Figure 7, a MAX622 supplies high-side voltage to a MAX333 quad analog switch to control any one of four high-side switches. The FET gates are normally connected to ground when the MAX333 logic inputs are low.

Low-Dropout Regulator

In Figure 8, a MAX622 high-side power supply powers an LM10 reference and op-amp combination, providing sufficient gate drive to turn on the FET. This allows the regulator to achieve less than 70mV dropout at 1A load using an IRF541, and just under 20mV for a SMP60N06.

The 200mV reference section is configured for a gain of 25 (e.g. 200mV x 25 = 5V) and connects to the noninverting input of the op amp; the regulator's output connects directly to the inverting input. The op amp amplifies the error between its inputs and varies the gate drive to the FET, regulating the output. Capacitor C6 reduces transients due to load changes; its size depends on the magnitude of the load change in the application and can be reduced or eliminated if the load remains relatively constant. With C6 = 1000µF, the output transient to a 1A load pulsed at 20Hz is typically less than 150mV. The regulator is turned on by applying V_{BATT} to the Enable/Shutdown input and turned off by pulling this input to ground.

The regulator output voltage, V_{OUT}, is set by the ratio of R1 to R2, calculated as follows:

$$R2 = R1\left(\frac{V_{OUT}}{0.2} - 1\right)$$

If the application does not require logic shutdown, connect the MAX622 V_{CC} pin directly to the battery and eliminate D2.

High-Side Power Supplies

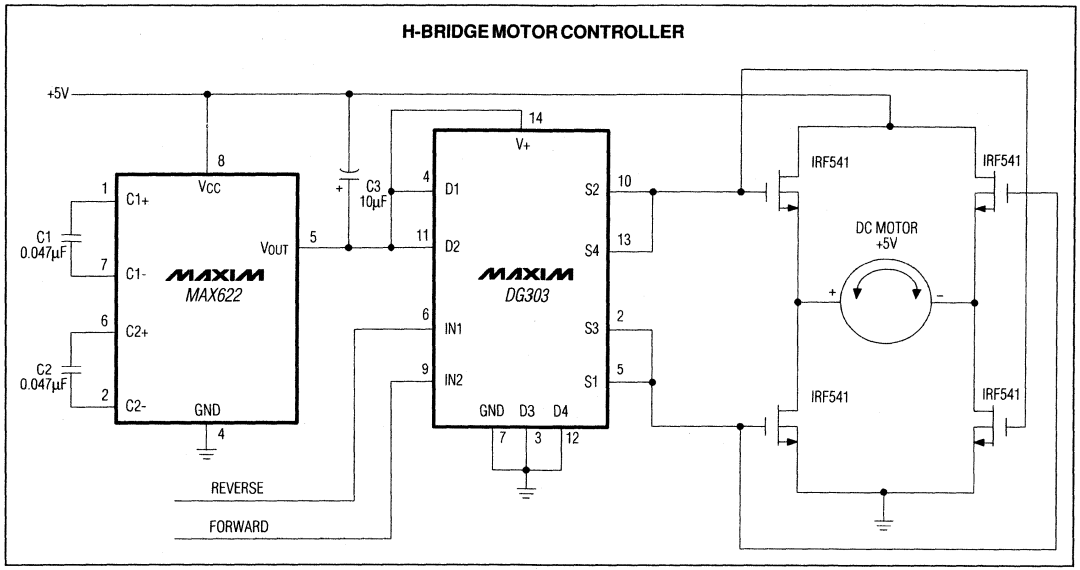


Figure 5. H-Bridge Motor Controller

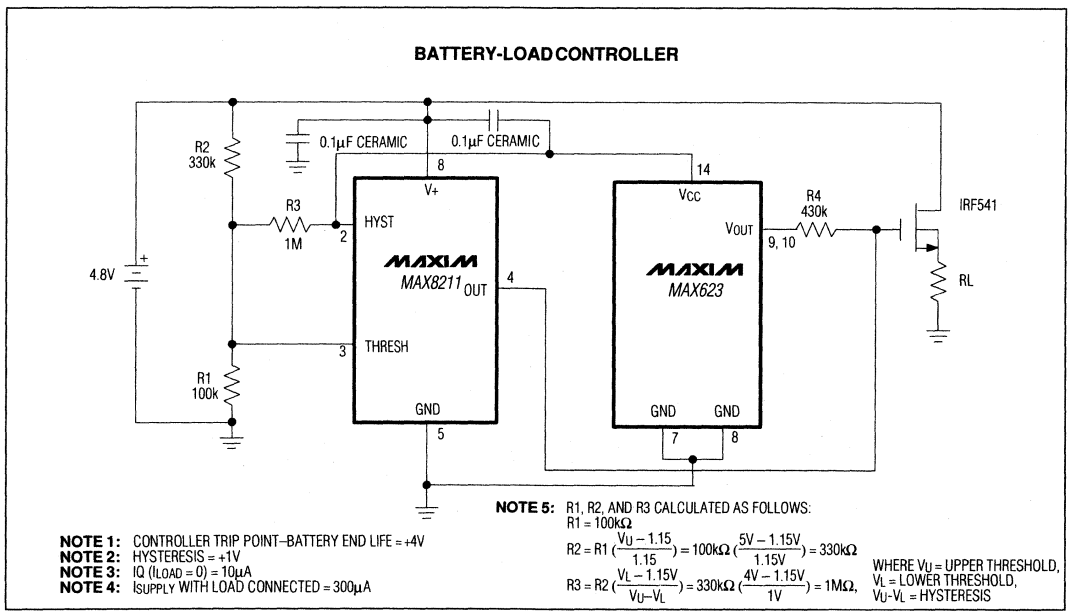


Figure 6. Battery-Load Controller Prevents Excessive Load at Battery End-of-Life

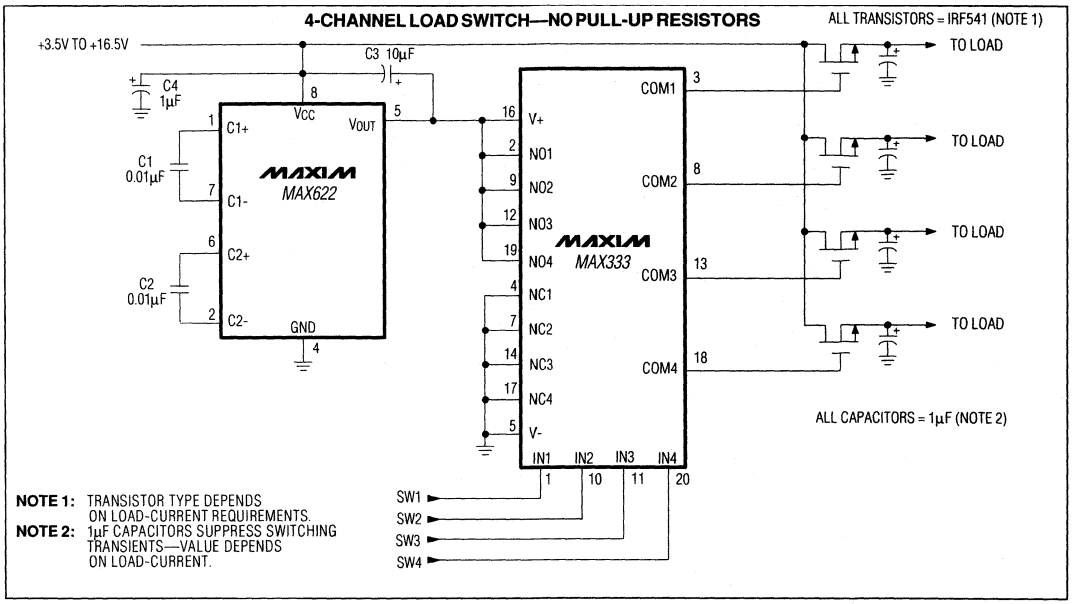


Figure 7. A MAX622 Powers a MAX333 Quad Analog Switch, Realizing a 4-Channel Load Switch with No Pull-Up Resistors

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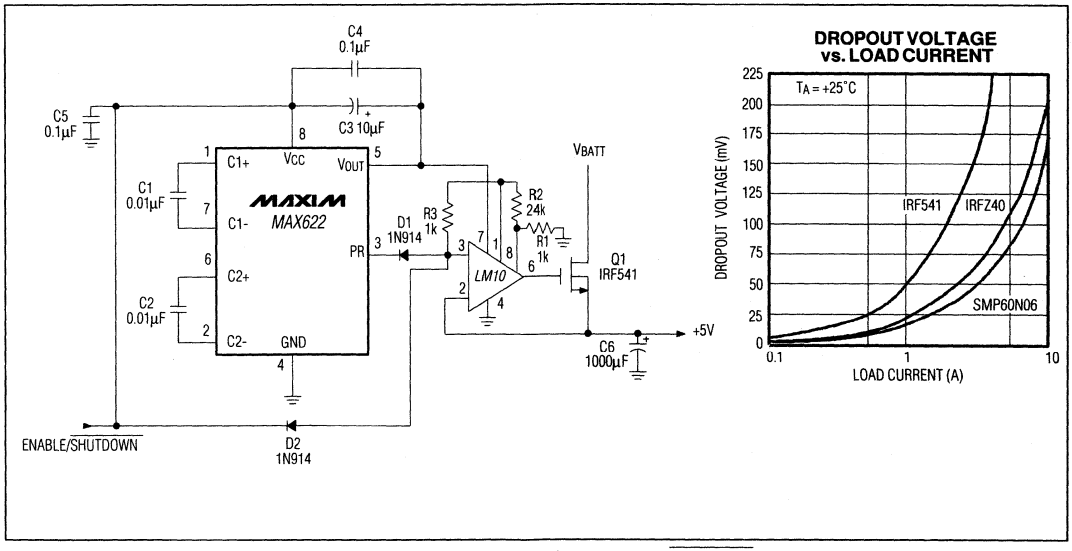
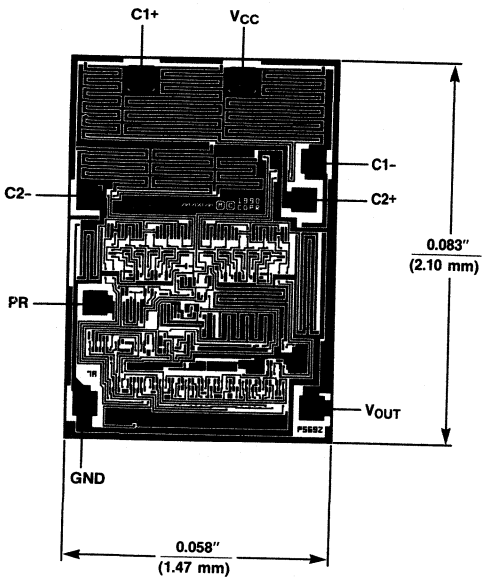


Figure 8. Ultra-Low Dropout Positive Voltage Regulator with Logic-Controlled Enable/Shutdown

High-Side Power Supplies

Chip Topography



NOTE: Connect substrate to V_{OUT}.

MAX622/MAX623 Transistor Count: 158

MAXIM

Quad, High-Side Power Switch

General Description

The MAX625 is a quad high-side power switch that switches 1A steady state loads with 5A peak currents. The switch resistances are typically 0.2Ω, and internal clamp diodes allow inductive load switching. The MAX625 is completely self-contained in a 24-pin, 0.300" narrow plastic DIP package and requires no external components for normal operation.

The +4.5V to +16.5V input supply range and a typical quiescent current of only 70µA make the MAX625 ideal for a wide range of line- and battery-powered switching and control applications that require high efficiency and small size.

An internal quad latch accepts four TTL/CMOS logic signals that control the four switches. The MAX625 eliminates expensive logic MOSFETs in +5V-only and other low-voltage switching circuits. It also replaces costly, bulky, and less efficient P-channel MOSFETs or PNP transistors.

Applications

Portable Computer Battery-Load Management

High-Side Power, N-Channel MOSFET Switching

Low-Side Switching from Low Supply Voltages

Solid-State Relay

Quad-Latching Level Translators

H-Bridge Motor Drivers

Stepper Motor Drivers

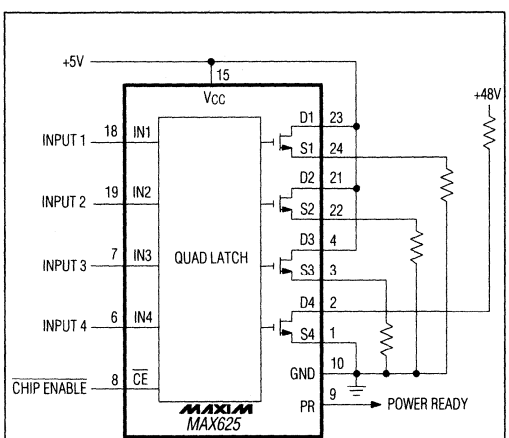
Features

- **0.2Ω Switch Resistance**
- **+4.5V to +16.5V Operating Supply Voltage Range**
- **Output Voltage Regulated to V_{CC} + 11V (Typ) Available at V+**
- **70µA Quiescent Current (Typ)**
- **Quad Latched TTL/CMOS Inputs**
- **Power-Ready Output**
- **Undervoltage Lockout**

Ordering Information

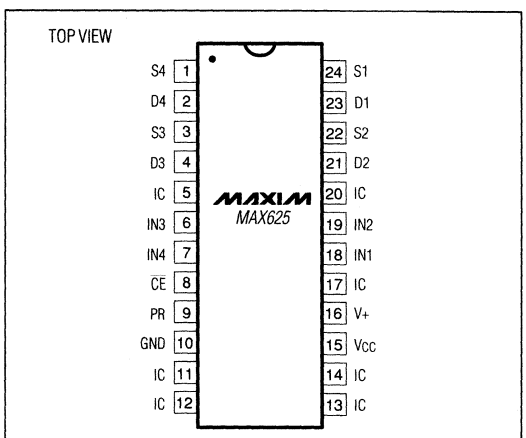
PART	TEMP. RANGE	PIN-PACKAGE
MAX625CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX625ENG	-40°C to +85°C	24 Narrow Plastic DIP

Typical Operating Circuit



POWER MANAGEMENT CIRCUIT ILLUSTRATING SEVERAL LOAD POSSIBILITIES

Pin Configuration



MAXIM

CMOS Micropower Step-Up Switching Regulator

General Description

Maxim's MAX630 and MAX4193 CMOS DC-DC regulators are designed for simple, efficient, minimum size DC-DC converter circuits in the 5 milliwatt to 5 watt range. The MAX630 and MAX4193 provide all control and power handling functions in a compact 8 pin package: a 1.31V bandgap reference, an oscillator, a voltage comparator, and a 375mA N-channel output MOSFET. A comparator is also provided for low battery detection.

Operating current is only 70μA and is nearly independent of output switch current or duty cycle. A logic level input shuts down the regulator to less than 1μA quiescent current. Low current operation ensures high efficiency even in low power battery operated systems. The MAX630 and MAX4193 are compatible with most battery voltages, operating from 2.0V to 16.5V.

The devices are pin compatible with the Raytheon bipolar circuits, RC4191/2/3, while providing significantly improved efficiency and low voltage operation. Maxim also manufactures the MAX631, MAX632, and MAX633 DC-DC converters which reduce the external component count in fixed output 5V, 12V, and 15V circuits. See Table 2 on the last page of this data sheet for a summary of other Maxim DC-DC converters.

Applications

+5V to +15V DC-DC Converters

High Efficiency Battery Powered DC-DC Converters

+3V to +5V DC-DC Converters

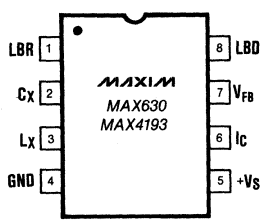
9V Battery Life Extension

Uninterruptible 5V Power Supplies

5mW to 5 Watt Switch-mode Power Supplies

Pin Configuration

Top View



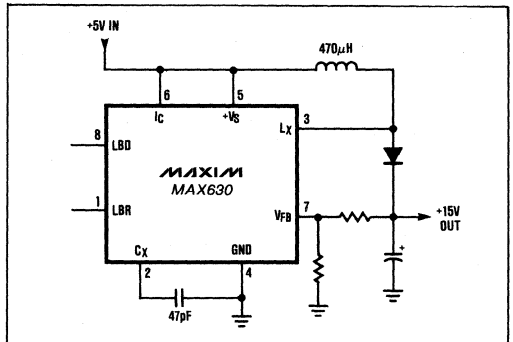
Features

- ♦ **High Efficiency—85% Typical**
- ♦ **70μA Typical Operating Current**
- ♦ **1μA Maximum Quiescent Current**
- ♦ **2.0 to 16.5V Operation**
- ♦ **525mA (Peak) Onboard Drive Capability**
- ♦ **±1.5% Output Voltage Accuracy (MAX630)**
- ♦ **Low Battery Detector**
- ♦ **Compact 8 Pin Mini-DIP and SO Packages**
- ♦ **Pin Compatible With RC4191/2/3**

Ordering Information

PART	TEMP. RANGE	8 Lead PACKAGE
MAX630CPA	0°C to +70°C	8 Lead Plastic DIP
MAX630CSA	0°C to +70°C	8 Lead Small Outline
MAX630CJA	0°C to +70°C	8 Lead CERDIP
MAX630EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX630ESA	-40°C to +85°C	8 Lead Small Outline
MAX630EJA	-40°C to +85°C	8 Lead CERDIP
MAX630MJA	-55°C to +125°C	8 Lead CERDIP
MAX4193C/D	0°C to +70°C	Dice
MAX4193CPA	0°C to +70°C	8 Lead Plastic DIP
MAX4193CSA	0°C to +70°C	8 Lead Small Outline
MAX4193CJA	0°C to +70°C	8 Lead CERDIP
MAX4193EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX4193ESA	-40°C to +85°C	8 Lead Small Outline
MAX4193EJA	-40°C to +85°C	8 Lead CERDIP
MAX4193MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



+5V to +15V Converter

4

CMOS Micropower Step-Up Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Operating Temperature Range
MAX630C, MAX4193C ..... 0°C to +70°C
MAX630E, MAX4193E ..... -40°C to +85°C
MAX630M, MAX4193M ..... -55°C to +125°C

Power Dissipation
Plastic DIP (derate 6.25mW/°C above 50°C) 468mW
Small Outline (derate 5.88mW/°C above 50°C) 441mW
CERDIP (derate 8.33mW/°C above 50°C) 833mW
Input Voltage (Pins 1, 2, 6, 7) ..... -0.3V to $+V_S$ +0.3V
Output Voltage, L_X and LBD 18V
L_X Output Current ..... 525mA Peak
LBD Output Current 50mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is no implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, T_A = +25°C, I_C = 5.0μA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX630			MAX4193			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage	$+V_S$	Operating Start-up	2.0 1.8		16.5	2.4		16.5	V
Internal Reference Voltage	V_{REF}		1.29	1.31	1.33	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_3 = 400mV	75	150		75	150		mA
Supply Current (at Pin 5)	I_S	I_3 = 0mA		70	125		90	200	μA
Efficiency				85			85		%
Line Regulation (Note 1)		$0.5V_0 < V_S < V_0$		0.08	0.2		0.08	0.5	% V_{OUT}
Load Regulation (Note 1)		V_S = +5V, P_{LOAD} = 0 to 150mW		0.2	0.5		0.2	0.5	% V_{OUT}
Operating Frequency Range (Note 2)	F_O		0.1	40	75	0.1	25	75	kHz
Reference Set Internal Pulldown Resistance	R_{IC}	$V_6 = V_S$	0.5	1.5	10	0.5	1.5	10	MΩ
Reference Set Input Voltage Threshold	V_{IC}		0.2	0.8	1.3	0.2	0.8	1.3	V
Switch Current	I_{SW}	V_3 = 1.0V	100			100			mA
Switch Leakage Current	I_{CO}	V_3 = 16.5V		0.01	1.0		0.01	5.0	μA
Supply Current (Shut Down)	I_{SO}	$I_C < 0.01\mu A$		0.01	1.0		0.01	5.0	μA
Low Battery Bias Current	I_{LBR}			0.01	10		0.01	10	nA
Capacitor Charging Current	I_{CX}			30			30		μA
C_X + Threshold Voltage				$+V_S$ - 0.1			$+V_S$ - 0.1		V
C_X - Threshold Voltage				0.1			0.1		V
V_{FB} Input Bias Current	I_{FB}			0.01	10		0.01	10	nA
Low Battery Detector Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		μA
Low Battery Detector Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V		0.01	5.0		0.01	5.0	μA

Note 1: Guaranteed by correlation with DC pulse measurements.
Note 2: The operating frequency range is guaranteed by design and verified with sample testing.

ELECTRICAL CHARACTERISTICS

(+V_S = +6.0V, T_A = Full Operating Temperature Range, I_C = 5.0μA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX630 MIN.	MAX630 TYP.	MAX630 MAX.	MAX4193 MIN.	MAX4193 TYP.	MAX4193 MAX.	UNITS
Supply Voltage	$+V_S$		2.2		16.5	3.5		16.5	V
Internal Reference Voltage	V_{REF}		1.25	1.31	1.37	1.20	1.31	1.42	V
Supply Current (Pin 5)	I_S	I_3 = 0mA		70	200		90	300	μA
Line Regulation (Note 1)		$0.5V_{OUT} < V_S < V_{OUT}$		0.2	0.5		0.5	1.0	% V_{OUT}
Load Regulation (Note 1)		V_S = +0.5V_0, P_L = 0 to 150mW		0.5	1.0		0.5	1.0	% V_{OUT}
Reference Set Internal Pulldown Resistance	R_{IC}	$V_6 = V_S$ 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C	 0.45 0.4 0.3	 1.5 1.5 1.5	 10 10 10	 0.45 0.4 0.3	 1.5 1.5 1.5	 10 10 10	MΩ
Reference Set Input Voltage Threshold	V_{IC}		0.2	0.8	1.3	0.2	0.8	1.3	V
Switch Leakage Current	I_{C0}	V_3 = 16.5V		0.1	30		0.1	30	μA
Supply Current (Shut Down)	I_{S0}	I_C < 0.01μA		0.01	10		0.01	30	μA
Low Battery Detector Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		μA

Note 1: Guaranteed by correlation with DC pulse measurements.

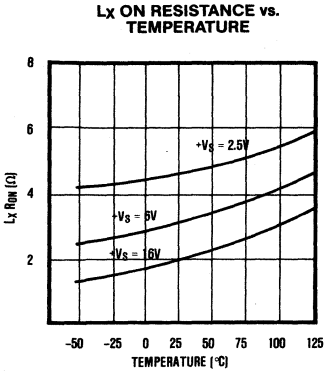
Pin Description

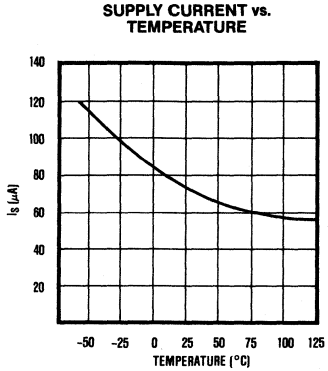
PIN	NAME	FUNCTION
1	LBR	Low Battery Detection Comparator input.The LBD output, pin 8, sinks current when ever this pin is below the low battery detector threshold, typically 1.31V.
2	C_X	An external capacitor connected between this terminal and ground sets the oscillator frequency. 47pF = 40KHz.
3	L_X	This pin drives the external inductor. The internal N-channel MOSFET which drives L_X has an output resistance of 4 ohms and a peak current rating of 525mA.
4	GND	Ground.
5	$+V_S$	The positive supply voltage, from 2.0V to 16.5V (MAX630).

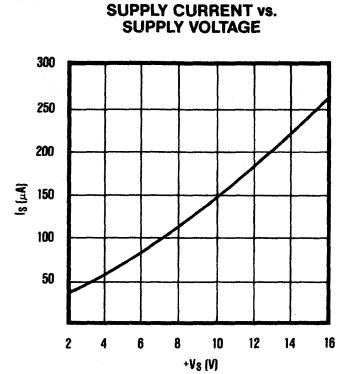
PIN	NAME	FUNCTION
6	I_C	The MAX630/MAX4193 shuts down when this pin is left floating or is driven below 0.2V. For normal operation connect I_C directly to $+V_S$ or drive it high with either a CMOS gate or pull-up resistor connected to $+V_S$. The supply current is typically 10nA in the shutdown mode.
7	V_{FB}	The output voltage is set by an external resistive divider connected from the converter output to V_{FB} and Ground. The MAX630/MAX4193 will pulse the L_X output whenever the voltage at this terminal is less than 1.31V.
8	LBD	The Low Battery Detector output is an open drain N-channel MOSFET which sinks up to 600 μA (typ) whenever the LBR input, pin 1, is below 1.31V.

CMOS Micropower Step-Up Switching Regulator

Typical Operating Characteristics







Detailed Description

The operation of the MAX630 can best be understood by examining the voltage regulating loop of Figure 1. R1 and R2 divide the output voltage, which is compared with the 1.3V internal reference by comparator COMP1. When the output voltage is lower than desired, the comparator output goes high and the oscillator output pulses are passed through the NOR gate latch, turning on the output N-channel MOSFET at pin 3, L_X. As long as the output voltage is less than the desired voltage, pin 3 drives the inductor with a series of pulses at the oscillator frequency.

Each time the output N-channel MOSFET is turned on, the current through the external coil, L1, increases, storing energy in the coil. Each time the output turns off, the voltage across the coil reverses sign and the voltage at L_X rises until the catch diode, D1, is forward biased, delivering power to the output.

When the output voltage reaches the desired level, 1.31V x (1 + R1/R2), the comparator output goes low and the inductor is no longer pulsed. Current is then supplied by the filter capacitor, C1, until the output voltage drops below the threshold, and once again L_X is switched on, repeating the cycle. The average duty cycle at L_X is directly proportional to the output current.

Output Driver (L_X Pin)

The MAX630/MAX4193 output device is a large N-channel MOSFET with an ON resistance of 4 ohms and a peak current rating of 525mA. One well known advantage that MOSFETs have over bipolar transistors in switching applications is higher speed, which reduces switching losses and allows the use of smaller, lighter, less costly magnetic components. Also important is that MOSFETs, unlike bipolar transistors, do not require base current which, in low power DC-DC converters, often accounts for a major portion of input power.

The operating current of the MAX630 and MAX4193 increases by approximately 1µA/kHz at maximum power output due to the charging current required by the gate capacitance of the L_X output driver (e.g. 40µA increase at a 40kHz operating frequency). In comparison, equivalent bipolar circuits typically drive their NPN L_X output device with 2mA of base drive, causing the bipolar circuit's operating current to increase by a factor of 10 between no load and full load.

Oscillator

The oscillator frequency is set by a single external, low cost ceramic capacitor connected to pin 2, C_X. 47pF sets the oscillator to 40kHz, a reasonable compromise between lower switching losses at low frequencies and reduced inductor size at higher frequencies.

Low Battery Detector

The low battery detector compares the voltage on LBR with the internal 1.31V reference. The output, LBD, is an open drain N-channel MOSFET. In addition to detecting and warning of a low battery voltage, the comparator can also perform other voltage monitoring operations such as power failure detection.

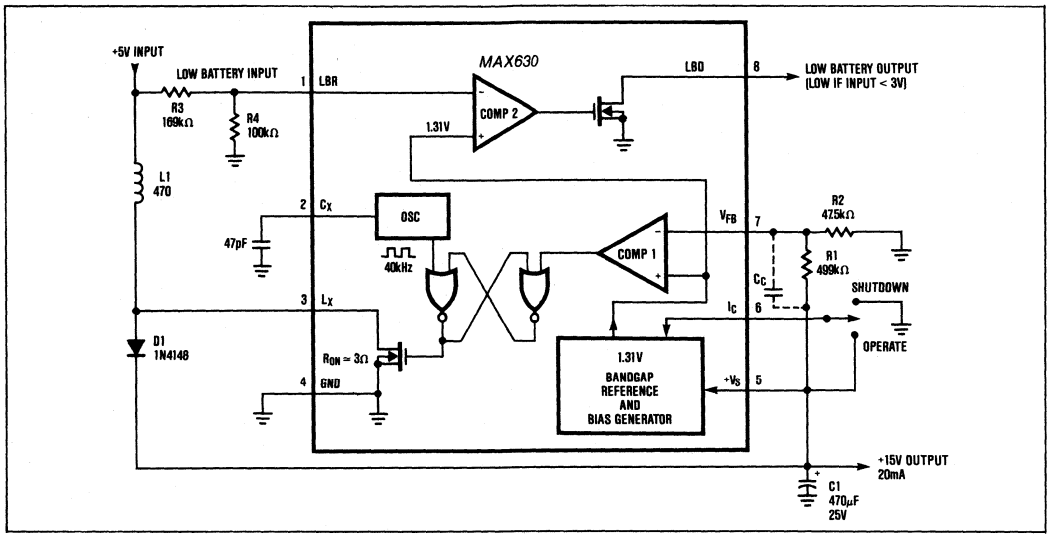


Figure 1. +5V to +15V Converter and Block Diagram

Another use of the low battery detector is to lower the oscillator frequency when the input voltage goes below a specified level. Lowering the oscillator frequency increases the available output power, compensating for the decrease in available power caused by reduced input voltage (See Figure 5).

Logic Level Shutdown Input

The shutdown mode is entered whenever I_C (pin 6) is driven below 0.2V or left floating. When shut down, the MAX630's analog circuitry, oscillator, L_X and LBD outputs are turned off. The device's quiescent current during shutdown is typically 10nA (1µA max).

Bootstrapped Operation

In most circuits, the preferred source of $+V_S$ voltage for the MAX630 and MAX4193 is the boosted output voltage. This is often referred to as a "bootstrapped" operation since the circuit figuratively "lifts" itself up.

The ON resistance of the N-channel L_X output decreases with an increase in $+V_S$, however, the device operating current goes up with $+V_S$ (see typical operating graph, I_S vs. $+V_S$). In circuits with very low output current and input voltages greater than 3V it may be more efficient to connect $+V_S$ directly to the input voltage rather than bootstrap.

External Components

Resistors

Since the LBR and V_{FB} input bias currents are specified as 10nA maximum, the current in the dividers R1/R2 and R3/R4 (figure 1) may be as low as 1µA without significantly affecting accuracy. Normally R2 and R4 are between 10k ohms and 1M ohm, which sets the current in the voltage dividers in the 1.3µA to 130µA range. R1 and R3 can then be calculated as follows:

$$10k\Omega \le R2 \le 1M\Omega \qquad R1 = R2 \times \frac{V_{OUT} - 1.31V}{1.31V}$$

$$10k\Omega \le R4 \le 1M\Omega \qquad R3 = R4 \times \frac{V_{LB} - 1.31V}{1.31V}$$

Where V_{OUT} is the desired output voltage and V_{LB} is the desired low battery warning threshold.

If the I_C (shutdown) input is pulled up through a resistor rather than connected directly to $+V_S$, the current through the pullup resistor should be a minimum of 4µA with I_C at the input-high threshold of 1.3V:

$$R_{IC} \le \frac{+V_S - 1.3V}{4\mu A}$$

CMOS Micropower Step-Up Switching Regulator

Inductor Value

The available output current from a DC-DC voltage boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency.

The inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses. If the inductance is too high, the MAX630 will not be able to deliver the desired output power, even with the L_X output on for every oscillator cycle. The available output power can be increased by either decreasing the inductance or the frequency. Reducing the frequency increases the on-period of the L_X output, thereby increasing the peak inductor current. The available output power is increased since it is proportional to the square of the peak inductor current (I_{pk}).

$$L_{MAX} = \frac{(V_{IN}\, T_{ON})^2\, f}{2\, P_{OUT}}$$

$$\text{since: } P_{OUT} = \frac{L I_{pk}^2\, f}{2}$$

$$\text{and: } I_{pk} = \frac{V_{IN}\, T_{ON}}{L}$$

Where P_{OUT} includes the power dissipated in the catch diode (D1) as well as that in the load. If the inductance is too low, the current at L_X may exceed the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}\, T_{ON}}{I_{MAX}}$$

Where I_{MAX} = 525mA (peak L_X current) and T_{ON} is the on-time of the L_X output.

The most common MAX630 circuit is a boost mode converter (Figure 1). When the N-channel output device is on, the current linearly rises since:

$$\frac{di}{dt} = \frac{V}{L}$$

At the end of the on-time (14μs for 40kHz, 55% duty cycle oscillator) the current is:

$$I_{pk} = \frac{V\, T_{ON}}{L} = \frac{5V \times 14\mu s}{470\mu H} = 150mA.$$

The energy in the coil is:

$$E = \frac{L\, I_{pk}^2}{2} = 5.25\mu J$$

At maximum load this cycle is repeated 40,000 times per second, and the power tranferred through the coil is 40,000x5.25 = 210mW. Since the coil only supplies the voltage above the input voltage, at 15V, the DC-DC converter can supply 210mW/(15V-5V) = 21mA. The coil provides 210mW and the battery directly supplies another 105mW, for a total of 315mW of output power. If the load draws less than 21mA, the MAX630 turns on its output only often enough to keep the output voltage at a constant 15V.

Reducing the inductor value increases the available output current: lower L increases the peak current, thereby increasing the available power. The external inductor required by the MAX630 is readily obtained from a variety of suppliers. (See Table 1). Standard coils are suitable for most applications.

Types of Inductors

Molded Inductors

These are cylindrically wound coils which look similar to 1 watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types.

Potted Toroidal Inductors

A typical 1mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685" in diameter by 0.385" high and mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode inductors since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes, often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used

with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective core area differs between the post, side, top and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permalloy powder (MPP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Nytronics	WEE-470	470μH, 10 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Torotel Prod.	PT 53-18	500μH, 5 ohms,
FERRITE CORES AND TOROIDS		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Diodes

In most MAX630 circuits, the inductor current returns to zero before L_X turns on for the next output pulse. This allows the use of slow turn-off diodes. On the other hand, the diode current abrubtly goes from zero to full peak current each time L_X switches off (figure 1, D1). To avoid excessive losses, the diode must therefore have a fast turn-on time.

For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well.

For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Filter Capacitor

The output voltage ripple has two components, with approximately 90° phase difference between them. One component is created by the change in the capacitor's stored charge with each output pulse. The other ripple component is the product of the capacitor's charge/discharge current and its ESR (effective series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than that caused by the change in charge.

$$V_{ESR} = I_{pk} \times ESR = \left(\frac{V_{IN}}{2Lf}\right) \times ESR \text{ (Volts p-p)}$$

Where V_{IN} is the coil input voltage, L is its inductance, f is the oscillator frequency, and ESR is the equivalent series resistance of the filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C} \text{ where, } Q = t_{DIS} \times \frac{I_{peak}}{2}$$

$$\text{and, } I_{peak} = t_{CHG} \times \frac{V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN}(t_{CHG})(t_{DIS})}{2LC}$$

Where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor (1/2f can be used for nominal calculations).

Oscillator Capacitor, C_X

The oscillator capacitor, C_X, is a non-critical ceramic or silver mica capacitor. C_X can also be calculated by:

$$C_X = \frac{2.14 \times 10^{-6}}{f} - C_{INT} \; (C_{INT} \simeq 5pF, \text{ see text})$$

Where f is the desired operating frequency in Hertz, and C_{INT} is the sum of the stray capacitance on the C_X pin and the internal capacitance of the package. The internal capacitance is typicaly 1pF for the plastic package and 3pF for the CERDIP package. Typical stray capacitances are about 3pF for normal printed circuit board layouts, but will be significantly higher if a socket is used.

CMOS Micropower Step-Up Switching Regulator

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents can flow through the ground connection of the MAX630/4193. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and supply bypassing should be used for the device.

When large values (>50kΩ) are used for the voltage setting resistors, R1 and R2 of Figure 1, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100pF to 10nF in parallel with R1 in Figure 1.

DC-DC Converter Configurations

DC-DC converters come in three basic topologies: buck, boost, and buck-boost (figure 2). The MAX630 is usually operated in the positive voltage boost circuit, where the output voltage is greater than the input.

The boost circuit is used where the input voltage is always less than the desired output and the buck circuit is used where the input is greater than the output. The buck-boost circuit inverts, and can be used with input voltages which are either greater or less than the output.

DC-DC converters can also be classified by the control method. The two most common are pulse width modulation (PWM) and pulse frequency modulation (PFM). PWM switch-mode power supply ICs (of which current mode control is one variant) are well established in high power off-line switchers. Both PWM and PFM circuits control the output voltage by varying duty cycle. In the PWM circuit the frequency is held constant and the width of each pulse is varied. In the PFM circuit, the pulse width is held constant and duty cycle is controlled by changing the pulse repetition rate.

The MAX630 refines the basic PFM by employing a constant frequency oscillator. Its output MOSFET is switched on when the oscillator is high and the output voltage is lower than desired. If the output voltage is higher than desired, the MOSFET output is disabled for that oscillator cycle. This "pulse skipping" varies the average duty cycle, and thereby controls the output voltage.

Note that, unlike the PWM ICs which use an op-amp as the control element, the MAX630 uses a comparator to compare the output voltage to an onboard reference. This reduces the number of external components, and operating current.

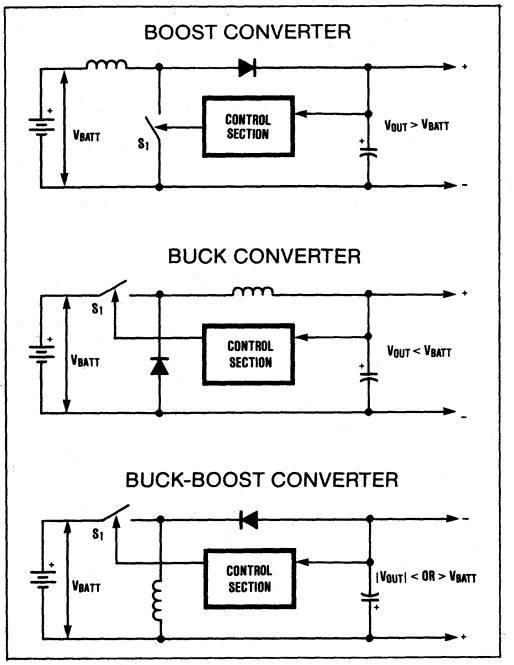


Figure 2. DC-DC Converter Configurations

Typical Applications

+5V to +15V DC-DC Converter

Figure 1 shows a simple circuit which generates +15V at approximately 20mA from a +5V input. The MAX630 has a ±1.5% reference accuracy, so the output voltage has an untrimmed accuracy of ±3.5% if R1 and R2 are 1% resistors. Other output voltages can also be selected by changing the feedback resistors. Capacitor C_X sets the oscillator frequency (47pF=40kHz), while C1 limits output ripple to about 50mV.

With a low cost molded inductor, the circuit's efficiency is about 75%, but an inductor with lower series resistance such as the Dale TE3Q4TA increases efficiency to around 85%. A key to high efficiency is that the MAX630 itself is powered from the +15V output. This provides the onboard N-channel output device with 15V gate drive, lowering its ON resistance to about 4 ohms. When +5V power is first applied, current flows through L1 and D1, supplying the MAX630 with 4.4V for startup.

CMOS Micropower Step-Up Switching Regulator

+5V to ±15V DC-DC Converter

The circuit in Figure 3 is similar to that of Figure 1 except that two more windings are added to the inductor. The 1408 (14mm x 8mm) pot core specified is an IEC standard size available from many manufacturers (see Table 1). The -15V output is semi-regulated, typically varying from -13.6V to -14.4V as the +15V load current changes from no load to 20mA.

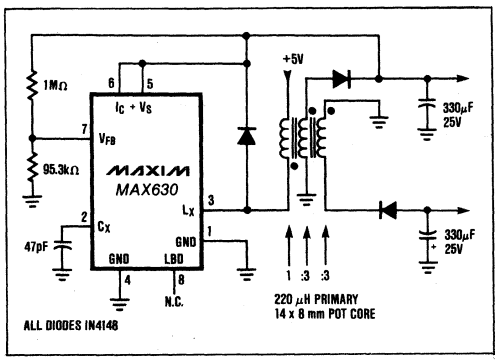


Figure 3. +5V to ±15V Converter

2½ Watt 3V to 5V DC-DC Converter

Some systems, although battery powered, need high currents for short periods, and then shutdown to a low power state. The extra circuitry of Figure 4 is designed to meet these high current needs. Operating in the buck-boost or flyback mode, the circuit converts -3V to +5V. The left side of the figure is similar to Figure 1, and supplies 15V for the gate drive of the external power MOSFET. This 15V gate drive ensures that the external device is completely turned on and has low ON resistance.

The right side of Figure 4 is a -3V to +5V buck-boost converter. This circuit has the advantage that when the MAX630 is turned off the output voltage falls to 0V, unlike the standard boost circuit where the output voltage is V_{BATT}-0.6V when the converter is shutdown. When shutdown, this circuit uses less than 10uA, with most of the current being the leakage current of the power MOSFET.

The inductor and output filter capacitor values have been selected to accomodate the increased power levels. With the values indicated, this circuit can supply up to 500mA at 5V, with an efficiency of 85%. Since the left side of the circuit powers only the right hand MAX630, the circuit will start up with battery voltages as low as 1.5V, independent of the loading on the +5V output.

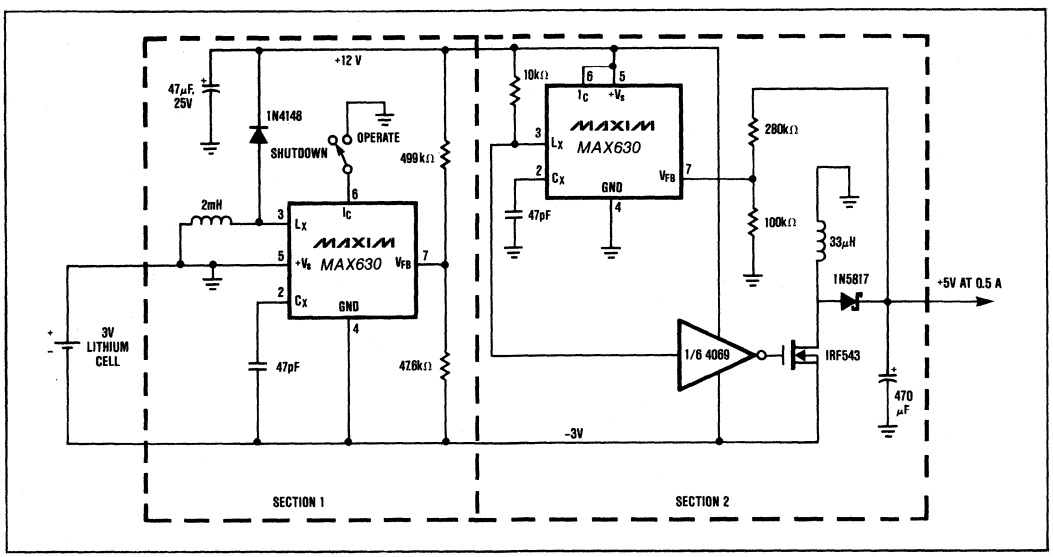


Figure 4. High Power 3V to 5V Converter with Shutdown

CMOS Micropower Step-Up Switching Regulator

+3V Battery to +5V DC-DC Converter

A common power supply requirement involves conversion of a 2.4 or 3V battery voltage to a 5V logic supply. The circuit in figure 5 converts 3V to 5V at 40mA with 85% efficiency. When I_C (pin 6) is driven low, the output voltage will be the battery voltage minus the drop across diode D1.

The optional circuitry using C1, R3, and R4 lowers the oscillator frequency when the battery voltage falls to 2.0V. This lower frequency maintains the output power capability of the circuit by increasing the peak inductor current, compensating for the reduced battery voltage.

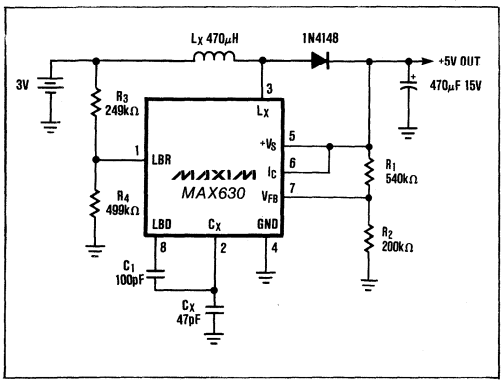


Figure 5. 3V to 5V Converter with Low-Battery Frequency Shift

Uninterruptable +5V Supply

In Figure 6 the MAX630 provides a continuous supply of regulated +5V, with automatic switch-over between line power and battery backup. When the line powered input voltage is at +5V, it provides 4.4V to the MAX630 and trickle charges the battery. If the line powered input falls below the battery voltage, the 3.6V battery supplies power to the MAX630, which boosts the battery voltage up to +5V, thus maintaining a continuous supply to the uninterruptable +5V bus. Since the +5V output is always supplied through the MAX630, there are no power spikes or glitches during power transfer.

The MAX630's low battery detector monitors the line powered +5V, and the LBD output can be used to shut down unnecessary sections of the system during power failures. Alternatively, the low battery detector could monitor the Nicad battery voltage and provide warning of power loss when the battery is nearly discharged.

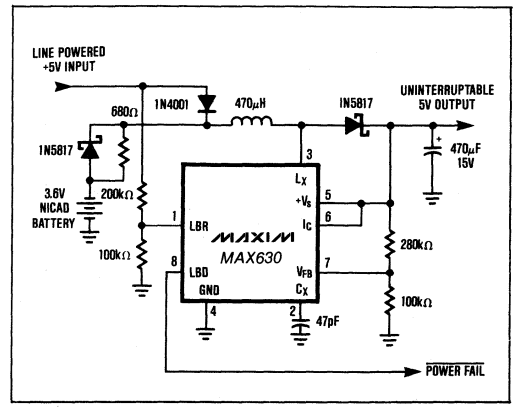


Figure 6. Uninterruptable +5V Supply

Unlike battery backup systems that use 9V batteries, this circuit does not need +12 or +15V to recharge the battery. Consequently, it can be used to provide +5V backup on modules or circuit cards which only have 5V available.

9V Battery Life Extender

Figure 7's circuit provides a minimum of 7V until the 9V battery voltage falls to less than 2V. When the battery voltage is above 7V the MAX630's I_C pin is low, putting it into the shutdown mode which draws only 10nA. When the battery voltage falls to 7V, the MAX8212 Voltage Detector's output goes high, enabling the MAX630. The MAX630 then maintains the output voltage at 7V even as the battery voltage falls below 7V. The low battery detector (LBD) is used to decrease the oscillator frequency when the battery voltage falls to 3V, thereby increasing the output current capability of the circuit.

Note that this circuit (with or without the MAX8212) can be used to provide 5V from 4 alkaline cells. The initial voltage is approximately 6V, and the output is maintained at 5V even when the battery voltage falls to less than 2V.

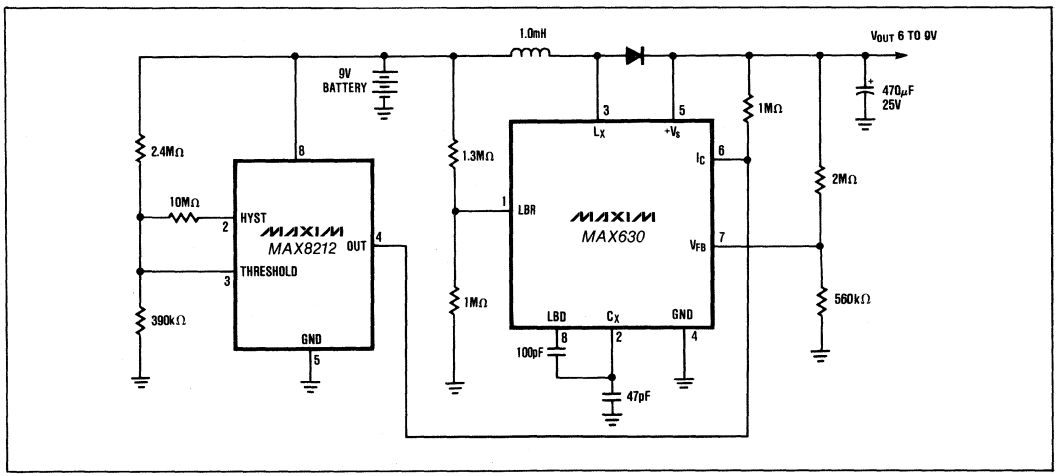


Figure 7. Battery Life Extension Down To 3V In

Dual Tracking Regulator

A MAX634 Inverting Regulator is combined with a MAX630 in Figure 8 to provide a dual tracking ±15V output from a 9V battery. The reference for the -15V output is derived from the positive output via R3 and R4. Both regulators are set to maximize output power at low battery voltage by reducing the oscillator frequency, via LBR, when V_{BATT} falls to 7.2V.

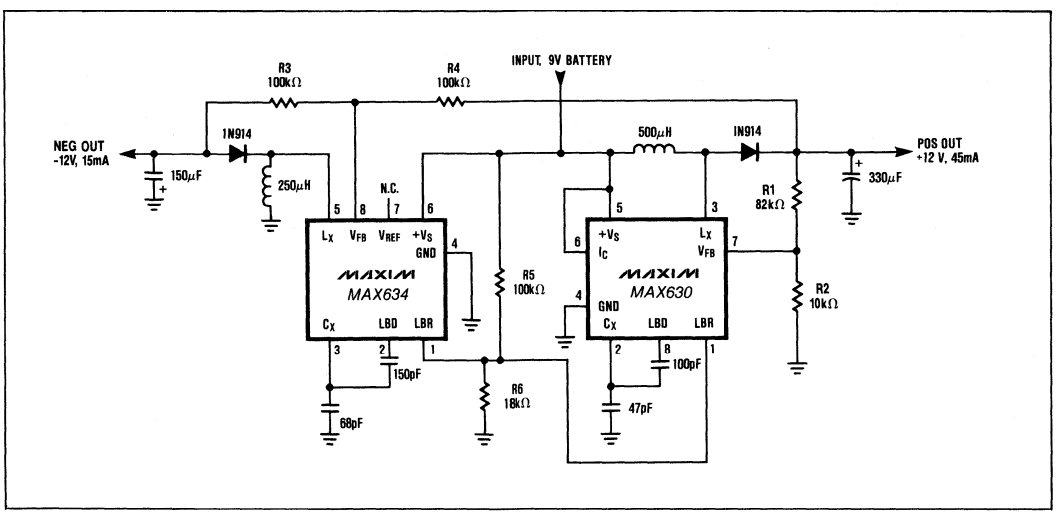


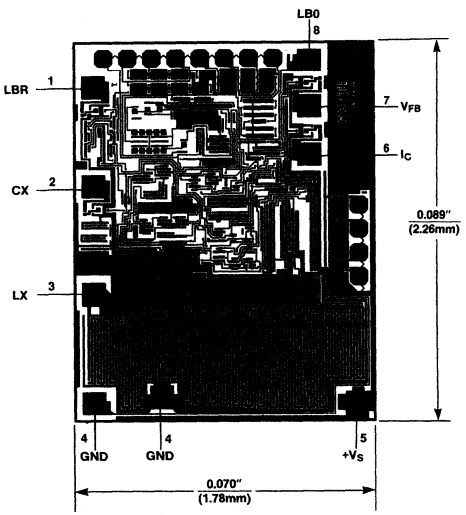
Figure 8. ±12V Dual Tracking Regulator

CMOS Micropower Step-Up Switching Regulator

Table 2. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Chip Topography



CMOS Fixed/Adjustable Output Step-Up Switching Regulators

General Description

The MAX631, MAX632, and MAX633 are +5V, +12V, and +15V fixed output, step-up DC-DC converters for use in low-power, high-efficiency switching regulator applications. The only external components required are an output filter capacitor and a low-cost inductor. Included on-chip are low battery detection circuitry and a charge pump output for generating a negative voltage in dual-supply applications.

Though most simply used as fixed output regulators, the MAX631/632/633 can also be set for other output voltages by adding an external voltage divider.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

Minimum Component, High-Efficiency DC-DC Converters

Portable Instruments

Rechargeable and Primary Battery Power Conversion

Uninterruptable On-Board Power Supplies

Card Level Multiple Power Conversion

Features

- ♦ **Fixed +5V, +12V, +15V Output Voltages**
- ♦ **Adjustable Output with 2 Resistors**
- ♦ **80% Typ Efficiency**
- ♦ **Only 2 External Components**
- ♦ **Charge Pump for Negative Output**
- ♦ **135µA Typ Operating Current**

Ordering Information

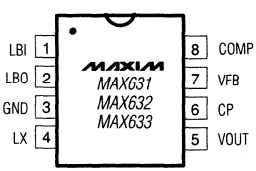
PART*	TEMP. RANGE	PIN-PACKAGE
MAX631XCPA	0°C to +70°C	8 Plastic DIP
MAX631XCSA	0°C to +70°C	8 Narrow SO
MAX631XC/D	0°C to +70°C	Dice
MAX631XEPA	-40°C to +85°C	8 Plastic DIP
MAX631XESA	-40°C to +85°C	8 Narrow SO
MAX631XEJA	-40°C to +85°C	8 CERDIP
MAX631XMJA	-55°C to +125°C	8 CERDIP
MAX632XCPA	0°C to +70°C	8 Plastic DIP
MAX632XCSA	0°C to +70°C	8 Narrow SO
MAX632XC/D	0°C to +70°C	Dice
MAX632XEPA	-40°C to +85°C	8 Plastic DIP
MAX632XESA	-40°C to +85°C	8 Narrow SO
MAX632XEJA	-40°C to +85°C	8 CERDIP
MAX632XMJA	-55°C to +125°C	8 CERDIP

** X = A for 5% Output Accuracy. X = B for 10% Accuracy.*

Ordering Information continued on last page.

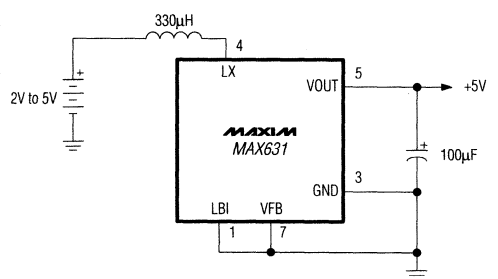
Pin Configuration

Top View



DIP/SO

Typical Operating Circuit



+5V OUTPUT DC-DC CONVERTER

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VOUT ..... +18V
Output Voltage, LX and LBO ..... +18V
Input Voltage, LBI and VFB ..... -0.3V to (VOUT + 0.3V)
LX Output Current ..... 450mA Peak
LBO Output Current 50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
  SO (derate 6mW/°C above +50°C) 450mW
  CERDIP (derate 8mW/°C above +50°C) 800mW

Operating Temperature Range
  MAX63_XC ..... 0°C to +70°C
  MAX63_XE ..... -40°C to +85°C
  MAX63_XM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range		Voltage at VOUT Over Temperature (C, E) Over Temperature (M)	 2.0 2.4		 16.5 16.5	V
Start-up Voltage		Voltage at VOUT T_A = +25°C Over Temperature (C, E) Over Temperature (M)	 1.5 1.8 2.0	 1.3		V
Supply Current	I_S	LX off, Over Temperature VOUT= +5V, MAX631 VOUT = +12V, MAX632 VOUT = +15V, MAX633		 0.135 0.5 0.75	 0.4 2.0 2.5	mA
Reference Voltage (Internal)		T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage		No Load, VFB = GND Over Temperature MAX631A, MAX632A, MAX633A } 5% Output Accuracy MAX631B, MAX632B, MAX633B } 10% Output Accuracy	 4.75 11.4 14.25 4.5 10.8 13.5	 5.0 12.0 15.0 5.0 12.0 15.0	 5.25 12.6 15.75 5.5 13.2 16.5	V
Efficiency				80		%
Line Regulation (Note 1)		+0.5VOUT<+V_S<VOUT		0.08		%VOUT
Load Regulation (Note 1)		V_S = +0.5VOUT, P_{OUT} = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f_O	VOUT = +5V MAX631A MAX631B VOUT = +12V MAX632A MAX632B VOUT = +15V MAX633A MAX633B	 40 35 45.5 40 45.5 40	 45 45 50 50 50 50	 50 60 56 65 56 65	kHz
Oscillator Frequency Tempco				-60		Hz/°C
Oscillator Duty Cycle		MAX631, VOUT = +5V MAX632, VOUT = +12V MAX633, VOUT = +15V	40 40 40	50 50 50	60 60 60	%
LX On Resistance	R_{ON}	I_X = 100mA, VOUT = +5V VOUT = +15V		6 3.5	12 7	Ω

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Leakage Current	I_{XL}	V4 = +16.5V T_A = +25°C Over Temperature (C, E) Over Temperature (M)		0.01	1.0 30 100	µA
Diode Forward Voltage	V_F	I_F = 100mA			1.0	V
CP On Resistance		VOUT = +5V, IOUT = ±10mA VOUT = +15V, IOUT = ±30mA		70 30	140	Ω
VFB Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Input Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V2 = +0.4V, V1 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V2 = +16.5V, V1 = +1.4V		0.01	3.0	µA

Note 1: Guaranteed by correlation with DC pulse measurements.

Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (1.31V), LBO sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when LBI is below 1.31V.
3	GND	Ground
4	LX	This pin drives the external inductor with an internal N-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 425mA.
5	VOUT	The regulated DC-DC converter output.
6	CP	The Charge Pump output is a low impedance buffer which swings from GND to VOUT at the oscillator frequency. 2 external capacitors and diodes can be connected to generate a negative output voltage (Figure 3).
7	VFB	When VFB is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected from VOUT to VFB and GND, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response.

Typical Applications

Basic Step-Up Circuits

Figure 1 shows the basic boost or step-up circuit for the MAX631/632/633. The circuit corresponds to Table 1 which shows values for typical input voltages and output currents.

Table 1. Inductor Selection for Common Designs

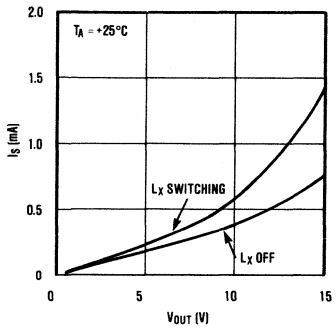
V_{IN} (V)	VOUT (V)	IOUT (mA)	EFF. (%)	INDUCTOR P.N. (Note 2)	µH	Ω
2	5	5	78	CB 6860-21	470	0.4
2	5	10	74	G 1B253	250	0.44
2	5	15	61	G 1B103	100	0.25
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55
3	12	5	79	CB 6860-19	330	0.35
3	12	10	79	CB 7070-28	180	0.48
5	12	12	88	CB 6860-21	470	0.4
5	12	25	87	CB 6860-19	330	0.35
3	15	5	73	CB 7070-29	220	0.55
3	15	8	71	CB 7070-27	150	0.43
5	15	10	85	CB 6860-21	470	0.4
5	15	15	85	CB 6860-19	330	0.35
8	15	35	90	G 1B503	500	0.56

Note 2: CB = Cadell-Burns, NY, (516) 746-2310
G = Gowanda Electronics Corp., NY, (716) 532-2234
Other Manufacturers listed in Table 2.

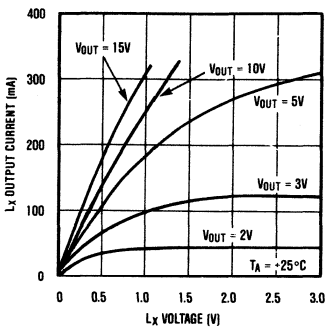
CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Typical Operating Characteristics

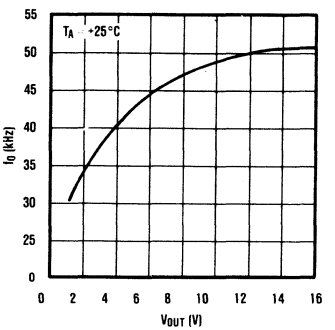
SUPPLY CURRENT vs. OUTPUT VOLTAGE



LX OUTPUT CURRENT vs. VOUT



OSCILLATOR FREQUENCY vs. OUTPUT VOLTAGE



Detailed Description

The operation of the MAX631/632/633 can best be understood by examining the regulating loop of Figure 1. When the output voltage drops below the preset (or externally set) value, the Error Comparator switches high and connects the internal 45kHz Oscillator to the gate of the LX output driver, N1. N1 is an N-channel MOSFET with a typical on resistance of 6Ω and a current rating of 150mA. The following equation provides a good rule of thumb to see if the MAX631/632/633 can provide the desired output current without exceeding the current rating of N1:

$$\frac{8\,(V_{OUT} - V_{IN})\,I_{OUT}}{V_{IN}} \leq 450mA$$

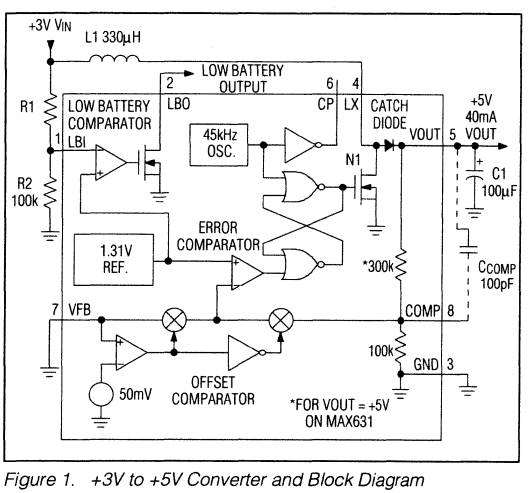


Figure 1. +3V to +5V Converter and Block Diagram

A low output voltage turns N1 on and off at the internal clock frequency. During each on half-cycle, the current through the inductor rises linearly, storing energy in the coil. During each off half-cycle, the coil's magnetic field collapses and voltage across the inductor reverses sign. The voltage at LX then rises until the internal diode is forward based, delivering power to the output. When the output voltage reaches the desired level, the Error Comparator inhibits N1 until the load discharges the output filter capacitor (C1) to less than the desired output level.

VIN, Bootstrapped Operation

The MAX631/632/633 does not have a V_{IN} pin. Input power to start the DC-DC converter is supplied via the external inductor to the VOUT pin. Once the converter has started, it is then powered from its own output. This "bootstrap" design ensures that the output MOSFET, N1, will have maximum gate drive and, hence, a minimum R_{ON}. It also allows the converter to start at lower input voltages.

VIN, Greater Than VOUT

If the regulator's input voltage is more than one forward diode drop greater than the desired output voltage, N1 will not turn on. Current will still be supplied to the load directly through the inductor and the internal diode, but without regulation. As long as the input is more than 0.6V above the desired output, the actual output voltage will be equal to the input voltage minus 0.6V.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX631, +12V for the MAX632, and +15V for the MAX633), VFB is connected to GND, and no external resistors are required. For an output voltage other than the preset value, an external voltage divider (R3 and R4, Figure 2) is required. VOUT is set as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4\left(\frac{VOUT}{1.31V} - 1\right)$$

Table 1 shows nominal inductor parameters for a variety of input and output voltages. Values are given for both maximum output and maximum efficiency designs. When noise is not critical, a low-cost bobbin inductor will suffice. For higher power circuits or when low EMI and noise are required, pot cores and toroids should be used. (See Tables 1 and 2 for typical part numbers and manufacturers.)

Table 2. Coil and Core Manufacturers (Note 3)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
BOBBIN INDUCTORS		
Dale	IHA-104	500µH, 0.5Ω
Caddell-Burns	7070-29	220µH, 0.55Ω
Gowanda	1B253	250µH, 0.44Ω
TRW	LL-500	500µH, 0.75Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82Ω
TRW	MH-1	600µH, 1.9Ω
Gowanda	050AT1003	100µH, 0.05Ω
FERRITE CORES AND TOROIDS (Note 4)		
Siemens	B64290-K38-X38	Tor. Core, 4µH/T^2
Magnetics	555.130	Tor. Core, 53nH/T^2
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T^2

Note 3: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 4: Permag Corp. is a distributor for many of the listed core and toroid manufacturers. (516) 822-3311.

Output Filter Capacitor

The MAX631/632/633's output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost are typically achieved with a high-quality aluminum electrolytic, in the 100µF to 500µF range, in parallel with a 0.1µF ceramic capacitor.

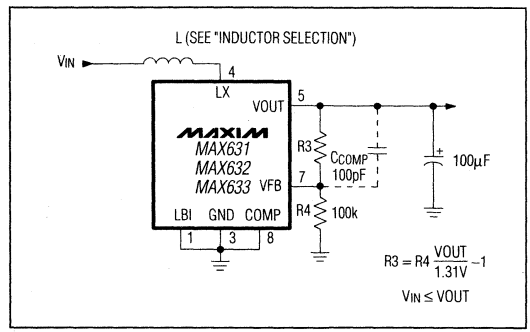


Figure 2. Connections for Adjustable Output

Catch Diode

The MAX631 series regulators contain an internal "catch" diode and, therefore, require no external diode for most applications. However, an external diode can be connected in parallel with the internal diode at the LX and VOUT pins. For example, a Schottky diode with a low forward voltage drop will provide some improvement in efficiency.

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection to the MAX631/632/633. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power-supply bypassing should be used.

When the value of the voltage setting resistors (R3 and R4, Figure 2) exceed 50kΩ, stray capacitance at the VFB input can add a "lag" to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between VOUT and COMP again adds a "lead" to the regulator's response.

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input, LBI, with the internal 1.31V bandgap reference. The Low Battery Detector Output, LBO, goes low whenever the input voltage at LBI is less than 1.31V. The Low Battery detection voltage is set by resistors, R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R1 = R2\left(\frac{VLB}{1.31V} - 1\right)$$

(VLB is the desired Low Battery detection voltage)

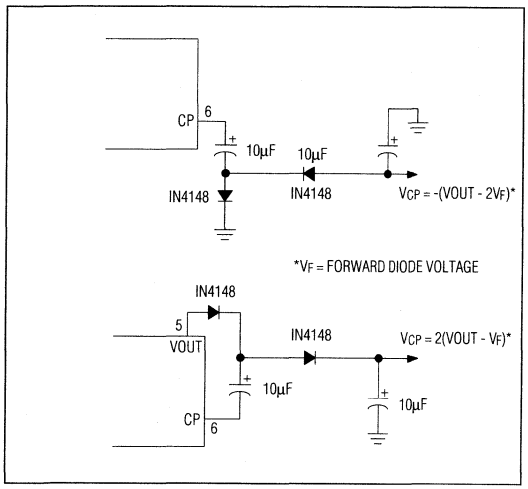


Figure 3. Using the Charge Pump (CP) output as a voltage inverter and/or doubler. Both circuits can be used together.

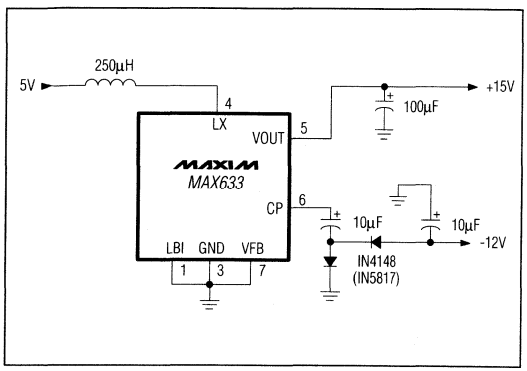


Figure 4. +5V to +15V/-12V Converter

Negative Output Voltage

The Charge Pump (CP) output is a low impedance buffer which swings from ground to VOUT at the oscillator frequency. Two external capacitors and diodes can be connected, as shown in Figure 3, to generate a negative output voltage of –(VOUT – 1.2V) or a positive output of 2(VOUT – 1.2V). 1.2V is the forward drop of 2 silicon diodes. Both circuits can be used at once if desired. With 10µF capacitors, the output impedance of V_{CP} is about 30Ω. If space is critical, the capacitors can be reduced, but with a slight increase in output impedance and V_{CP} output ripple.

The circuit shown in Figure 4 provides approximately ±10mA with VOUT = +15V, and ±15mA if VOUT = +12V. The magnitude of the negative output is about 3V less than VOUT due to the forward voltage drop of the 1N4148 diodes and the output impedance of CP. Using Schottky diodes (IN5817) will increase the absolute value of the negative output by about 1V. The performance of the CP output is shown in Figure 5.

What Value of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is greater than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or range of input voltage), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input

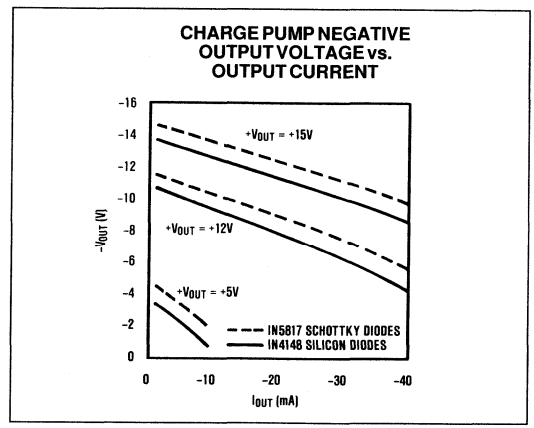


Figure 5. Charge Pump Negative Output Voltage vs. Current

voltage, determines how much energy will be stored in the coil.

The inductor must meet four electrical criteria:

[ ] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case conditions for high power-switch transistor on time and high input voltage.

[ ] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[ ] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for digital circuits; toroid or pot core types work well for EMI-sensitive analog circuits.

[ ] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX631/632/633 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst-case is:

[ ] Maximum load current
[ ] Minimum supply voltage
[ ] Maximum inductor value, including tolerance
[ ] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
[ ] Worst-case low on time

Inductor Value- High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. All kinds of odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values may result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

[ ] Maximum supply voltage
[ ] Minimum inductor value, including tolerance
[ ] Minimum on resistance of the switch
[ ] Low switching frequency (or maximum switch on-time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1]\quad I_{pk} = \frac{VOUT + V_{DIODE} - V_{IN}}{(0.25)\,(V_{IN} - V_{SW})}\,(IOUT)$$

$$[2]\quad L = \frac{V_{IN} - V_{SW}}{I_{pk}}\,(t_{ON})$$

Where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with V_{IN} = +15V and 1.5V max, 0.5V min with V_{IN} = +5V.

Example: A +5V 10% input must be converted to +15V at 15mA. A Schottky diode (1N5817) and a MAX633B are used.

Calculate maximum inductor value allowed:

$$I_{pk} = \frac{15V + 0.4V - 4.5V}{(0.25)\,(4.5V - 0.75V)}\,(15mA) = 174mA$$

$$L = \frac{4.5 - 0.75}{174mA}\,(8\mu s) = 172\mu H$$

Calculate the minimum inductor value allowed:

I_{pk} = 450mA (from table of max ratings)

$$L = \frac{5.5V - 0.25V}{450mA}\,(12\mu s) = 140\mu H$$

If this minimum value is greater than the maximum value calculated above, an external power MOSFET must be used. See the MAX641/642/643 data sheet.

A value of 160µH would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

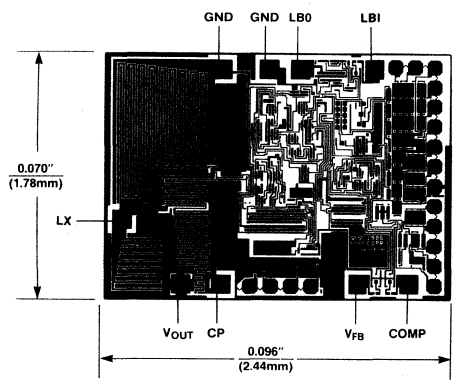
Inductor Saturation

When using off-the-shelf inductors, make sure the peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor. Inductor saturation leads to very high current levels causing excessive power dissipation, poor efficiency, and possible damage to the chip and the catch diode.

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates. It is this rapid current increase and the resultant high peak currents that can damage the inductor and the catch diode.

Chip Topography



Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX633XCPA	0°C to +70°C	8 Plastic DIP
MAX633XCSA	0°C to +70°C	8 Narrow SO
MAX633XC/D	0°C to +70°C	Dice
MAX633XEPA	-40°C to +85°C	8 Plastic DIP
MAX633XESA	-40°C to +85°C	8 Narrow SO
MAX633XEJA	-40°C to +85°C	8 CERDIP
MAX633XMJA	-55°C to +125°C	8 CERDIP

** X = A for 5% Output Accuracy. X = B for 10% Accuracy.*

MAXIM

CMOS Micropower Inverting Switching Regulator

General Description

Maxim's MAX634 and MAX4391 CMOS DC-DC regulators are designed for simple, efficient, inverting DC-DC converter circuits. The MAX634 and MAX4391 switching regulators provide all control and power handling functions in a compact 8 pin package: a 1.25V bandgap reference, an oscillator, a comparator for output voltage regulation, and a 525mA P-channel output MOSFET. A second comparator is also provided for convenient low battery detection.

The operating current is typically 100μA and is nearly independent of output switch current and duty cycle, thus ensuring high efficiency even in low power battery operated systems. Operating in the inverting configuration, the MAX634 and MAX4391 can convert a positive input voltage in the range of +3V to 16.5V to any negative output voltage up to -20V.

These devices are pin compatible enhancements of the Raytheon bipolar circuit, RC4391. Improvements include significantly higher efficiency, extended low voltage operation and improved output voltage accuracy (MAX634).

Maxim manufactures a broad line of DC-DC converters, including the MAX635, MAX636, and MAX637; which reduce the external component count in fixed -5V, -12V, and -15V output DC-DC converter circuits. See Table 2 on the last page of this data sheet for a summary of other Maxim DC-DC converters.

Applications

High Efficiency Battery Powered DC-DC Converters

Board Level, Local Power Supply Generation

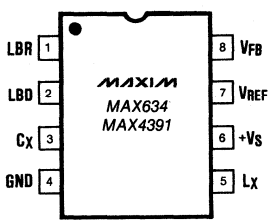
Regulated Negative Output Power Supplies

+5V to ±12V or ±15V Power Conversion

Regulated Voltage Inverters

Pin Configuration

Top View



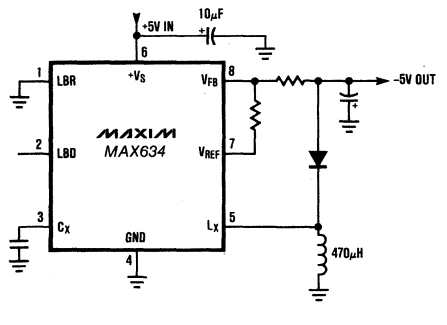
Features

- Converts Positive Voltage to Negative Voltage
- Low Operating Current—100μA
- Compact 8 Pin MiniDIP and SO Packages
- High Efficiency—85% Typical
- Low Battery Detector
- 4% Output Voltage Accuracy (MAX634)
- +3V to +16.5V Input Voltage Range
- Adjustable Output Voltage
  - —Up to -20V with Simple Coil
  - —Virtually Unlimited Voltage with Transformer

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX634C/D	0°C to +70°C	Dice
MAX634CPA	0°C to +70°C	8 Lead Plastic DIP
MAX634CSA	0°C to +70°C	8 Lead Small Outline
MAX634EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX634ESA	-40°C to +85°C	8 Lead Small Outline
MAX634EJA	-40°C to +85°C	8 Lead CERDIP
MAX634MJA	-55°C to +125°C	8 Lead CERDIP
MAX4391C/D	0°C to +70°C	Dice
MAX4391CPA	0°C to +70°C	8 Lead Plastic DIP
MAX4391CSA	0°C to +70°C	8 Lead Small Outline
MAX4391EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX4391ESA	-40°C to +85°C	8 Lead Small Outline
MAX4391EJA	-40°C to +85°C	8 Lead CERDIP
MAX4391MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



+5V to -5V Converter

CMOS Micropower Inverting Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) ..... +18V
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Operating Temperature Range
MAX634C, MAX4391C ..... 0°C to +70°C
MAX634E, MAX4391E ..... -40°C to +85°C
MAX634M, MAX4391M ..... -55°C to +125°C

Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW
Input Voltage, Pins 1, 3, 8 (Note 2) ..... -0.3V to $+V_S$ +0.3V
L_X Output Current ..... 525mA Peak
LBD Output Current 50mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX634			MAX4391			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage (Note 1)	$+V_S$		2.3		16.5	4.0		16.5	V
Supply Current	I_{IN}	No External Loads $+V_S$ = 4.0V $+V_S$ = 16.5V		70 150	150 500		90 170	250 500	µA
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V $V_{OUT\ nom}$ = -15.0V	-5.20 -15.70		-4.80 -14.30	-5.35 -15.85		-4.65 -14.15	V
Line Regulation (Note 4)		$V_{OUT\ nom}$ = -5.0V V_{IN} = 5.0V to 15V			2.0			3.0	$\%V_{OUT}$
Load Regulation (Note 4)		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW $V_{OUT\ nom}$ = -15.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW			0.4 0.14			0.4 0.14	$\%V_{OUT}$
Reference Voltage			1.22	1.25	1.28	1.18	1.25	1.32	V
Switch Current	I_{SW}	Pin 5 = 5.0V	75	150		75	150		mA
Switch Leakage Current	I_{CO}	Pin 5 = -18V, $+V_S$ = 6V		0.01	1.0		0.01	5.0	µA
Capacitor Charging Current	I_{CX}			30			30		µA
C_X + Threshold Voltage				$+V_S$ - 0.1			$+V_S$ - 0.1		V
C_X - Threshold Voltage				0.1			0.1		V
Operating Frequency Range (Note 3)	F_O		0.1		75	0.1		75	kHz
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1000		250	600		µA
Low Battery Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V		0.01	3.0		0.01	5.0	µA
Low Battery Input Threshold	V_{LBR}			1.25			1.25		V
Low Battery Input Bias Current	I_{LBR}			0.01	10		0.01	10	nA
Feedback Input Bias Current	I_{FB}			0.01	10		0.01	10	nA
Efficiency		Figure 2		80			80		%

Note 1: In addition to the Absolute Maximum rating of +18V, the input voltage also must not exceed 24 - $|-V_{OUT}|$.
Note 2: The input voltage limit may be exceeded provided input current is limited to less than 1mA.
Note 3: The operating frequency range is guaranteed by design and verified with sample testing.
Note 4: Guaranteed by correlation with DC pulse measurements.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, full operating temperature range unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX634 MIN.	MAX634 TYP.	MAX634 MAX.	MAX4391 MIN.	MAX4391 TYP.	MAX4391 MAX.	UNITS
Supply Voltage (Note 5)	$+V_S$		2.6		16.5	4.0		16.5	V
Supply Current	I_{IN}	No External Loads $+V_S$ = 4.0V $+V_S$ = 16.5V			150 500			250 500	µA
Reference Voltage	V_{REF}		1.18	1.25	1.32	1.13	1.25	1.36	V
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V $V_{OUT\ nom}$ = -15.0V	-5.25 -16.0		-4.75 -14.0	-5.5 -16.5		-4.5 -13.5	V
Line Regulation		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 5.0V to 15V			3.0			4.0	$\%V_{OUT}$
Load Regulation		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW $V_{OUT\ nom}$ = -15.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW			0.5 0.3			0.5 0.3	$\%V_{OUT}$
Switch Leakage Current	I_{CO}	Pin 5 = -18V, $+V_S$ = 6V		0.01	20			30	µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500			250			µA
Low Battery Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V			3			5	µA

Note 5: In addition to the Absolute Maximum rating of +18V, the input voltage also must not exceed 24 - | $-V_{OUT}$|.

Pin Description

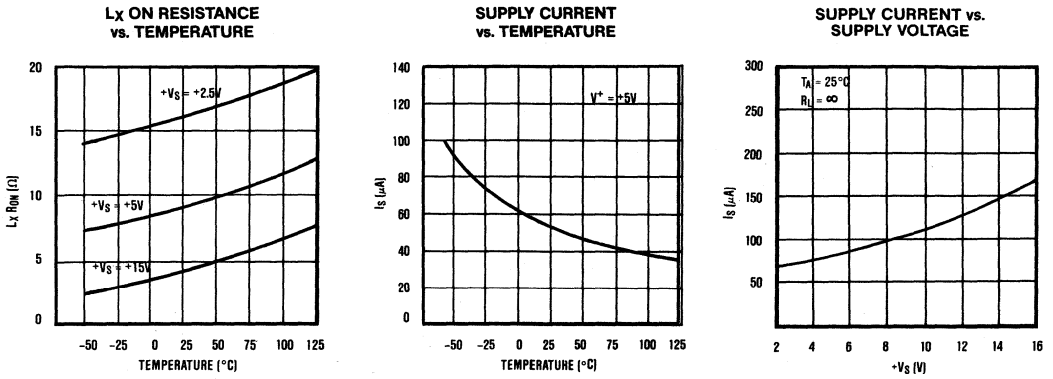
4

PIN	NAME	FUNCTION
1	LBR	Low Battery Detection comparator input. The LBD output, pin 2, sinks current when this pin is below the low battery detector threshold of 1.25V.
2	LBD	The Low Battery Detector output is an open drain N-channel MOSFET which sinks current when the LBR input, pin 1, is below 1.25V.
3	C_X	An external capacitor connected between this terminal and ground sets the oscillator frequency. 47pF = 40kHz
4	GND	Ground.
5	L_X	External Inductor output driver. The internal P-channel MOSFET which drives this pin has an output resistance of 8Ω and a peak current rating of 525mA.

PIN	NAME	FUNCTION
6	$+V_S$	The positive supply voltage, from +3V to +16.5V (MAX634). The total voltage difference between the negative output voltage and the positive input voltage must be less than 24V.
7	V_{REF}	The Voltage REFerence output is 1.25V, generated by an on-chip bandgap reference.
8	V_{FB}	The output voltage is set by an external resistive divider connected to the Voltage Feedback input, pin 8. The MAX634/MAX4391 will pulse the L_X ouput whenever the voltage at this terminal is above Ground.

CMOS Micropower Inverting Switching Regulator

Typical Operating Characteristics



Detailed Description

Principle of Operation

Figure 1 shows a simplified buck-boost voltage inverter, sometimes called an inverting or flyback converter. When the switch is closed a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. The current linearly decays to zero and the magnetic field collapses as the energy stored in the inductor is transferred to the output filter capacitor.

The MAX634 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has fallen below the desired value.

Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive input voltage into a negative voltage. When the feedback voltage at pin 8 is above ground, the P-channel MOSFET at pin 5 turns on during the next low-going period of the oscillator. The P-channel MOSFET delivers current to the external inductor, storing energy in its magnetic field. When the oscillator output goes high, the P-channel MOSFET turns off, and the "kickback" of the inductor pulls current through diode D1, negatively charging the output filter capacitor, C1. This cycle repeats until the output voltage pulls the feedback input, pin 8, below ground.

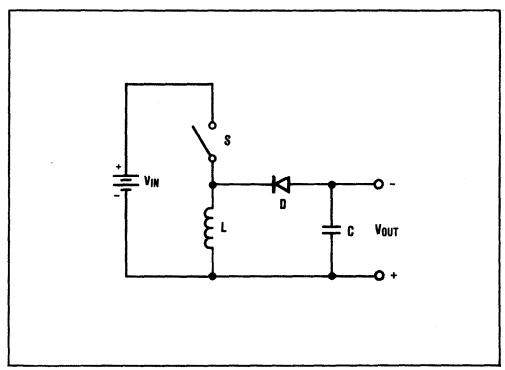


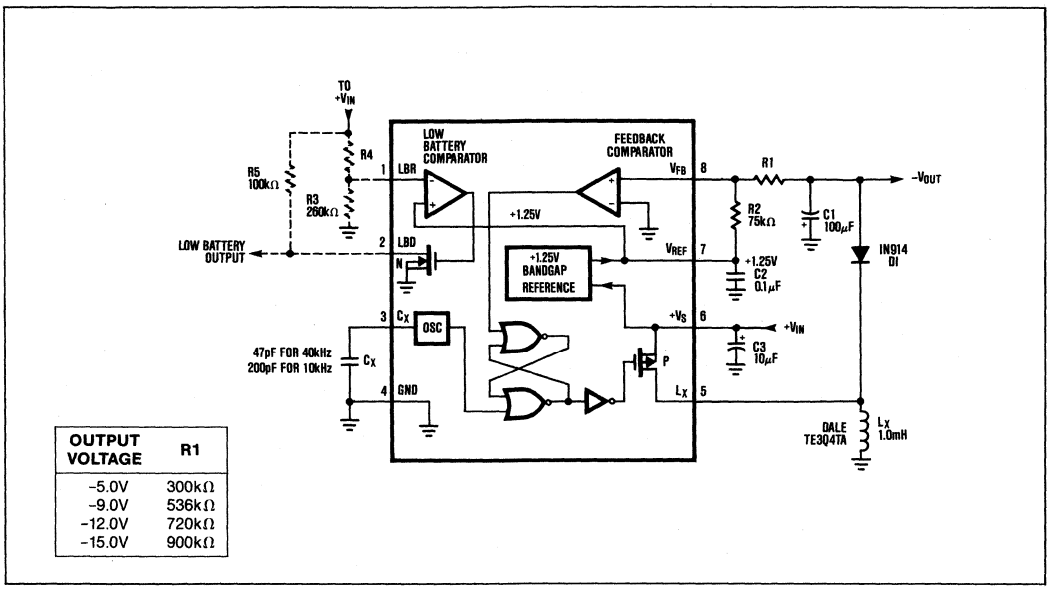
Figure 1. Simplified Voltage Inverter

The NOR gate latch prevents high frequency oscillations by not allowing L_X to switch repeatedly during an oscillator cycle.

The output voltage is determined by the internal 1.25V reference and the ratio of the resistors R1 and R2.

$$V_{OUT} = 1.25V \times \frac{R1}{R2}$$

Capacitor C1 is the output filter capacitor. The capacitance and ESR (equivalent series resistance) of C1 determine the output ripple. C2 and C3 are bypass capacitors; while C_X sets the oscillator frequency.



OUTPUT VOLTAGE	R1
-5.0V	300kΩ
-9.0V	536kΩ
-12.0V	720kΩ
-15.0V	900kΩ

Figure 2. Standard Application Circuit

Oscillator

The MAX634/MAX4391 oscillator uses only one external component, a capacitor C_X connected between pin 3 and Ground. A value of 47pF sets the oscillator frequency to approximately 40kHz.

The oscillator can also be externally driven with a CMOS gate which swings from ground to $+V_S$. The L_X output is always off when the C_X pin is externally driven high.

Low Battery Detector

The Low Battery Detector (LBD) Output (pin 2, Figure 2) sinks current whenever the input voltage at Low Battery Resistor (pin 1) is less than +1.25V. The LBR input is a high impedance CMOS input, with less than 10nA leakage current. The LBD output is an open drain N-channel MOSFET with about 500Ω of output resistance. The operating voltage of the low battery detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between pins 1 and 2.

$$V_{LOBATT} = 1.25V \times (1 + \frac{R4}{R3}) \text{ or,}$$

$$R4 = R3 \times (\frac{V_{LOBATT}}{1.25V} - 1)$$

where V_{LOBATT} is the operating voltage of the low battery detector, and R3 is usually between 10kΩ and 10MΩ, with a typical value being 470kΩ.

External Component Selection

Inductor Value

The available output current from an inverting DC-DC voltage converter is determined by the value of the external inductor, the output voltage, the input voltage, and the operating frequency. The inductor must 1) have the correct inductance, 2) be able to handle the peak currents, and 3) have acceptable series resistance and core losses.

$$L_{MAX} = \frac{(V_{IN}\, T_{ON})^2\, f}{2\, P_{OUT}}$$

$$L_{MIN} = \frac{V_{IN}\, T_{ON}}{I_{MAX}}$$

where I_{MAX} is the maximum allowable peak L_X current (525mA).

Contrary to what most people would expect at first glance, reducing the inductor value increases the available output current: lower L increases the peak current, thereby increasing the available power. If the inductance is too high, the MAX634/MAX4391 will not be able to deliver the desired output power,

CMOS Micropower Inverting Switching Regulator

even with the L_X output turned on with each oscillator cycle. The available output power can be increased by either decreasing the inductance or by decreasing the frequency. Decreasing the frequency increases the on period of the L_X output, thereby increasing the peak inductor current, which in turn increases the available output power since the output power is proportional to the square of the peak inductor current.

The most common MAX634 circuit is the buck-boost voltage inverter (Figure 2). When the P-channel output device is on, the current in the inductor linearly rises since:

$$\frac{di}{dt} = \frac{V}{L}$$

At the end of the on period the current is

$$I_{pk} = \frac{V_{IN}\ T_{on}}{L} = \frac{5V \times 50\mu s}{1mH} = 250mA$$

assuming a 10kHz, 50% duty cycle oscillator and $+V_S = 5V$

The energy in the coil is:

$$E = \frac{1}{2} L\ I_{pk}^2 = 31.2\mu J$$

At maximum load this cycle is repeated 10,000 times per second, and the power transferred through the coil is 10,000 x 31.2μJ = 312mW. If the output voltage is -5V, then 312/5 = 62.5mA of output current is available, ignoring losses and component tolerances. In a practical circuit, 50mA of output current is available at -5V.

The external inductor required by the MAX634/MAX4391 is readily obtained from a variety of suppliers. (See Table 1.)

Types of Inductors

Molded Inductors

These are cylindrically wound coils which look similar to 1 watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types.

Potted Toroidal Inductors

A typical 1mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685" in diameter by 0.385" high and mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode inductors since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes, often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective cross sectional area differs between the post, side, top and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permalloy powder (MPP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Caddell-Burns	6860-19	330μH, 0.33 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Torotel Prod.	PT 53-18	500μH, 5 ohms
FERRITE CORES AND TOROIDS		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

External Diode

In most MAX634 circuits the inductor current returns to zero before L_X turns on for the next output pulse. This allows the use of slow turn-off diodes. On the other hand, the diode current abruptly goes from zero to full peak current each time L_X switches off (Figure 2, D1). To avoid excessive losses during turn-on, the diode must have a fast turn-on time.

The 1N914 or 1N4148 is suitable for low power applications. The 1N5817 series of Schottky diodes or their equivalent are suitable for higher power applications. Rectifier diodes such as the 1N4001 series are unacceptable since their slow turn-on results in excessive losses.

Filter Capacitor

The output filter capacitor (C1 in Figure 2) stores the energy delivered by the inductor, and delivers current to the load. The output voltage ripple is directly affected by the capacitance and the equivalent series resistance (ESR) of the output filter capacitor.

The output voltage ripple has two components, with approximately 90° phase difference. One ripple component is created by the change in stored charge in the capacitor with each output pulse. The other ripple component is the product of the capacitor charge/discharge current times the ESR (effective series resistance) of the capacitor. With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than the ripple from the change in charge.

$$V_{ESR} = I_{pk} \times ESR \text{ (Volts P-P)}$$

$$= \left(\frac{V_{IN}}{2LF}\right) \times ESR \text{ (Volts P-P)}$$

where V_{IN} is the input voltage to the coil, L is the inductance of the coil, f is the oscillator frequency, and ESR is the equivalent series resistance of the output filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C} \text{ where: } Q = t_{DIS} \times \frac{I_{peak}}{2}$$

$$\text{and: } I_{peak} = t_{CHG} \times \frac{V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN}(t_{CHG})(t_{DIS})}{2LC}$$

where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor (1/(2f) can be used for norminal calculations).

Oscillator Capacitor, C_X

The oscillator capacitor can be a low cost ceramic capacitor. If the circuit will be operated over a wide temperature range, an capacitor with a low temperature coefficient of capacitance should be used.

The value of C_X can be calculated using the formula:

$$C_X = \frac{2.14 \times 10^{-6}}{f} - C_{INT}$$

where f is the desired operating frequency in Hertz, and C_{INT} is the sum of the stray capacitance on the C_X pin and the internal capacitance of the package. The internal capacitance is about 1pF for the plastic package and 3pF for the CERDIP package. Typical stray capacitance is about 3pF for normal printed circuit board layouts, but will be significantly higher if a socket is used.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that the peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external current boosting transistors. Inductor saturation leads to very high current levels through the external boost transistors, causing excessive power dissipation, poor efficiency, and possible damage to the inductor and the external transistor.

Test for saturation by applying the maximum load, the maximum input voltage, and (for a safety margin) lowering the clock frequency by 25%. Monitor the inductor current using a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates. It is this rapid current increase and the resultant high peak currents that can damage the inductor and the external boost transistor.

Bypassing and Compensation

The high operating current pulses in the L_X output and the external inductor can cause erratic operation unless the MAX4391/MAX634 is properly bypassed. Connect a 10µF bypass capacitor directly across the MAX4391 between pin 6 ($+V_S$) and pin 4 (Ground) to minimize the inductance and high frequency impedance of the power source. Make sure that the high current ground return path of the inductor does not cause a voltage drop in the MAX4391 ground line.

CMOS Micropower Inverting Switching Regulator

The reference voltage output, pin 7, should also be bypassed to ground to avoid coupling to the high current path that includes the L_X output, the inductor, and its ground return.

With light loads, coupling from the high power circuit into the control circuitry may cause the output pulses to occur in bursts, thereby increasing low frequency ripple and degrading the line and load regulation. Normal operation with evenly distributed output pulses can be restored by adding a 100pF to 10nF compensation capacitor across the feedback resistor, R1. Minimizing the stray capacitance on the V_{FB} terminal will often eliminate the need for this compensation capacitor.

Typical Applications

-5V Output Regulated Voltage Inverter

The standard circuit in Figure 2 will deliver 50mA at -5V. Efficiency is 85% when using a low loss pot core or toroidal inductor such as the Dale TE3Q4TA series. Using a low cost molded inductor with several ohms series resistance reduces the efficiency to 70%.

-12V and -15V Output DC-DC Inverters

The circuit of Figure 2 can also be used for -12V or -15V outputs by simply changing the value of R1 in the feedback network using the formula

$$R1 = \frac{V_{OUT}\ R2}{1.25V}$$

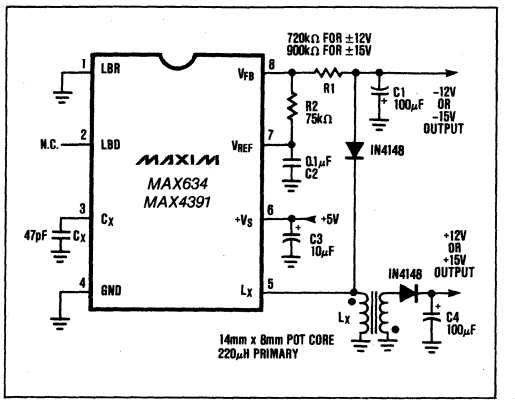


Figure 3. Dual Output, ±12V or ±18V DC-DC Converter

Dual Output, ±12V or ±15V DC-DC Converters

The buck-boost configuration of the MAX634 is well suited for dual output DC-DC converters. As shown in Figure 3, all that is needed is a second winding on the inductor. Typically, this second winding is bifilar (primary and secondary are wound simultaneously using two wires in parallel). The inductor core is usually a toroid or a pot core, see Table 1.

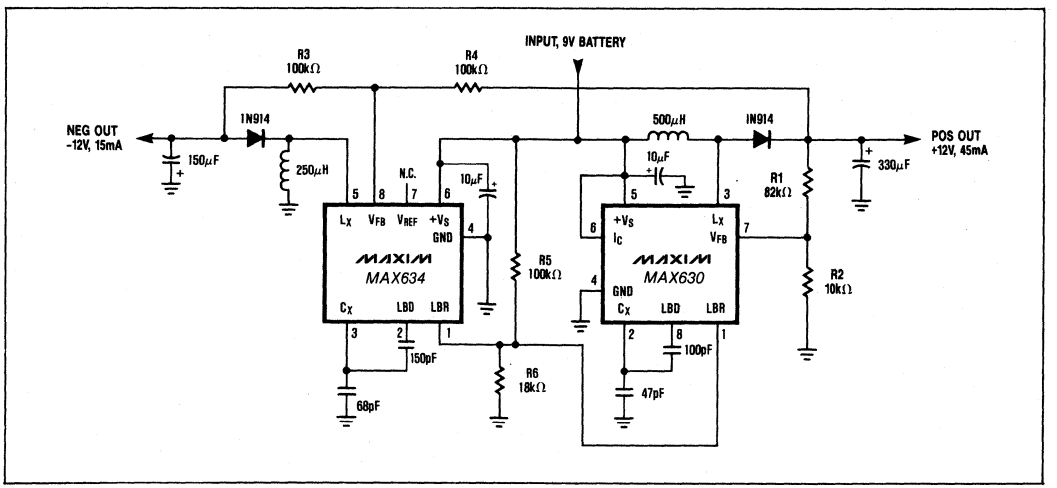


Figure 4. ±12V Dual Tracking Regulator

CMOS Micropower Inverting Switching Regulator

The negative output voltage is fully regulated by the MAX634. The positive voltage is semi-regulated, and will vary slightly with load changes on either the positive or negative outputs. See the MAX630 data sheet for a similar circuit with a fully regulated positive output and a semi-regulated negative output. If both outputs must be fully regulated use both a MAX634 and a MAX630, as shown in Figure 4.

Voltage Inverter

In Figure 5, the negative output voltage tracks the positive input voltage. This circuit performs the same function as Maxim's ICL7660, but with better output regulation and higher output current capability. With the circuit components shown, Figure 5 will deliver approximately 50mA at -9V when the input is +9V, and about 30mA at -5V when the input is +5V.

Input voltage tracking is achieved by using the positive input voltage as the reference instead of the onboard bandgap reference.

The output voltage is set by the input voltage, R1, and R2 as follows:

$$V_{OUT} = -\frac{R2}{R1} \times +V_S$$

Low Power Shutdown

Unlike the MAX630, the MAX634 and MAX4391 do not have a logic level shutdown pin, but a low power mode can easily be implemented as shown in Figure 6. Since the operating current is only 250μA maximum, the GND pin can be driven directly by a CMOS gate or N-channel FET. Drive GND low for normal operation; let it float or drive it high to enter the low power shutdown mode. In low power shutdown the MAX634 circuit draws only the leakage current of the L_X output.

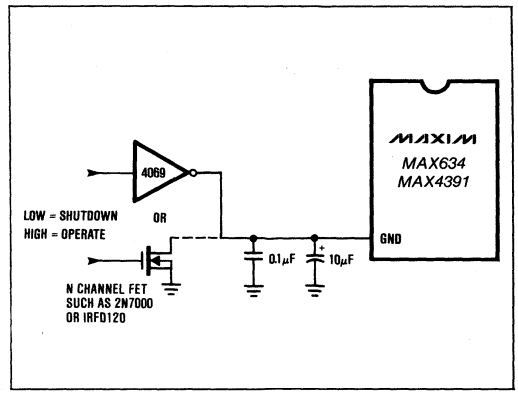


Figure 6. Low Power Shutdown

The Ground pin should be well bypassed and any voltage drop across the CMOS gate adds to the reference voltage, slightly increasing the regulated output voltage.

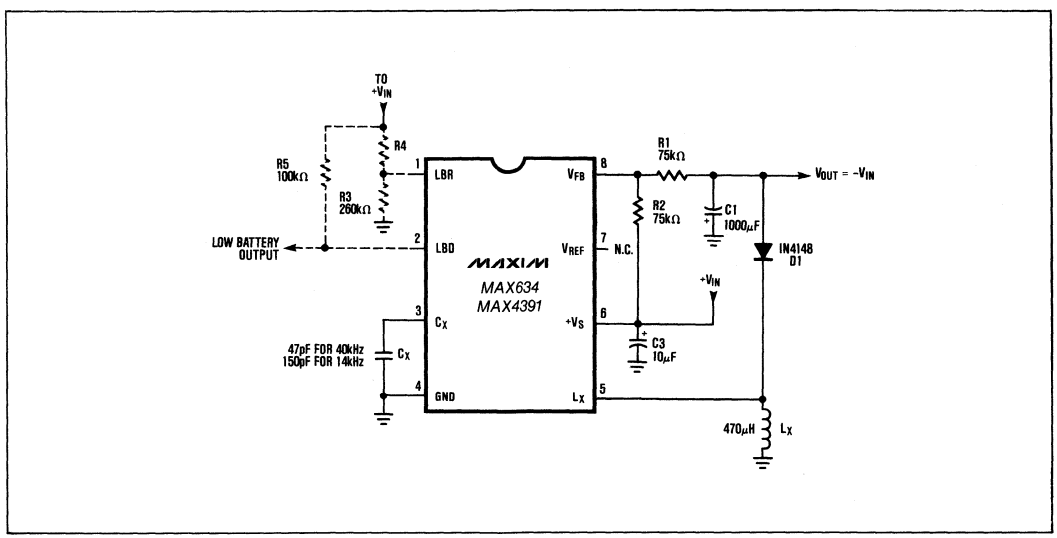
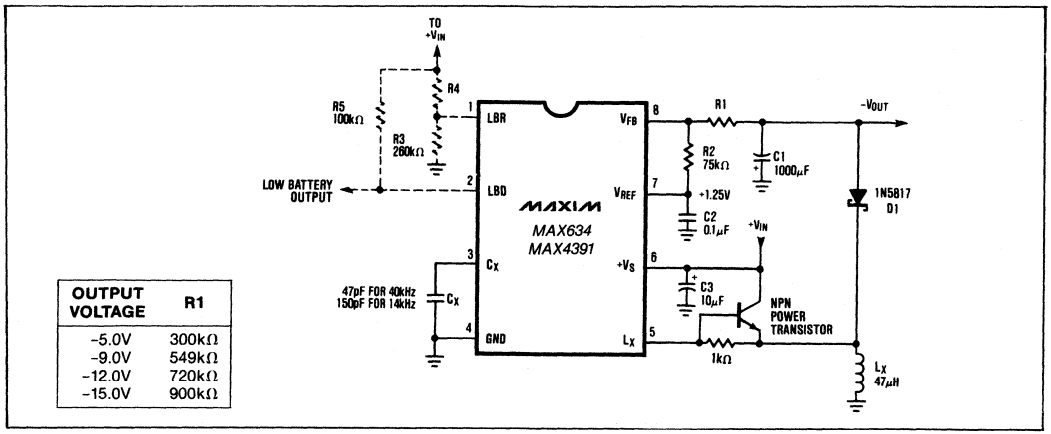


Figure 5. Regulated Voltage Inverter

CMOS Micropower Inverting Switching Regulator



OUTPUT VOLTAGE	R1
-5.0V	300kΩ
-9.0V	549kΩ
-12.0V	720kΩ
-15.0V	900kΩ

Figure 7. Boosting Output Power With External NPN Power Transistor

Boosting Output Power With External Power Devices

The MAX634 and MAX4391 are limited to a maximum switch current of 525mA. If higher current, or output resistance less than the 6 ohms of the MAX634 is required, the circuits of Figures 7, 8, or 9 can be used.

The circuit of Figure 7 uses an NPN bipolar transistor to boost the output current. All of the NPN transistor base current is used to drive the inductor, but the voltage drop across the transistor will be approxmately 0.7V.

The circuit of Figure 8 uses a low resistance N-channel MOSFET in a transformer coupled voltage inverter circuit. This circuit has the advantage that a positive output voltage can also be obtained by simply adding a diode and an output filter capacitor. The -15V output is fully regulated for both line and load variations; the +20V output voltage will varies with changes in load on either the +20V or -15V output, as well as changes in the +5V input. This variation is normally less than 10%.

High Output Voltage

The circuit in Figure 9 converts any positive voltage from +3V to +16V to any desired output voltage, as long as the voltage breakdown of the external P-Channel MOSFET is not exceeded. This circuit is also useful for generating a high power, high efficiency -12V or -15V output using a simple one winding coil.

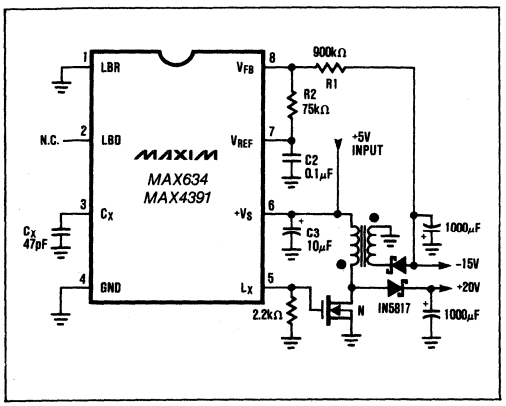


Figure 8. High Power +5V to -15V DC-DC Converter

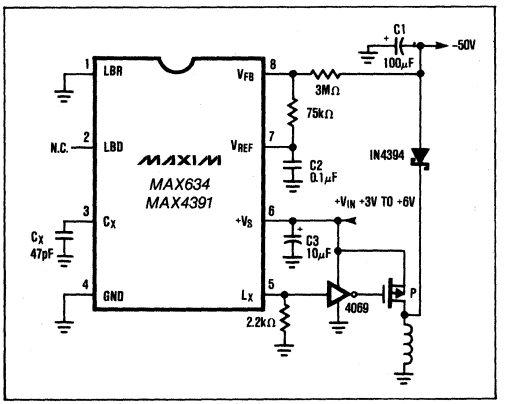


Figure 9. Boosting Voltage External P-Channel MOSFET

Operating with Wide Input Voltage Range

The available output power varies as the square of the input voltage. The Low Battery Detector can compensate for a reduction in input voltage by lowering the oscillator frequency, as shown in Figure 10. With the values shown, the oscillator frequency is 40kHz when the input voltage is above 6V. When the input falls below 6V, the Low Battery Detector (LBD) output goes low, placing the 100pF capacitor in parallel with C_X, reducing the oscillator frequency to 14kHz. This increases the available output power by a factor of 3.

This circuit can be used with any of the other application circuits in this data sheet.

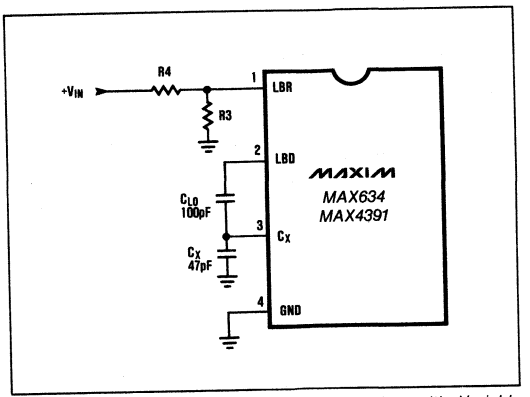
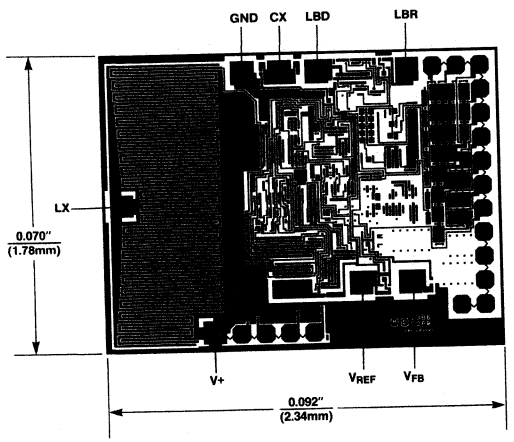


Figure 10. Wide Input Voltage Range Operation with Variable Frequency Oscillator.

Chip Topography



CMOS Micropower Inverting Switching Regulator

Table 2. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Preset/Adjustable Output CMOS Inverting Switching Regulators

General Description

The MAX635/MAX636/MAX637 inverting switching regulators are designed for minimum component DC-DC conversion in the 5mW to 500mW range.

Low power applications require only a diode, output filter capacitor, and a low-cost inductor. An additional MOSFET and driver are needed for higher power applications. Low battery detection circuitry is included on chip.

The MAX635/636/637 are preset for -5V, -12V, and -15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

Minimum Component, High-Efficiency DC-DC Converters

Portable Instruments

Battery Power Conversion

Board Level DC-DC Conversion

Features

- ♦ **Preset -5V, -12V, -15V Output Voltages**
- ♦ **Adjustable Output with 2 Resistors**
- ♦ **85% Typ Efficiency**
- ♦ **Only 3 External Components**
- ♦ **80µA Typ Operating Current**
- ♦ **Low Battery Detector**

Ordering Information

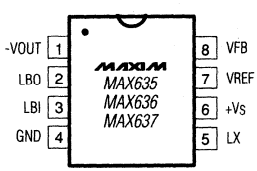
PART*	TEMP. RANGE	PIN-PACKAGE
MAX635XCPA	0°C to +70°C	8 Plastic DIP
MAX635XCSA	0°C to +70°C	8 Narrow SO
MAX635XC/D	0°C to +70°C	Dice
MAX635XEPA	-40°C to +85°C	8 Plastic DIP
MAX635XESA	-40°C to +85°C	8 Narrow SO
MAX635XEJA	-40°C to +85°C	8 CERDIP
MAX635XMJA	-55°C to +125°C	8 CERDIP
MAX636XCPA	0°C to +70°C	8 Plastic DIP
MAX636XCSA	0°C to +70°C	8 Narrow SO
MAX636XC/D	0°C to +70°C	Dice
MAX636XEPA	-40°C to +85°C	8 Plastic DIP
MAX636XESA	-40°C to +85°C	8 Narrow SO
MAX636XEJA	-40°C to +85°C	8 CERDIP
MAX636XMJA	-55°C to +125°C	8 CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.*

Ordering Information continued on last page.

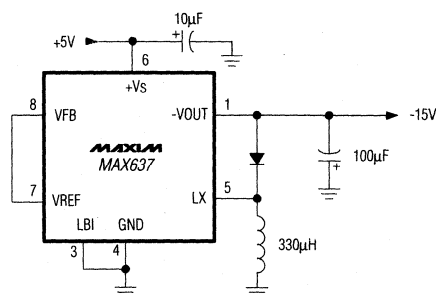
Pin Configuration

Top View



DIP/SO

Typical Operating Circuit



+5V TO -15V CONVERTER

Preset/Adjustable Output CMOS Inverting Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ (Note 1) ..... +18V
Input Voltage, LBO, LBI, VFB ..... -0.3V to ($+V_S$ + 0.3V)
LX Output Current ..... 525mA Peak
LBO Output Current 50mA
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Operating Temperature Range
MAX63_ _C ..... 0°C to +70°C
MAX63_ _E ..... -40°C to +85°C
MAX63_ _M ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISITICS

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	$+V_S$	T_A = +25°C Over Temperature	2.3 2.6		16.5 16.5	V
Supply Current	I_S	No Load, LX Off, Over Temperature $+V_S$ = +5V $+V_S$ = +15V		 80 260	 150 500	µA
Reference Voltage	VREF	T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 2)		No Load, VFB = VREF, $+V_S$ = +5V Over Temperature				V
		MAX635A, MAX636A, MAX637A } 5% Output Accuracy	-4.75 -11.4 -14.25	-5.0 -12.0 -15.0	-5.25 -12.6 -15.75	
		MAX635B, MAX636B, MAX637B } 10% Output Accuracy	-4.5 -10.8 -13.5	-5.0 -12.0 -15.0	-5.5 -13.2 -16.5	
Efficiency				85		%
Line Regulation (Note 2)		+5V<$+V_S$<+15V		0.5		%VOUT
Load Regulation (Note 2)		P_{OUT} = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f_0	+VS = +5V MAX63_A MAX63_B	45 40	50 50	56 65	kHz
Oscillator Duty Cycle		$+V_S$ = +5V	40	50	60	%
LX On Resistance	R_{ON}	I_X = 100mA, $+V_S$ = +5V = +15V		9 4	16 8	Ω
LX Leakage Current	I_{XL}	$+V_S$ = +16.5V T_A = +25°C Over Temperature		0.01	1.0 30	µA
VFB Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V2 = +0.4V, V3 = +1.1V T_A = 25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V2 = +16.5V, V3 = +1.4V		0.01	3.0	µA

Note 1: In addition to the Absolute Maximum Rating of +18V, the input voltage also must not exceed 24V -| -VOUT|.
Note 2: Guaranteed by correlation with DC pulse measurements.

Preset/Adjustable Output CMOS Inverting Switching Regulators

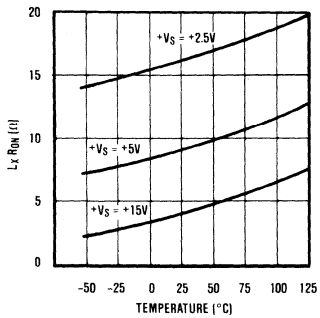
Pin Description

PIN	NAME	FUNCTION
1	-VOUT	The sense INPUT for fixed output operation, -VOUT, is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter (Figure 2), VOUT does not supply current, LX does.
2	LBO	Low Battery Detector Output. An open drain N-channel MOSFET which sinks current when the voltage at LBI is below 1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the low Battery Detector threshold (+1.31V), LBO sinks current.
4	GND	Ground

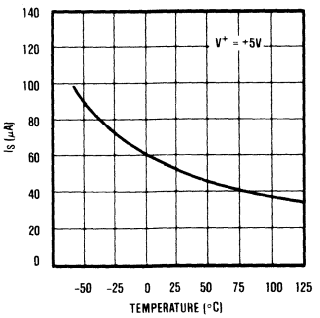
PIN	NAME	FUNCTION
5	LX	This pin drives the external inductor with an internal P-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	+VS	The positive Supply Voltage, from +2V to +16.5V. The total difference between the negative output voltage and the positive input must be less than 24V.
7	VREF	The Voltage Reference output is +1.31V, generated by an on-chip bandgap reference.
8	VFB	When VFB is tied to VREF, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected to VFB and VREF, this pin becomes the feedback input for adjustable output operation.

Typical Operating Characteristics

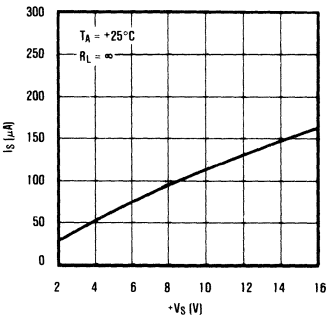
LX ON RESISTANCE vs. TEMPERATURE



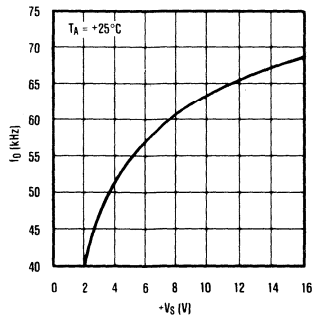
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



4

Preset/Adjustable Output CMOS Inverting Switching Regulators

Detailed Description

Principle of Operation

Figure 1 shows a simplified inverting converter. When the switch is closed, a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. As the energy stored in the inductor is transferred to the output filter capacitor, the current linearly decays to zero, and the magnetic field collapses.

The MAX635/636/637 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has become more positive than the desired value.

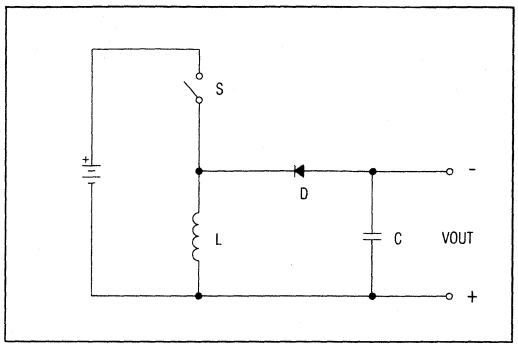


Figure 1. Simplified Inverting Converter

Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive voltage into a negative one. When the output becomes more positive than the preset level, the Error Comparator switches low, and the MOSFET at LX is toggled on and off at the clock frequency. During the low-going period of the oscillator, P1 is on, and current is delivered to the external inductor through the LX pin.

When the oscillator output goes high, the MOSFET turns off, but current continues to flow through the inductor. Diode D1 thus conducts, and the output filter capacitor, C1, is charged negatively.

Basic Step-Down Circuit

Table 1 lists some coil manufacturers and typical part numbers. Table 2 shows nominal inductor parameters for a variety of input and output voltages. The data refers to the circuit of Figure 2. When noise is not critical, a

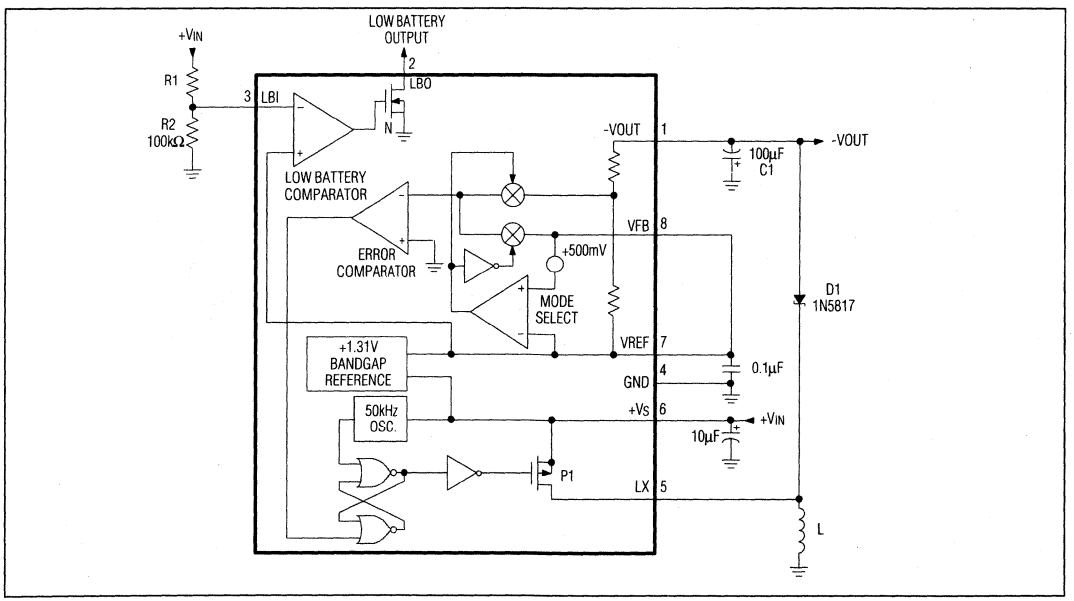


Figure 2. MAX635/636/637 Block Diagram and Typical Circuit (Table 2)

low-cost bobbin inductor will suffice. For higher power circuits, or when low noise and EMI are required, pot cores or toroids should be used. If more output power is desired, see the Medium Power Inverters section.

Table 1. Coil and Core Manufacturers (Note 3)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
ASIA		
TDK Corporation 13-1, Nihonbashi 1-chome Chuo-ku Tokyo 103 Japan		
EUROPE		
Richard Jahre GmbH Luetzowstrasse 90 1000 Berlin 30 Germany		
BOBBIN INDUCTORS		
Dale	IHA-104	500µH, 0.5Ω
Caddell-Burns	7070-29	220µH, 0.55Ω
Gowanda	1B253	250µH, 0.44Ω
TRW	LL-500	500µH, 0.75Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82Ω
TRW	MH-1	600µH, 1.9Ω
Gowanda	050AT1003	100µH, 0.05Ω
FERRITE CORES AND TOROIDS (Note 4)		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T^2
Siemens	B64290-K38-X38	Tor. Core, 4µH/T^2
Magnetics	555.130	Tor. Core, 53nH/T^2
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T^2

Note 3: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 4: Permag Corp. is a distributor for many of the listed core and toroid manufacturers (516) 822-3311.

Table 2. Inductor Selection for Common Designs (Figure 2)

V_{IN} (V)	VOUT (V)	IOUT (mA)	Part No.	INDUCTOR µH	INDUCTOR Ω
+3	-5	5	7070-27	150µH	0.43
+5	-5	25	7070-27	150µH	0.43
+9	-5	40	7070-31	330µH	0.72
+12	-5	45	7070-33	470µH	0.88
+15	-5	50	7070-35	680µH	1.5
+5	-12	12	7070-26	120µH	0.32
+9	-12	30	7070-31	330µH	0.72
+12	-12	40	7070-33	470µH	0.88
+3	-15	2	7070-27	150µH	0.43
+5	-15	8	7070-27	150µH	0.43
+9	-15	25	7070-31	330µH	0.72

Note 5: Caddell-Burns N.Y. (516) 746-2310.

Low Battery Detector

The Low Battery Output, LBO, sinks current whenever the input voltage at Low Battery Input, LBI, is less than +1.31V. LBI is a high impedance CMOS input, with less than 10nA leakage current. LBO is an open drain N-channel MOSFET with about 500Ω of output resistance. The trip voltage of the Low Battery Detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between LBO and LBI.

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1 \right)$$

(V_{LB} is the desired Low Battery detection voltage.)

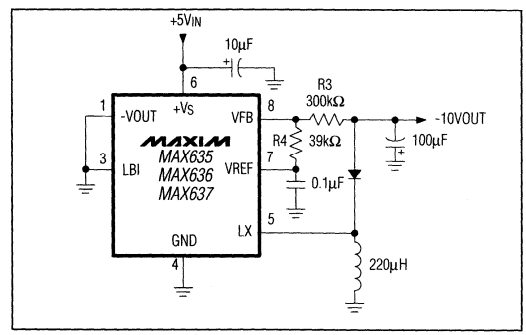


Figure 3. Adjustable Output Operation

Preset/Adjustable Output CMOS Inverting Switching Regulators

Fixed or Adjustable Output

For operation at one of the preset output voltages (-5V for the MAX635, -12V for the MAX636, and -15V for the MAX637), V_{FB} is connected to VREF, and no external resistors are required.

Other output voltages are selected by connecting an external voltage divider to VFB as shown in Figure 3. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$VOUT = -1.31V \times \frac{R3}{R4}$$

External Components

What Value of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is opposite in polarity to the input.

Inductor selection for any DC-DC converter depends on three things: the desired output power, the input voltage (or input voltage range), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input voltage, determines how much energy will be stored in the coil.

The maximum amount of energy (E_L) in the coil each cycle is a function of the peak current (I_{pk}) and the inductance of the coil (L):

The inductor must meet four electrical criteria:

[ ] **Value –** low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

[ ] **Saturation –** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[ ] **EMI –** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for digital circuits; toroid or pot core types work well for EMI-sensitive analog circuits.

[ ] **DC resistance –** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX635/636/637 operating frequency.

Inductor Value – Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

[ ] Maximum load current
[ ] Minimum supply voltage
[ ] Maximum inductor value, including tolerance
[ ] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
[ ] Worst-case low on time

Inductor Value – High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values can result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

[ ] Maximum supply voltage
[ ] Minimum inductor value, including tolerance
[ ] Minimum on resistance of the switch
[ ] Low switching frequency (or maximum switch on time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1] \quad I_{pk} = \frac{VOUT + V_{DIODE}}{(0.25)\,(V_{IN} - V_{SW})}\,(IOUT)$$

$$[2] \quad L = \frac{V_{IN} - V_{SW}}{I_{pk}}\,(t_{ON})$$

where VSW is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V

max, 0.25V min with VIN = +15V and 1.5V max, 0.5V min with VIN = +5V.

Example: A +5V 10% input must be converted to -12V at 12mA.
A Schottky diode (1N5817) and a MAX636A are used.

Calculate the maximum inductor value allowed:

$$I_{pk} = \frac{12V - 0.4V}{(0.25)(4.5V - 1.5V)} (12mA) = 198mA$$

$$L = \frac{4.5V - 1.5V}{198mA} (9\mu s) = 136\mu H$$

Calculate the minimum inductor value allowed:

I_{pk} = 525mA (from table of max ratings; use the power MOSFET max ratings for external transistor circuits.)

$$L = \frac{5.5V - 0.5V}{525mA} (11\mu s) = 105\mu H$$

A value of 120µH would be a good choice for this application.

I_{pk} must also be compared to the current rating of the LX switch. If I_{pk} exceeds the peak current rating of the switch (525mA), an external MOSFET or transistor with an adequate current rating must be used (see Medium Power Inverters).

The coil resistance has a significant effect on the output current; a coil with a low resistance will increase the output current and overall efficiency. The inductor should have a powdered iron or ferrite core and should have a resistance less than 0.5Ω.

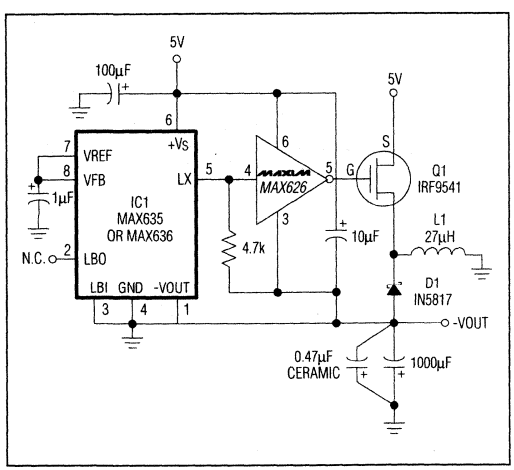


Figure 4. Medium Power Inverter

Medium Power Inverters

In the circuit of Figure 4, the MAX626 MOSFET driver is used to convert the open drain LX output to a signal suitable for driving the gate of an external P-Channel MOSFET. The IRF9541 has a gate threshold voltage of 2V to 4V so it will have a relatively high resistance if driven with only 5V of gate drive. To increase the gate drive voltage, and thereby increase efficiency, the negative supply pin of the CMOS inverter is connected to the negative output rather than to the ground. Once the circuit is started, the gate drive swings from +5V to -VOUT.

At start-up, the voltage at -VOUT is one Schottky diode drop above ground, and the gate drive to the power MOSFET is slightly less than 5V. The output should be only lightly loaded to ensure start-up, since the output power capability of the circuit is very low until -VOUT is a couple of volts negative. (See Table 3 for component values for L2 and IC1.)

Table 3. Component Selector for Medium Power Inverters (Figure 4)

V_{IN}	-VOUT	IOUT	EFFICIENCY	IC1	L1
5V	-5V	400mA	70%	MAX635	27µH
5V	-5V	500mA	64%	MAX635	18µH
5V	-12V	150mA	75%	MAX636	27µH
5V	-12V	200mA	70%	MAX636	18µH

Notes: 18µH Coil = Caddell-Burn's (Mineola, NY) Model 6860-04.
27µH Coil = Caddell-Burn's Model 6860-06.

External Diode

In most DC-DC converter circuits, the current in the "catch" diode (Figure 2, D1) abruptly goes from zero to its peak value each time the MOSFET at LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Output Filter Capacitor

The MAX635/636/637's output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent

Preset/Adjustable Output CMOS Inverting Switching Regulators

Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100µF to 500µF range, in parallel with a 0.1µF ceramic capacitor.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns on NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boosting transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Bypassing and Compensation

The high current pulses in the LX output and the external inductor can cause erratic operation unless the MAX635/636/637 is properly bypassed. Connect a 10mF bypass capacitor directly across the device between +VS and GND to minimize the inductance and high frequency impedance of the power source. Also make sure that the high current ground return path of the inductor does not cause a voltage drop in the regulator's ground line.

The reference voltage output, VREF, should be bypassed to ground with a 0.1µF capacitor. Avoid coupling to the high current path that includes the LX output and the inductor ground return.

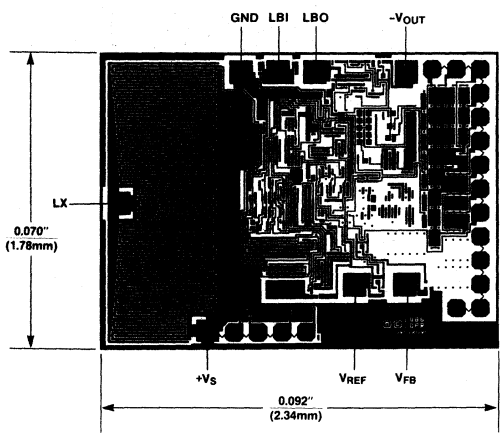
When the value of the voltage setting resistors (R3 and R4, Figure 3) exceed 50kΩ, stray capacitance at the VFB input can add a "lag" to the feedback response causing output pulses to occur in bursts. This increases low-frequency ripple and lowers efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed output pulses can be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

Ordering Information (continued)

PART*	TEMP. RANGE	PIN - PACKAGE
MAX637XCPA	0°C to +70°C	8 Plastic DIP
MAX637XCSA	0°C to +70°C	8 Narrow SO
MAX637XCJA	0°C to +70°C	8 CERDIP
MAX637XC/D	0°C to +70°C	Dice
MAX637XEPA	-40°C to +85°C	8 Plastic DIP
MAX637XESA	-40°C to +85°C	8 Narrow SO
MAX637XEJA	-40°C to +85°C	8 CERDIP
MAX637XMJA	-55°C to +125°C	8 CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.*

Chip Topography



MAXIM

+5V/Adjustable CMOS Step-Down Switching Regulator

General Description

The MAX638 step-down switching regulator is designed for minimum component, low power, DC-DC conversion.

Typical applications require only a small, low-cost inductor, an output filter capacitor, and a catch diode. Low battery detection circuitry is included on chip.

Though most simply used as a fixed +5V output regulator, the MAX638 can be set for other voltages by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Features

- ♦ **Fixed +5V Output**
- ♦ **Adjustable Output with 2 Resistors**
- ♦ **Low Operating Current**
- ♦ **85% Typ Efficiency**
- ♦ **8-Pin Plastic DIP and Narrow SO Packages**
- ♦ **3 External Components**
- ♦ **Low Battery Detector**

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX638XCPA	0°C to +70°C	8 Plastic DIP
MAX638XCSA	0°C to +70°C	8 Narrow SO
MAX638XC/D	0°C to +70°C	Dice
MAX638XEPA	-40°C to +85°C	8 Plastic DIP
MAX638XESA	-40°C to +85°C	8 Narrow SO
MAX638XEJA	-40°C to +85°C	8 CERDIP
MAX638XMJA	-55°C to +125°C	8 CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.*

Applications

Efficient DC-DC Step-Down Regulation

Linear Voltage Regulator Replacement

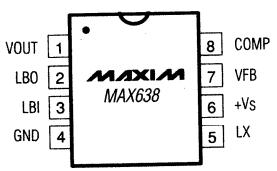
+12V to +5V Conversion

Battery Life Extension

Portable Instruments

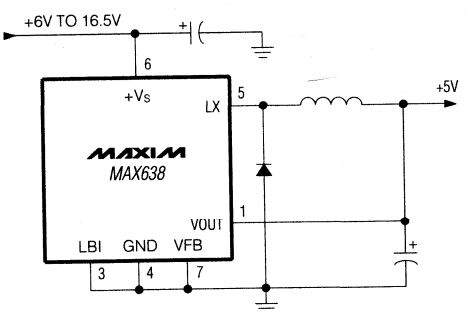
Pin Configuration

Top View



DIP/SO

Typical Operating Circuit



+5V OUTPUT STEP-DOWN REGULATOR

+5V/Adjustable CMOS Step-Down Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ ..... +18V
Output Voltage, L_X ..... +18V
Output Voltage, LBO ..... $+V_S$
Input Voltage, LBO, LBI, VFB, COMP ..... -0.3V to ($+V_S$ + 0.3V)
L_X Output Current ..... 525mA Peak
LBO Output Current 50mA
Operating Temperature
MAX638C ..... 0°C to +70°C
MAX638E ..... -40°C to +85°C
MAX638M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$+V_S$	Over Temperature V_{OUT} = +5V Adjustable mode	 5 2.2		 16.5 16.5	V
Supply Current	I_S	T_A = +25°C Over Temperature		135 180	 600	µA
Reference Voltage (Internal)		T_A = +25°C Over Temperature	1.28 1.24	1.31	1.34 1.38	V
V_{OUT} Voltage (Note 1)		No Load, V_{FB} = GND, 638A Over Temperature 638B	4.75 4.5	5.0 5.0	5.25 5.5	V
Efficiency				85		%
Line Regulation (Note 1)		+10V < $+V_S$ < +15V		0.2		% V_{OUT}
Load Regulation (Note 1)		P_{OUT} = 0mW to 150mW		0.2		% V_{OUT}
Oscillator Frequency	f_O			65		kHz
Oscillator Duty Cycle				50		%
L_X ON Resistance	R_{ON}	I_X = 100mA		6	12	Ω
L_X Leakage Current	I_{XL}	V_5 = OV T_A = +25°C Over Temperature		0.01	1.0 30	µA
V_{FB} Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Input Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V_2 = +0.4V, V_3 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V_2 = $+V_S$, V_3 = +1.4V		0.01	3.0	µA

Note 1: Guaranteed by correlation with DC pulse measurements.

+5V/Adjustable CMOS Step-Down Switching Regulator

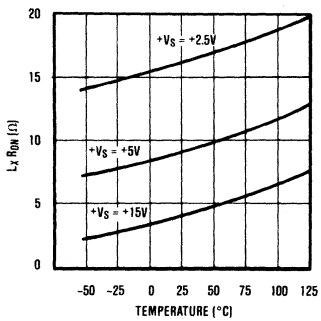
Pin Description

PIN	NAME	FUNCTION
1	VOUT	The sense INPUT for fixed +5V output operation, VOUT, is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter (Figure 2), the VOUT pin does not supply current, LX does.
2	LBO	Low Battery Detector Output. An open drain N-channel MOSFET which sinks current when the voltage at LBI is below +1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO sinks current.
4	GND	Ground

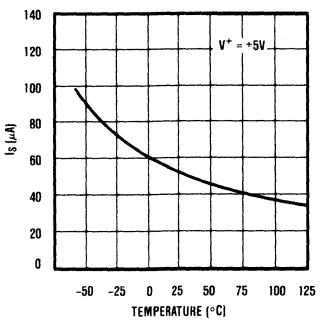
PIN	NAME	FUNCTION
5	LX	This pin drives the external inductor with an internal P-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	+VS	The input voltage, from VOUT to +16.5V.
7	VFB	When VFB is grounded, the DC-DC converter output will be +5V. When an external voltage divider is connected from VOUT to VFB, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. It is normally left unconnected.In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response.

Typical Operating Characteristics

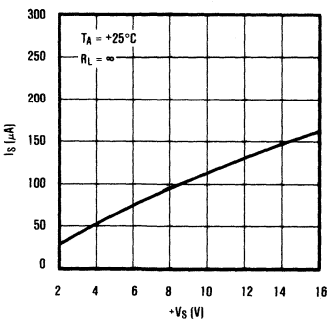
LX ON RESISTANCE vs. TEMPERATURE



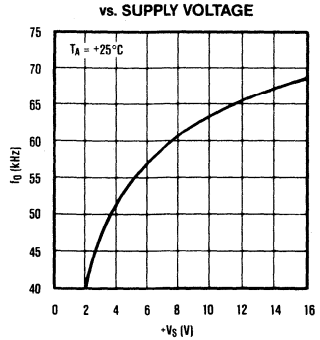
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



4

+5V/Adjustable CMOS Step-Down Switching Regulator

Detailed Description

Basic Operation

Figure 1 shows a simplified step-down DC-DC converter. When the switch closes, a charging current flows through the inductor creating a magnetic field. (This current flows into the filter capacitor and load as well.) When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. But since the switch is now open, the current must flow through the diode. With the switch open, the inductor alone supplies current to the load. This current linearly decays to zero as the magnetic field collapses and the energy in the core of the inductor is transferred to the filter capacitor and load.

Figure 2 shows a block diagram of the MAX638 and a typical connection in which a +9V input is converted to a +5V output with 85% efficiency. When the output drops below +5V, the Error Comparator switches high and connects the internal 65kHz oscillator to the gate of the LX output driver. LX turns on and off at the clock frequency, charging and discharging the inductor and supplying current to the output as described above. When the output voltage reaches +5V, the comparator output goes low and the inductor is no longer pulsed.

Basic Step-Down Circuits

Table 1 shows nominal inductor parameters for a variety of input voltages. The data refers to the circuit of Figure 3.

Output Driver (LX Pin)

A large P-channel MOSFET with an on resistance of approximately 6Ω is used to charge the inductor. It is internally connected between $+V_S$ and LX and has a peak current rating of 525mA. The available output current for most applications will be less than the peak current rating. A good rule of thumb for MAX638 maximum output current is:

4 IOUT < 525mA, assuming $V_{IN} \simeq 2$ VOUT

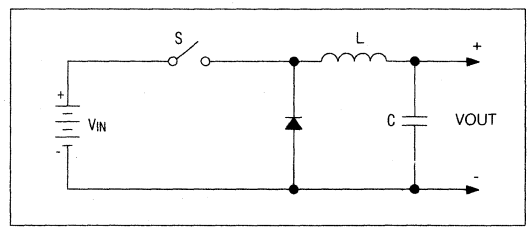


Figure 1. Simplified Step-Down Converter

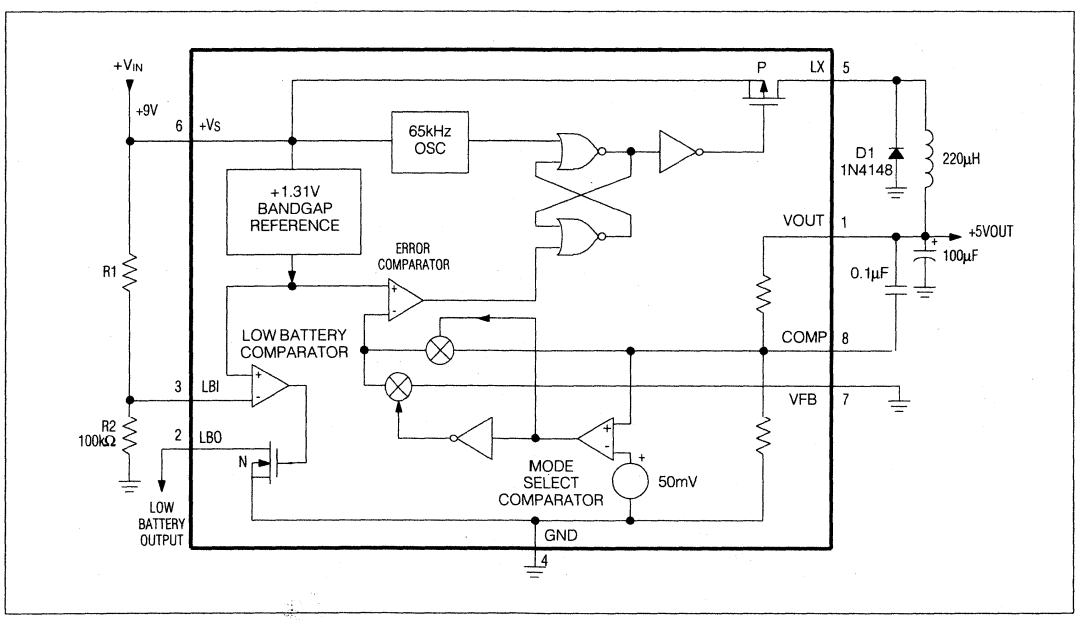


Figure 2. MAX638 Block Diagram and Typical Circuit

Table 1. Inductor Selection For Common Designs (See Figure 3)

MAXIM PART NO.	V_{IN} (V)	VOUT (V)	IOUT (mA)	TYP EFF (%)	I_{pk} (mA)	PART NO.*	INDUCTOR (L) µH	Ω
MAX638	7-9.5	5	35	92	200	7070-27	150	0.4
	8-9.5	5	55	89	200	7070-27	150	0.4
	10-14	5	50	92	300	7070-30	270	0.6
	12	5	60	92	250	7070-30	270	0.6
	12	5	75	89	300	7070-28	180	0.5

* Caddell-Burns, NY, (516) 746-2310

Fixed or Adjustable Output

For operation at the preset +5V output voltage, VFB is connected to GND, and no external resistors are required. For other output voltages, an external voltage divider is connected to VFB as shown in Figure 4. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4\left(\frac{VOUT}{1.31V} - 1\right)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI) with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO) goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery detection voltage is set by resistors, R1 and R2 (Figure 2).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R1 = R2\left(\frac{V_{LB}}{1.31V} - 1\right)$$

(V_{LB} is the desired Low Battery detection voltage)

What Value of Inductor?

A General Discussion

The converter in this data sheet operates by charging an inductor from a DC input, and then discharging the inductor to generate a DC output less than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or input voltage range), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This and the input voltage determines how much energy will be stored in the coil.

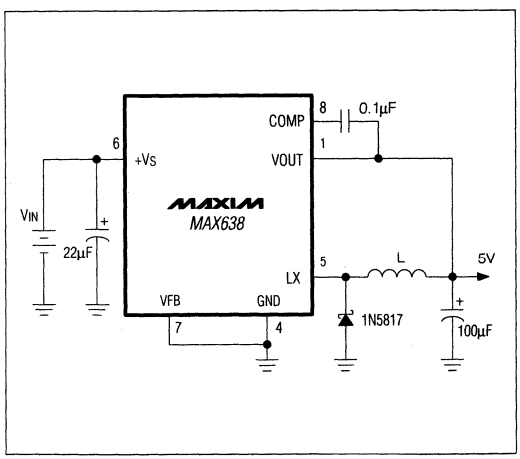


Figure 3. Typical Operating Circuit (Table 1)

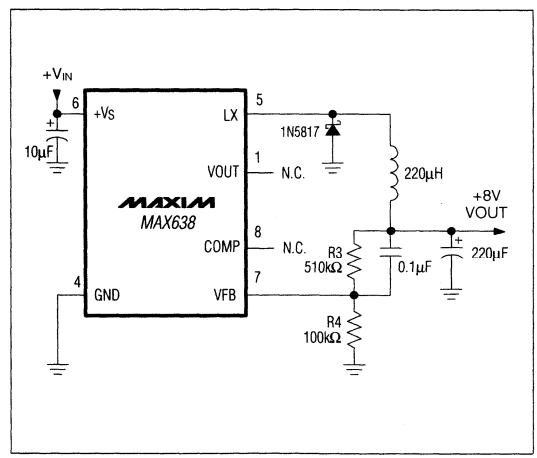


Figure 4. Adjustable Output Operation

+5V/Adjustable CMOS Step-Down Switching Regulator

The inductor must meet four electrical criteria:

[ ] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

[ ] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[ ] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

[ ] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 2Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX638 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

[ ] Maximum load current
[ ] Minimum supply voltage
[ ] Maximum inductor value, including tolerance
[ ] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
[ ] Worst-case low on time

Inductor Value- High Enough?

The inductor value must be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values can result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

[ ] Maximum supply voltage
[ ] Minimum inductor value, including tolerance
[ ] Minimum on resistance of the switch
[ ] Low switching frequency (or maximum switch on-time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for low ripple.

$$[1] \quad I_{pk} = \frac{4\,IOUT}{\frac{V_{IN} - V_{SW} - VOUT}{VOUT - V_{DIODE}} + 1}$$

$$[2] \quad L = \frac{V_{IN} - V_{SW} - VOUT}{I_{pk}} (t_{ON})$$

where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with V_{IN} = +15V and 1.5V max, 0.5V min with V_{IN} = +5V.

Example: A +12V 10% input must be converted to +5V at 50mA. A Schottky diode (1N5817) and a MAX638B are used.

Calculate the maximum inductor value allowed:

$$I_{pk} = \frac{(4)\,(50mA)}{\frac{10.8V - 0.75V - 5V}{5V - 0.4V} + 1} = 95mA$$

$$L = \frac{10.8V - 0.75V - 5V}{95mA} (6\mu s) = 319\mu H$$

Calculate the minimum inductor value allowed:

$$I_{pk} = 525mA \text{ (from table of max ratings)}$$

$$L = \frac{13.2V - 0.25V - 5V}{525mA} (9.2\mu s) = 139\mu H$$

The standard value of 270µH would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

Output Filter Capacitor

The MAX638's output ripple has 2 components which are 90° out-of-phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost

are typically achieved with a high-quality aluminum electrolytic, in the 100µF to 500µF range, in parallel with a 0.1µF ceramic capacitor.

Table 2. Coil and Core Manufacturers (Note 2)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
ASIA		
TDK Corporation 13-1, Nihonbashi 1-chome Chuo-ku Tokyo 103 Japan		
EUROPE		
Richard Jahre GmbH Luetzowstrasse 90 1000 Berlin 30 Germany		
BOBBIN INDUCTORS		
Dale	IHA-104	500µH, 0.5Ω
Caddell-Burns	7070-29	220µH, 0.55Ω
Gowanda	1B253	250µH, 0.44Ω
UTC	LL-500	500µH, 0.75Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82Ω
UTC	MH-1	600µH, 1.9Ω
Gowanda	050AT1003	100µH, 0.05Ω
FERRITE CORES AND TOROIDS (Note 3)		
Siemens	B64290-K38-X38	Tor. Core, 4µH/T^2
Magnetics	555.130	Tor. Core, 53nH/T^2
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T^2

Note 2: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufactures of these components.

Note 3: Permag Corp. is a distributor for many of the listed core and toroid manufacturers (516) 822-3311.

External Diode

In most MAX638 circuits, the current in the external diode (D1, Figure 2) abruptly goes from zero to its peak value each time LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low-power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher power circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boost transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

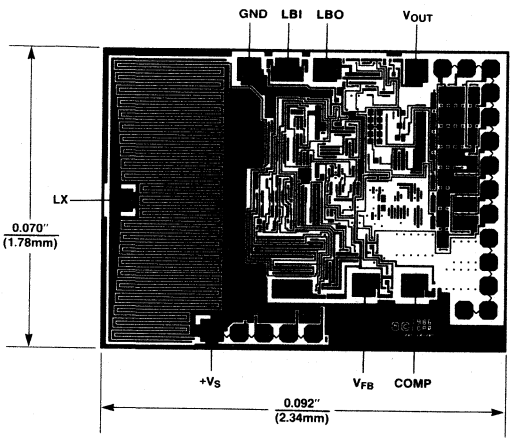
Bypassing and Compensation

Since the inductor charge and discharge currents can be relatively large, high currents may flow in ground connections near the MAX638. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power-supply bypassing should be used. A 10µF aluminum electrolytic placed at the device pins is recommended.

When the value of the voltage setting resistors (R3 and R4, Figure 4) exceed 50kΩ, stray capacitance at the VFB input can add a "lag" to the feedback response, increasing low-frequency ripple and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 0.1µF) in parallel with R3.

+5V/Adjustable CMOS Step-Down Switching Regulator

Chip Topography



MAXIM

Fixed Output 10W CMOS Step-Up Switching Regulators

General Description

The MAX641/MAX642/MAX643 step-up switching regulators are designed for minimum component DC-DC converter circuits in the 5mW to 10W range.

Low-power applications require only an output filter capacitor and a small, low-cost inductor. An additional MOSFET or bipolar transistor is needed for high-power applications. Low battery detection circuitry is included on chip.

The MAX641/642/643 are preset for +5V, +12V, and +15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors. Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive. See Table 3 for a summary of other DC-DC converter products.

Applications

Simple, High-Efficiency DC-DC Converters

Uninterruptible Board-Level Power Supplies

Power Conditioning for Battery Systems

Portable Instruments and Communications

Features

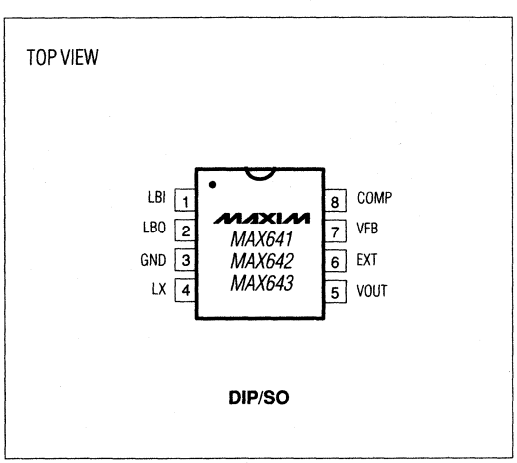
- ♦ **Fixed +5V, +12V, +15V Output Voltages**
- ♦ **Adjustable Output with 2 Resistors**
- ♦ **On-Chip Driver for High-Power External MOSFET**
- ♦ **135µA Typ Operating Current**
- ♦ **80% Typ Efficiency**
- ♦ **8-Pin Narrow DIP and Narrow SO Packages**

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX641XCPA	0°C to +70°C	8 Plastic DIP
MAX641XCSA	0°C to +70°C	8 Narrow SO
MAX641XC/D	0°C to +70°C	Dice
MAX641XEPA	-40°C to +85°C	8 Plastic DIP
MAX641XESA	-40°C to +85°C	8 Narrow SO
MAX641XEJA	-40°C to +85°C	8 CERDIP
MAX641XMJA	-55°C to +125°C	8 CERDIP
MAX642XCPA	0° to +70°C	8 Plastic DIP
MAX642XCSA	0° to +70°C	8 Narrow SO
MAX642XC/D	0° to +70°C	Dice
MAX642XEPA	-40°C to +85°C	8 Plastic DIP
MAX642XESA	-40°C to +85°C	8 Narrow SO
MAX642XEJA	-40°C to +85°C	8 CERDIP
MAX642XMJA	-55°C to +125°C	8 CERDIP

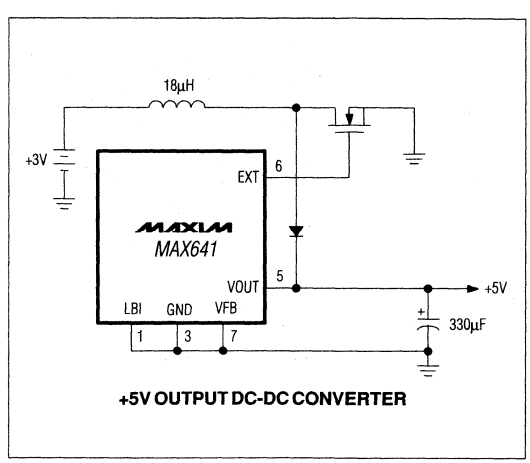
X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.
Ordering information continued on last page.

Pin Configuration



DIP/SO

Typical Operating Circuit



+5V OUTPUT DC-DC CONVERTER

Fixed Output 10W CMOS Step-up Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VOUT ..... +18V
Output Voltage, LX and LBO ..... +18V
Input Voltage, LBI, LBO, VFB, COMP. . -0.3V to (+VOUT + 0.3V)
LX Output Current ..... 450mA Peak
LBO Output Current 50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
  Small Outline (derate 6mW/°C above +50°C) 450mW
  CERDIP (derate 8mW/°C above +50°C) 800mW

Operating Temperature
  MAX64_ _C ..... 0°C to +70°C
  MAX64_ _E ..... -40°C to 85°C
  MAX64_ _M ..... -55°C to 125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	+Vs	Voltage at VOUT Over Temperature	2.0		16.5	V
Start-up Voltage	+Vs	Voltage at VOUT T_A = +25°C Over Temperature	 1.5 1.8	 1.3		V
Supply Current	Is	LX Off, Over Temperature VOUT = +5V VOUT = +12V VOUT = +15V		 0.135 0.5 0.75	 0.4 2.0 2.5	mA
Reference Voltage (Internal)	VREF	T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 1)		No Load, VFB = GND, Over Temperature MAX641A, MAX642A, MAX643A } 5% Output Accuracy MAX641B, MAX642B, MAX643B } 10% Output Accuracy	 4.75 11.4 14.25 4.5 10.8 13.5	 5.0 12.0 15.0 5.0 12.0 15.0	 5.25 12.6 15.75 5.5 13.2 16.5	V
Efficiency		With External MOSFET		80		%
Line Regulation (Note 1)		0.5VOUT < +Vs < VOUT		0.08		% VOUT
Load Regulation (Note 1)		+Vs = 0.5VOUT, P_{OUT} = 0mW to 150mW		0.2		% VOUT

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	f_0	VOUT = +5V MAX641A MAX641B VOUT = +12V MAX642A MAX642B VOUT = +15V MAX643A MAX643B	 40 37.5 45.5 42 45.5 42	 45 45 50 50 50 50	 50 56.5 56 62.5 56 62.5	kHz
Oscillator Frequency Tempco				-60		Hz/°C
Oscillator Duty Cycle		MAX641, VOUT = +5V MAX642, VOUT = +12V MAX643, VOUT = +15V	40 40 40	50 50 50	60 60 60	%
EXT Output Resistance		VOUT = +5V, IOUT = ±10mA VOUT = +15V, IOUT = ±30mA		140 90		Ω
EXT Switching Time	t_{ON}, t_{OFF}	C_L = 330pF VOUT = +5V VOUT = +15V		 160 125		ns
LX On Resistance	R_{ON}	I_X = 100mA, VOUT = +5V VOUT = +15V		6 3.5	12 7	Ω
LX Leakage Current	I_{XL}	V4 = +16.5V T_A = +25°C Over Temperature (C,E) Over Temperature (M)		0.01	1.0 30 100	µA
Diode Forward Voltage	V_F	I_F = 100mA			1.0	V
VFB Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V2 = +0.4V, V1 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V2 = +16.5V, V1 = +1.4V		0.01	3.0	µA

Note 1: Guaranteed by correlation with DC pulse measurements.

Fixed Output 10W CMOS Step-up Switching Regulators

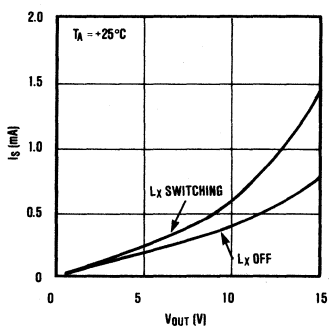
Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI is below +1.31V.
3	GND	Ground
4	LX	In low-power applications, LX drives the external inductor with an internal N-channel power MOSFET. LX has a typical output resistance of 6Ω and a peak current rating of 450mA.
5	VOUT	The regulated DC-DC converter output when the internal MOSFET and catch diode are used. When an external diode is used, this pin becomes the supply voltage input pin and is usually connected to the cathode of the external diode.

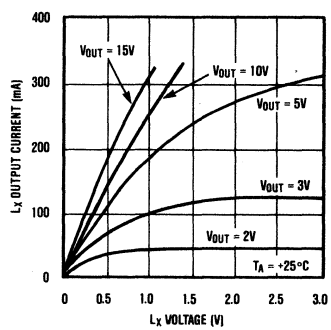
PIN	NAME	FUNCTION
6	EXT	The drive output for an external power MOSFET or bipolar transistor EXT swings from GND to VOUT and has approximately 100Ω sink/source impedance. EXT is low when LX is open circuit and high when LX is on.
7	VFB	When VFB is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected to VFB, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response. Ground comp when using an External Voltage divider on VFB.

Typical Operating Characteristics

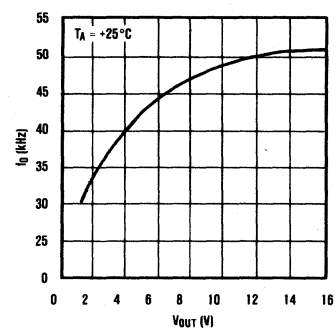
SUPPLY CURRENT vs. OUTPUT VOLTAGE



L_X OUTPUT CURRENT vs. V_{OUT}



OSCILLATOR FREQUENCY vs. OUTPUT VOLTAGE



Fixed Output 10W CMOS Step-Up Switching Regulators

Detailed Description

Basic Operation

The operation of the MAX641 series can best be understood by examining the regulating loop of Figure 1. When the output voltage drops below the preset (or externally set) value, the Error Comparator switches high and connects the internal 45kHz Oscillator to the gate of the internal MOSFET and to the EXT output. EXT is typically connected to the gate of an external N-channel power MOSFET. When EXT is activated, the MOSFET turns on and off at the internal clock frequency.

When EXT is high, the MOSFET switches on, and the inductor current increases linearly storing energy in the coil. When EXT switches the MOSFET off, the coil's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at the anode of the catch diode then rises until the diode is forward biased, delivering power to the output. As the output voltage reaches the desired level, the Error Comparator inhibits EXT until the load discharges the output filter capacitor to less than the desired output level.

Though designed to power an external MOSFET or bipolar transistor, the MAX641 series will also work well in low-power applications (<250mW) with its own internal MOSFET and catch diode. In these applications, the LX output does the current switching and an external capacitor and inductor are all that are needed.

V_{IN}, Bootstrapped Operation

The MAX641/642/643 do not have a V_{IN} pin. Input power to start the DC-DC converter is supplied via the external inductor (and diode, if used) to the VOUT pin. Once the converter has started, it is then powered from its own output. This design ensures that the output MOSFET will have maximum gate drive and, hence, a minimum R_{ON}. It also allows the converter to start at lower input voltages.

V_{IN} Greater Than VOUT

If the regulator's input voltage is more than 1 forward diode drop greater than the desired output voltage, the EXT and LX outputs will not turn on, and the output will no longer be regulated. However, current will be supplied to the load directly through the catch diode. As long as the input is more than 0.6V above the desired output,

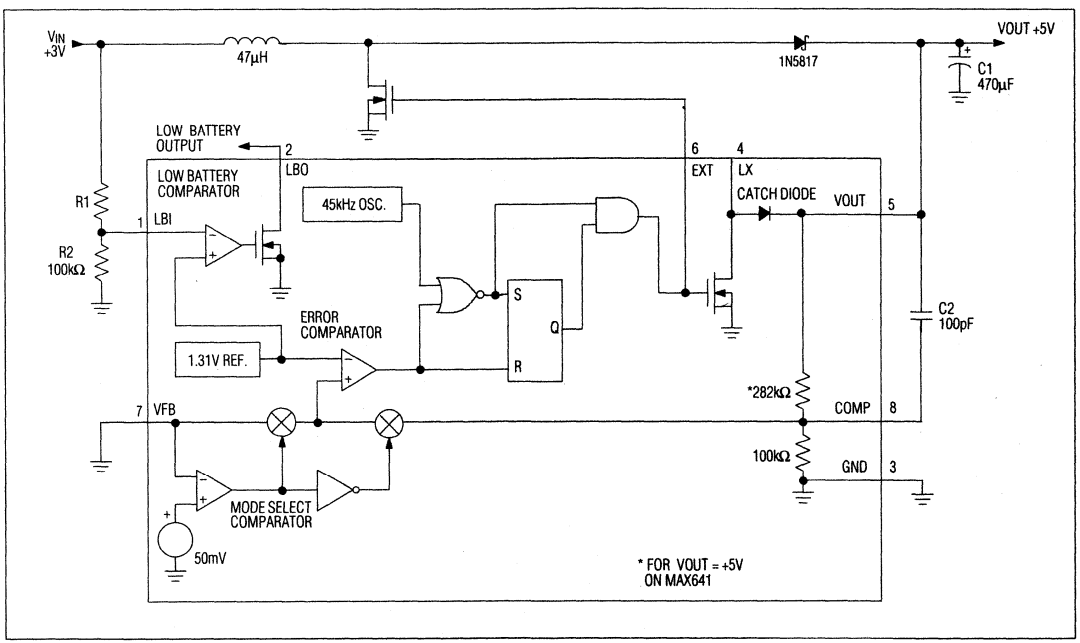


Figure 1. +3V to +5V Converter and Block Diagram for MAX641/642/643

Fixed Output 10W CMOS Step-up Switching Regulators

the output will equal the input voltage, less the forward drop of the catch diode.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX641, +12V for MAX642, and +15V for MAX643), VFB is connected to GND, and no external resistors are required.

For other output voltages, a voltage divider is connected to VFB as shown in Figure 2. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4\left(\frac{VOUT}{1.31} - 1\right)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI), with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO) goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery threshold is set by resistors R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R1 = R2\left(\frac{VLB}{1.31V} - 1\right)$$ (VLB is the desired Low Battery detection voltage)

What Value Of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input, then discharging the inductor to generate a DC output greater than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or range of input voltage), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input voltage, determines how much energy will be stored in the coil.

The inductor must meet four electrical criteria:

[ ] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

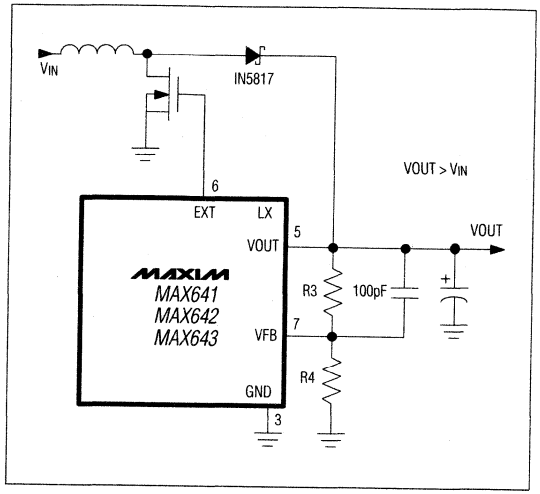


Figure 2. Connections for Adjustable Output Operation

[ ] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[ ] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

[ ] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX641/642/643 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

[ ] Maximum load current
[ ] Minimum supply voltage
[ ] Maximum inductor value, including tolerance
[ ] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
[ ] Worst-case low on time

Fixed Output 10W CMOS Step-Up Switching Regulators

Inductor Value- High Enough?

The inductor value must be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values may result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

[ ] Maximum supply voltage
[ ] Minimum inductor value, including tolerance
[ ] Minimum on resistance of the switch
[ ] Low switching frequency (or maximum switch on time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1]\quad I_{pk} = \frac{VOUT + V_{DIODE} - V_{IN}}{(0.25)\,(V_{IN} - V_{SW})}\ (IOUT)$$

$$[2]\quad L = \frac{V_{IN} - V_{SW}}{I_{pk}}\ (t_{ON})$$

Where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with V_{IN} = +15V and 1.5V max, 0.5V min with V_{IN} = +5V.

Example: A +5V 10% input must be converted to +15V at 15mA. A Schottky diode (1N5817) and a MAX643B are used.

Calculate maximum inductor value allowed:

$$I_{pk} = \frac{15V + 0.4V - 4.5V}{(0.25)\,(4.5V - 0.75V)}\,(15mA) = 174mA$$

$$L = \frac{4.5 - 0.75}{174mA}\,(8\mu s) = 172\mu H$$

Calculate the minimum inductor value allowed:

I_{pk} = 450mA (from table of max ratings; use the power MOSFET max ratings for external transistor circuits)

$$L = \frac{5.5V - 0.25V}{450mA}\,(12\mu s) = 140\mu H$$

A value of 160µH would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

Application Hints

External MOSFET

An external MOSFET or transistor can be used to drive the inductor in high-power applications. The current handling specifications of the device must match the peak current which flows in the inductor (see Inductor Selection). The only restriction on the size of the external driver is that the EXT output must be able to drive the external device's gate (or base) capacitance at the internal clock rate (45kHz). An external driver may be used to increase operating voltage range of the MAX641/642/643.

Table 2 contains a list of MOSFETs and their manufacturers. Logic level MOSFETs should be used when the supply voltage is less than +5V. Refer to Figures 4 and 5 for circuits requiring external MOSFETs.

Output Filter Capacitor

The MAX641/642/643 output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost are typically achieved with a high-quality aluminum electrolytic, in the 100µF to 500µF range, in parallel with a 0.1µF ceramic capacitor.

Diodes

When the MAX641/642/643 are used with an external power MOSFET, the internal diode can be used if the peak diode current rating (450mA) and maximum package power dissipation ratings are observed. For higher power circuits, an external Schottky diode such as the 1N5817 (1 Amp) or 1N5821 (3 Amp) should be connected between LX and VOUT in parallel with the internal diode. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are not recommended because their slow turn-on time results in excessive losses and poor efficiency.

Fixed Output 10W CMOS Step-up Switching Regulators

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection near the MAX641/642/643. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and a bypass capacitor (10µF) should be at the VOUT pin, even if large filter capacitor are used elsewhere in the circuit.

When large values (>50kΩ) are used for the voltage setting resistors (R3 and R4 of Figure 2), stray capacitance at the VFB input can add a "lag" to the feedback response, destabilizing the regulator and causing output pulses to occur in bursts. This problem can often be avoided by minimizing pin lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed pulses can also be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between VOUT and COMP adds a "lead" to the regulator's response.

Table 1. Representative N-Channel Power MOSFETs

PART NUMBER	PKG.	Ron AT (I_{DS}, V_{GS} = X)	V(MAX)	MFG.
IRFD121	4p DIP	0.3Ω (1.3A, 10V)	60	H/IR
BUZ71A	TO-220	0.12Ω (6A, 10V)	50	MOT/SI/SM
BUZ21	TO-220	0.1Ω (9A, 10V)	100	MOT/SI/SM
IRF513	TO-220	0.8Ω (2A, 10V)	100	H/IR/MOT/SI
IRF530	TO-220	0.18Ω (8A, 10V)	100	H/IR/MOT/SI
IRF540	TO-220	0.085Ω (8A, 10V)	100	H/IR/MOT/SI
IRF620	TO-220	0.8Ω (2.5A, 10V)	200	H/IR/MOT/SI
IRF640	TO-220	0.18Ω (10A, 10V)	200	H/IR/MOT/SI

Manufacturer Code: H= Harris, IR= International Rectifier, MOT= Motorola, SM= Siemens, SI= Siliconix

N-Channel Logic-Level Power MOSFETs

PART NUMBER	PKG.	Ron AT (I_{DS}, V_{GS} = X)	V(MAX)	MFG.
RFP25N06L	TO-220	0.85Ω (12.5A, 5V)	50	H
RFP12N10L	TO-220	0.20Ω (6A, 5V)	100	H
PFP15N06L	TO-220	0.14Ω (7.5A, 5V)	50	H
IRL540	TO-220AB	0.11Ω (24A, 4V)	100	IR
IRL734	TO-220AB	0.3Ω (7.8A, 4V)	60	IR
IRZ14	TO-220AB	0.07Ω (23A, 4V)	60	IR
MTM25N05L	TO-220AB	0.1Ω (12.5A, 5V)	50	MOT
MTM15N05L	TO-220AB	0.15Ω (7.5A, 5V)	50	MOT
MTP12N10L	TO-220AB	0.18Ω (6A, 5V)	100	MOT

Manufacturer Code: H= Harris, IR= International Rectifier, MOT= Motorola

Note: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Table 2. Inductance Values for Commonly Encountered Power Supplies (Figure 5)

MAXIM PART NO.	V_{IN} (V)	VOUT (V)	I_{OUT} (mA)	TYP EFF (%)	I_{pk} (A)	PART NO.*	INDUCTOR (L) µH	Ω
MAX641	3	5	200	83	1.3	6860-13	100	.10
	3	5	300	80	2.0	6860-09	47	.05
MAX642	5	12	200	91	1.2	6860-08	39	0.05
	5	12	350	89	2	6860-04	18	0.03
	5	12	550	87	3.5	7200-02	12	0.01
MAX643	5	15	100	92	1.2	6860-08	39	0.05
	5	15	150	89	1.5	6860-06	27	0.04
	5	15	225	89	2	6860-04	18	0.03
	5	15	325	85	3.5	7200-02	12	0.01

* Ferrite Bobbin Coils from Caddell-Burns, NY (516) 746-2310

Inductor Saturation

It is important to be sure that the inductor does not saturate, particularly in high-power circuits. Inductor saturation leads to very high current levels through the external boost transistor, causing excessive power dissipation, poor efficiency, and possible damage to the inductor and the external transistor.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

To ensure that the current rating(s) of the FET(s) is not exceeded, the inductance value of the coil, including the manufacturer's tolerances, should never be lower than that used in the calculations or in Table 2. In addition, to ensure that the core does not saturate, the current rating of the coil should be greater than the peak current, I_{pk}.

Coil resistance has a significant effect on the output current. To increase the output current and raise the overall efficiency, the inductor should have a resistance less than a few tenths of an Ohm.

Inductance Values

Inductance values for commonly encountered power supplies are listed in Table 2. The data in Table 2 refers to the circuit in Figure 5.

Typical Applications

Basic High-Power Hookup

Figure 5 shows the standard circuit configuration for a fixed output step-up DC-DC converter. The output power is determined by the current ratings of the external MOSFET and inductor, as well as, the switching time of the EXT output into the gate capacitance of the MOSFET. Typical switching times are given in the Electrical Characteristics Table.

Low-Power Step-Up Conversion

In low-power applications, the LX output and internal diode may be used instead of an external MOSFET and diode, as shown in Figure 3. The power handling capability of this circuit is about 250mW. See the MAX631 data sheet for inductor selection information.

High-Voltage Operation

If the external MOSFET or transistor has an adequate voltage rating, the output voltage range of the MAX641/642/643 can be extended (Figure 4). The adjustable output mode must be used (VFB connected to external resistors), and the VOUT pin must be connected to the circuit's INPUT voltage.

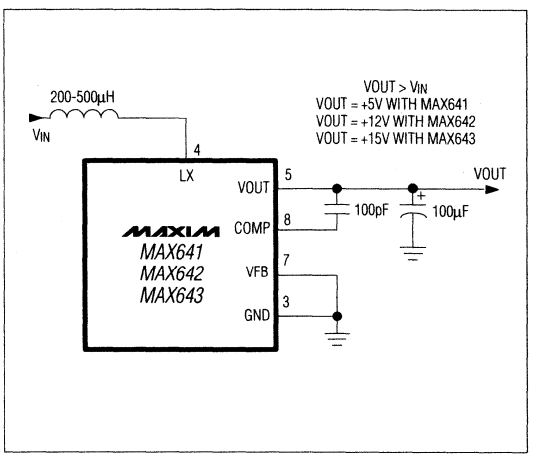


Figure 3. Low-Power, Fixed Output Step-Up Converter Using LX

Fixed Output 10W CMOS Step-up Switching Regulators

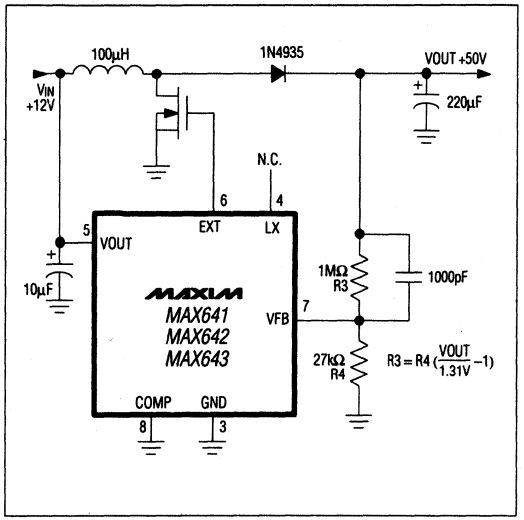


Figure 4. High-Voltage Step-Up Converter

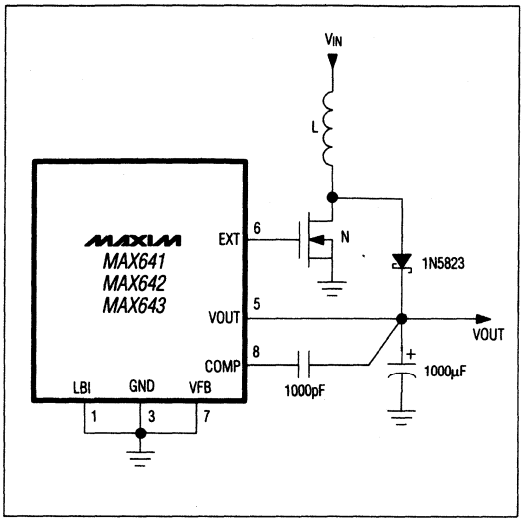


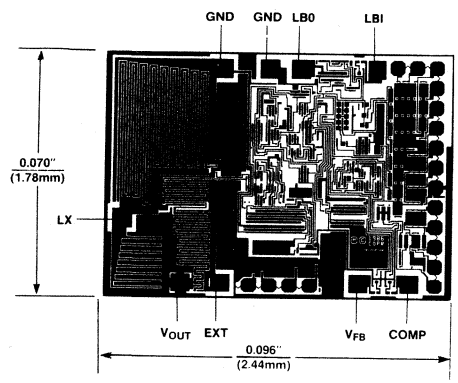
Figure 5. High Output Current Step-Up Converter (See Table 2)

Table 3. Maxim DC-DC Converters

PART NUMBER	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
Low-Power Boost Converters				
MAX630/4193	DC-DC Boost Converter	2V to 16.5V	VOUT>V_{IN}	Improved RC4193 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
High-Power Boost Converters				
MAX641	High-Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High-Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High-Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET
Low-Voltage Boost Converters				
MAX654	Low-Voltage Boost Converter	1.15V to 5.6V	+5V	Optimized for 1 cell
MAX655	Low-Voltage Boost Converter	1.5V to 5.6V	+5V	Optimized for 2 cells
MAX656	Low-Voltage Boost Converter	1.15V to 5.6V	+5V	Drives external MOSFET
MAX657	Low-Voltage Boost Converter	1.15V to 3.6V	+3V	Optimized for 1 cell
MAX658	Low-Voltage Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX659	Low-Voltage Boost Converter	1.5V to 3.6V	+3V	Optimized for 2 cells
Invertering Converters				
MAX634/4391	DC-DC Voltage Inverter	2V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2V to 16.5V	-15V	Only 3 external components
Step-Down Converter				
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	VOUT< V_{IN}	Only 3 external components
Charge-Pump Converters				
MAX680	± Output Charge Pump	2V to 6V	±2V_{IN}	4 external capacitors
MAX681	± Output Charge Pump	2V to 6V	±2V_{IN}	MAX680 with internal capacitors
ICL7660	Negative Charge Pump	1.5V to 10V	-V_{IN}	Not regulated
ICL7662/Si7661	Negative Charge Pump	4.5V to 20V	-V_{IN}	Not regulated
Dual Output Converters				
MAX742	Current-Mode Controller	+5V	±15V/±12V	Drives external MOSFETs
MAX743	Current-Mode Regulator	+5V	±15V/±12V	3W output

Fixed Output 10W CMOS Step-up Switching Regulators

Chip Topography



Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX643XCPA	0°C to +70°C	8 Plastic DIP
MAX643XCSA	0°C to +70°C	8 Narrow SO
MAX643XC/D	0°C to +70°C	8 Dice
MAX643XEPA	-40°C to +85°C	8 Plastic DIP
MAX643XESA	-40°C to +85°C	8 Narrow SO
MAX643XEJA	-40°C to +85°C	8 CERDIP
MAX643XMJA	-55°C to +125°C	8 CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.*

Low Voltage Step-Up DC-DC Converters

General Description

The MAX654-659 step-up DC-DC converters operate from low input voltages such as those supplied by single-cell batteries. They feature a low battery indicator and can run in standby mode to prolong battery life. A Power Ready output provides a means to control external circuitry when standby mode is used.

The performance characteristics of each device are listed in the following table. The MAX654/656/657 are optimized for single-cell input, while the MAX655/658/659 work best with two series alkaline or NiCad cells, or one lithium cell. The MAX654/655/657/659 contain an internal power MOSFET, while an external MOSFET is required with the MAX656/658.

PART	TYP INPUT RANGE (V)	OUT (V)	POWER SWITCH	OUTPUT (mA)
MAX654	1.15-1.56	5	Internal	40
MAX655	2.30-3.10	5	Internal	60
MAX656	1.15-1.56	5	Ext MOSFET	170
MAX657	1.15-1.56	3	Internal	60
MAX658	2.30-3.10	5	Ext MOSFET	110
MAX659	2.30-3.10	3	Internal	60

Applications

Battery-Powered Devices

Single-Cell Instruments

Pagers and Radio Controlled Receivers

4-20mA Loop Powered Instruments

Features

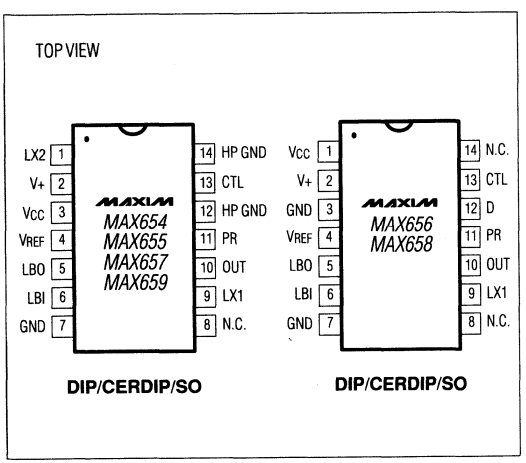
- ♦ **+5V at 170mA from a Single-Cell Battery**
- ♦ **Guaranteed Start-Up at 1.15V**
- ♦ **Minimum Component Count**
- ♦ **Shutdown Mode–80µA Quiescent Current**
- ♦ **Low Battery Indication**
- ♦ **Power Ready Function**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX654CPD	0°C to +70°C	14 Plastic DIP
MAX654CSD	0°C to +70°C	14 Narrow SO
MAX654C/D	0°C to +70°C	Dice
MAX654EPD	-40°C to +85°C	14 Plastic DIP
MAX654ESD	-40°C to +85°C	14 Narrow SO
MAX654MJD	-55°C to +125°C	14 CERDIP
MAX655CPD	0°C to +70°C	14 Plastic DIP
MAX655CSD	0°C to +70°C	14 Narrow SO
MAX655C/D	0°C to +70°C	Dice
MAX655EPD	-40°C to +85°C	14 Plastic DIP
MAX655ESD	-40°C to +85°C	14 Narrow SO
MAX655MJD	-55°C to +125°C	14 CERDIP

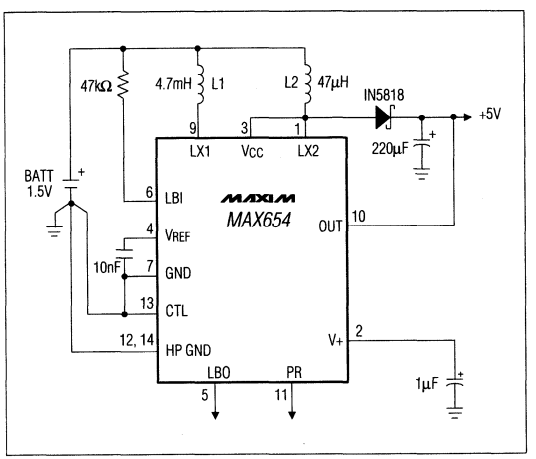
Ordering information continued on page 5-56.

Pin Configurations



DIP/CERDIP/SO DIP/CERDIP/SO

Typical Operating Circuit



Low Voltage Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Peak Voltage at LX1 Pin ..... +16V
Peak Voltage at LX2 or V_{CC} Pin ..... +6.6V
Supply Voltage to L1 ..... +15V
Supply Voltage to L2, V_{CC} ..... +5.6V
Peak Current, LX1 ..... 50mA
Peak Current, LX2 ..... 1.6A
LBO Output Current 50mA
Input Voltage, CTL, LBI (Note 1) ..... -0.3V to (V+ + 0.3V)

Operating Temperature
MAX65XCXX ..... 0°C to +70°C
MAX65XEXX ..... -40°C to +85°C
MAX65XMXX ..... -55°C to +125°C
Power Dissipation
Plastic DIP (derate 10mW/°C above 70°C) 800mW
SO (derate 8.7mW/°C above 70°C) 695mW
CERDIP (derate 9.5mW/°C above 70°C) 750mW
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 Sec) ..... +300°C

Note 1: V+ is generated at LX1. In low current mode, it is 4.5V to 5.6V (2.6V to 3.6V on MAX657, 659); in high current mode, it is 10V to 15V.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX654, MAX656, MAX657

(GND = 0V, V_{BATT} = 1.2V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	MAX654, MAX656	$T_A = T_{MIN}$ to T_{MAX}	4.5	5.0	5.5	V
		MAX657	$T_A = T_{MIN}$ to T_{MAX}	2.7	3.0	3.3	
Output Current	I_L				See Table 1		mA
Minimum Input Voltage to LX1	V_{LX1}	I_L = 0µA			0.9	1.0	V
Minimum Startup Voltage to LX1	V_{LX1}	I_L = 0µA			1.1	1.15	V
Input Voltage to LX2	V_{LX2}					5.6	V
Peak LX2 Switch Current	I_{LX2}	MAX654, MAX657				1.5	A
Standby Current	I_Q	I_L = 0µA, CTL = Open			80		µA
Switching Frequency	f_0	V_{BATT} = 1.0V to 1.6V		15.5	18	24	kHz
		$T_A = T_{MIN}$ to T_{MAX}			18		
LX2, D Switch Duty Cycle	%ON	MAX654, MAX656		66	75	80	%
		MAX657		50	66	75	
LX2, D Switch On Time	t_{ON}	MAX654, MAX656		30	42	46	µs
		MAX657		23	37	44	
LX2 On Resistance	R_{DSON}	MAX654, MAX657		0.40		0.67	Ω
D Output Saturation Current		MAX656	Source Sink		-25 100		mA
Low Battery Input Threshold Voltage	V_{LBI}			1.12		1.18	V
Low Battery Input Threshold Tempco					-0.5		mV/°C
Low Battery Input Bias Current	I_{LBI}				0.01	10	nA
Low Battery Output	V_{LBO}	V_{LBI} < 1.12V, I_{LBO} = 1.6mA V_{LBO} > 1.18V, I_{LBO} = -1µA		V+-1		0.4	V
CTL Input Threshold	V_{CTL}				0.7		V
PR Output	V_{PR}	PR High, I_{PR} = -1µA PR Low, I_{PR} = 1mA			V_{OUT} - 0.2 0.3		V

ELECTRICAL CHARACTERISTICS: MAX655, MAX658, MAX659

(GND = 0V, V_{BATT} = 2.4V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	MAX655, MAX658	$T_A = T_{MIN}$ to T_{MAX}	4.5	5.0	5.5	V
		MAX659	$T_A = T_{MIN}$ to T_{MAX}	2.7	3.0	3.3	
Output Current	I_L				See Table 1		mA
Minimum Input Voltage to LX1	V_{LX1}	I_L = 0µA			0.9	1.0	V
Minimum Startup Voltage to LX1	V_{LX1}	I_L = 0µA			1.0	1.5	V
Input Voltage to LX2	V_{LX2}					5.6	V
Peak LX2 Switch Current	I_{LX2}					1.5	A
Standby Current	I_Q	I_L = 0µA, CTL = Open			40		µA
Switching Frequency	f_0	V_{BATT} = 2.0V to 3.2V		15.5	18	24	kHz
		$T_A = T_{MIN}$ to T_{MAX}			18		
LX2, D Switch Duty Cycle	%ON	MAX655, MAX658		40	50	60	%
		MAX659		25	33	37	
LX2, D Switch On Time	tON	MAX655, MAX658		18	28	35	µs
		MAX659		12	18	22	
LX2 On Resistance	R_{DSON}			0.40		0.67	Ω
D Output Saturation Current		MAX658	Source Sink		-25 100		mA
Low Battery Input Threshold Voltage	V_{LBI}			1.12		1.18	V
Low Battery Input Threshold Tempco					-0.5		mV/°C
Low Battery Input Bias Current	I_{LBI}				0.01	10	nA
Low Battery Output	V_{LBO}	V_{LBI} < 1.12V, I_{LBO} = 1.6mA V_{LBI} > 1.18V, I_{LBO} = -1µA		V+ -1		0.4	V
CTL Input Threshold	V_{CTL}				0.7		V
PR Output	V_{PR}	PR High, I_{PR} = -1µA PR Low, I_{PR} = 1mA			V_{OUT} - 0.2 0.3		V

Operating Principle

The MAX654-659 are step-up converters; energy from a battery is first stored in a coil and then discharged to the load. Essentially, the circuit consists of a battery in series with a coil (L2) and switch (LX2), along with a rectifier (D1) and filter capacitor (C1) as shown in Figure 1. When the switch is closed, current builds up in the coil, creating a magnetic field. Next, the switch opens, the magnetic field collapses, and the voltage across the inductor reverses polarity. This voltage adds to that of the battery and supplies current to the load via the rectifier.

The switch is controlled by a constant frequency oscillator whose output is gated on and off by a comparator that monitors the output voltage. When V_{OUT} rises above the comparator threshold, the MOSFET at LX2 is held off.

The key to operating CMOS circuitry from a 1V supply depends on a technique called bootstrapping. A specially designed oscillator starts itself up on a very low voltage and builds up (or bootstraps) a higher voltage that in turn is used as the supply for further operation. The bootstrapped supply yields higher efficiency because it can drive the gate of the internal FET transistors to lower on resistances.

When power is first applied, the circuit is very inefficient for the first cycle until a higher voltage is generated on the flyback half of the cycle. This higher voltage is rectified and filtered and powers the entire IC (and thus the oscillator) for the next cycle. Since each cycle generates a higher voltage for the next cycle, the voltage builds up very rapidly. An internal regulator limits the voltage to about 12V. The load for this supply is only the CMOS chip itself, so the requirements for the external inductor, L1, are not demanding. The +12V supply is brought out to the V+ pin and is connected to a tantalum capacitor for filtering.

The bootstrapped 12V drives an internal N-channel power FET that furnishes the switching power for the load.

Low Voltage Step-Up DC-DC Converters

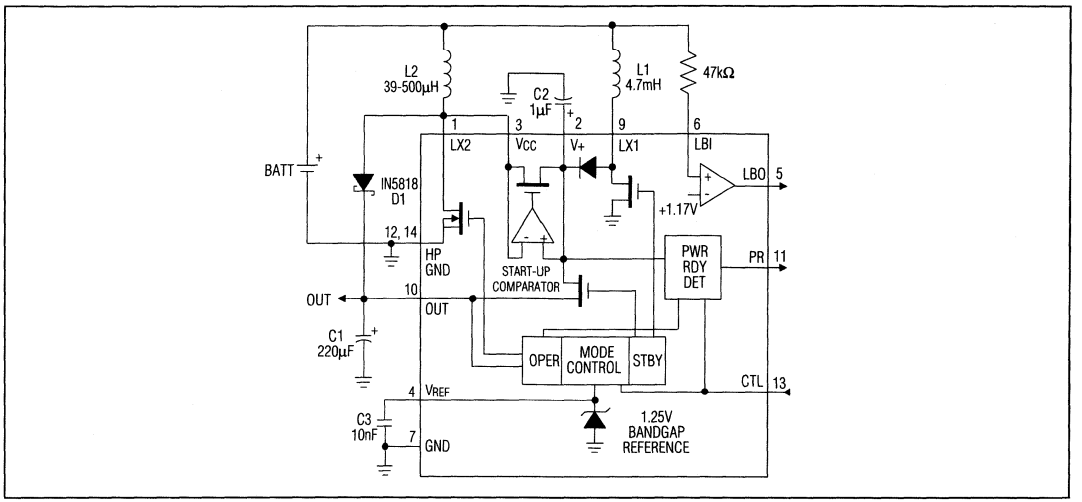


Figure 1. MAX654/655/657/659 Block Diagram

Since the gate of this FET is driven from a 12V supply, it has a very low on resistance and can efficiently switch high currents through a second inductor, L2. It is the power stored in this second inductor that is delivered to the 5V load via an external Schottky diode. The rectified 5V output is connected back to the OUT pin to provide feedback. The MAX654-659 thus have two separate switching circuits and use two separate inductors.

Circuit Details

A typical application circuit is shown in Figure 3. The higher value inductor, L1, is typically 4.7mH, and may

Pin Description

MAX656 MAX658 PIN #	MAX654 MAX655 MAX657 MAX659 PIN #	NAME	FUNCTION
–	1	LX2	Output (drain) of high-power N-channel power MOS switch.
1	3	VCC	Start-up Bias Input; MAX654/655/657: connect to LX2. MAX656/658: connect to drain of external MOSFET.
2	2	V+	Output of low power-up converter; 10V to 15V in high-power mode, 4.5V to 5.6V in MAX654/655/656/658 standby mode, 2.6V to 3.6V in MAX657/59 standby mode.
3, 7	7	GND	Low-Power Ground.
4	4	VREF	1.25V bandgap reference output; should be decoupled with a capacitor to pin 3. This terminal is high impedance and cannot source or sink current.
5	5	LBO	Low Battery Monitor Output. Sinks 1.6mA when LBI is less than 1.17V, otherwise sources 1µA from V+.
6	6	LBI	Low Battery Monitor Input 1.17V threshold.
8, 14	8	N.C.	No Connection.
9	9	LX1	Output (drain) of low-power N-channel power driver.
10	10	OUT	+5V (+3V on MAX657/659). Feedback (input) pin for high-power operation; output pin in standby mode.
11	11	PR	Power Ready Output; high when high-power converter is ready to supply power. High output level = VOUT.
-	12, 14	HP GND	High-Power Ground.
13	13	CTL	Control Mode Switch Input; open circuit or high for standby mode, ground for high-power mode.
12	–	D	Driver output to external FET Output voltage swings from GND to V+.

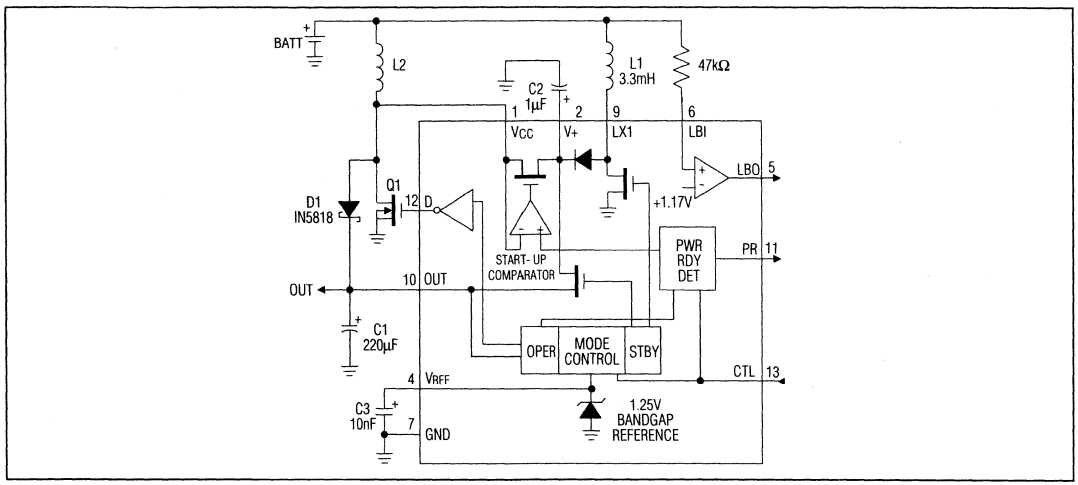


Figure 2. MAX656/658 Block Diagram

have fairly high losses. It is used for the low-power section of the circuit and is rectified by an internal diode and routed to V+, where it is filtered by an external capacitor, C1. The second inductor, L2, ranges from 12µH to 500µH, depending on input voltage and load current. It must have low series resistance and have sufficient core material to handle the load power without saturating. With the MAX654/5/7/8, the inductor, L2, is connected to LX2, which is simply the drain of the high-power FET. Current flowing through L2 is rectified by an external Schottky diode, D1, and filtered by an external capacitor, C2. This is the main +5V output (+3V on the MAX657/659). It is connected to the OUT pin which is the feedback input in high-power mode. Figure 4 shows a similiar circuit with the MAX656 using an external FET for higher power output.

Low-Power Standby Mode

A control pin (CTL) puts the device into standby mode to conserve power. When this pin is held low, the IC operates normally. But if it is driven high or left open, the chip goes into standby. Several things happen in standby mode: the PR pin is driven low, the high-power FET is gated off, the 12V (V+) switching supply is reduced to

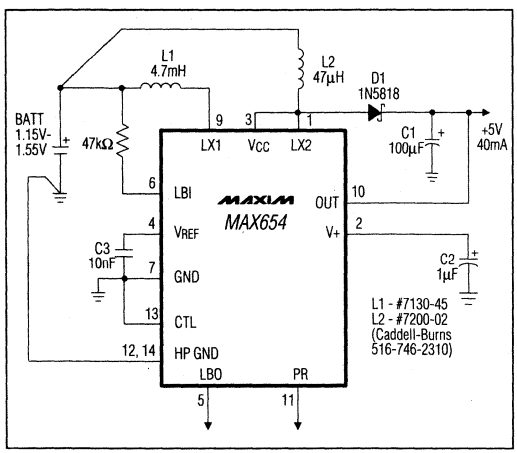


Figure 3. MAX654 Typical Application

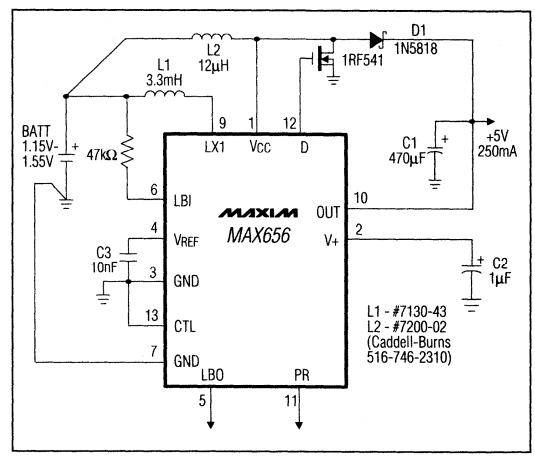


Figure 4. MAX656 Typical Application

Low Voltage Step-Up DC-DC Converters

+5V (+3V on the MAX657/659) and is connected to the OUT pin. By lowering the internal 12V supply to 5V, the leakage currents of the CMOS circuits (and the losses associated with its voltage reference and oscillator) are reduced to a minimum. The internal low-power 5V supply can furnish up to 500µA and is connected to the normal 5V OUT pin to supply current to standby circuitry.

Power Ready Output Pin

During initial start-up (and when placed in standby mode), the MAX654-659 internal voltages are too low to drive the power FET efficiently. A separate comparator determines when this voltage has reached a high enough value to drive the power FET. The output of this comparator gates the FET drive signal. This scheme extends battery life in standby mode and prevents the power FET from stalling when switching to high-power mode. The comparator output appears at the PR pin and can be used to control external circuitry, such as the gate of a MOSFET connecting the load to the power supply, further reducing battery drain.

Start-Up and Mode Considerations

The MAX654-659 may be started up in either low-power (standby) or high-power mode. When starting in the high-power mode, both the low-power switch and the high-power switch start immediately. Whether or not the load is connected, the output voltage will rise to 5V in the first few cycles. Note that in the high-power mode, the OUT pin is used as a feedback input.

If a high-power load (greater than about 500µA) is connected to the OUT pin and the device is placed in the low-power mode via the CTL pin, the low-power oscillator will have to furnish all of the 5V power via the OUT pin, and the low-power oscillator will stall. Therefore, it is important to disconnect any load currents (greater than 500µA) whenever the low-power or standby mode is selected. The PR pin may be used to disconnect the load via an external transistor.

Input Filtering

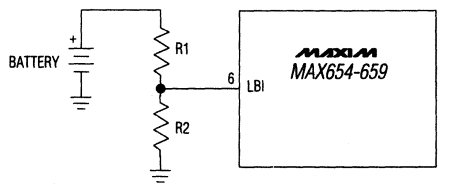
It is important to limit the rate of rise of the input voltage if the circuit is first turned on with a mechanical switch or by the installation of battery(ies). A simple R-C network made up of the battery's internal resistance and a 10µF tantalum capacitor placed at the battery side of L2 input is sufficient for this purpose. This capacitor also helps to absorb the (relatively) high peak currents that are drawn from the battery in the high-power mode.

Output Filtering

An output reservoir capacitor must be placed on the OUT pin to provide filtering for the 5V output. Capacitor values should be 100µF or greater, with low effective series resistance to minimize output ripple. The V+ pin (12V) should be filtered with a 1µF capacitor, tied between the V+ pin and ground.

Low Battery Function

A completely independent low battery monitor is built into the MAX654-659. Its input, LBI, is the + input of a CMOS comparator whose input is connected to an internal 1.17V reference. This input can be connected directly to the battery in single-cell circuits. The trip voltage of the Low Battery Detector may be adjusted using an external voltage divider as shown in Figure 5. The output, LBO, can sink 1.6mA or source several microamperes from V+. Place a 47kΩ resistor in series with the LBI pin.



$10k\Omega \le R2 \le 10M\Omega$

$$R1 = R2\left(\frac{V_{LB}}{1.17} - 1\right)$$

V_{LB} = Trip Point of Low Battery Detector

Figure 5. Setting Low Battery Detector Trip Point

Inductor Selection

Low-Power Coil, L1

For the low-power inductor (L1) a 4.7mH coil with a DC resistance of less than 40Ω is adequate for most applications. In general, higher inductance values allow lower start-up voltages, while lower resistances yield lower quiescent current in standby mode. If the inductance is made too high, the low-power (V+) output voltage and current are reduced. This in turn reduces the efficiency of the power section, so the +5V output (in standby mode) supplies less current. Lower values of inductance raise the minimum start-up voltage.

High-Power Coil, L2

The high-power coil, L2, stores most of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core and have low series resistance to minimize losses. It also must have an adequate current rating to prevent saturation.

A coil must be selected that keeps the peak current at LX2 below the maximum rating of the switch. This maximum is 1.5A for the MAX654/55/57/59 and depends on the current rating of the external FET and inductor when using the MAX656/58. The optimum inductance can be found using Figures 6-11 (refer to the Output Current vs. Input Voltage Section), or inductance values may be approximated from Table 1, or finally, the inductance may be calculated as follows:

The first step is to calculate the minimum permissible inductance that keeps the peak current below the current rating of the individual components. This is done using the highest expected input voltage ($V_{IN(MAX)}$), the longest on time per cycle for the LX2 switch ($t_{ON(MAX)}$), and the lowest total series resistance, R_{MIN}, where R_{MIN} is the sum of the minimum coil and FET resistances. These are the conditions under which the highest coil current flows.

For the MAX654, from the Electrical Characteristics table:

I_{pk} of LX2 = 1.5A
$R_{DSON(MIN)} = 0.4\Omega$
$f_{0(MIN)}$ = 15,500Hz
duty cycle maximum, %ON(MAX) = 0.8
$t_{ON(MAX)} = 46\mu s$

Assume that the minimum coil resistance , $R_{COIL(MIN)}$ is:

$$R_{COIL(MIN)} = 0.1\Omega$$

The minimum total resistance, $R_{(MIN)}$ is:

$$R_{(MIN)} = R_{DSON(MIN)} + R_{COIL(MIN)} = 0.4 + 0.1 = 0.5\Omega$$

Then:

$$I_{pk} = 1.5A = \frac{V_{IN(MIN)}}{R_{(MIN)}} \times [1-e^{-R_{(MIN)}\, t_{ON(MAX)} / L_{(MIN)}}]$$

or:

$$L_{(MIN)} = \frac{-R_{(MIN)}\, t_{ON(MAX)}}{ln\left[1-R_{(MIN)}\, I_{pk}/V_{IN(MAX)}\right]}$$

The above two equations "blow up" if R(MIN) = 0, but work fine for $R_{(MIN)} \geq 0.001\Omega$. For a maximum input voltage of 1.56V (single alkaline cell) and a minimum coil resistance of 0.1Ω, the minimum permissible inductance for the MAX654/57 is 35.1µH.

Having determined the minimum inductance that keeps the peak current below the individual component ratings, we next calculate a new peak current (I'_{pk}) using the highest resistance ($R_{(MAX)}$) and the lowest input voltage ($V_{IN(MIN)}$). Using these parameters, we will calculate the minimum available output (DC) current.

From the Electrical Characteristics table:

$R_{DSON(MAX)} = 0.67\Omega$
$f_{0(MAX)}$ = 24,000Hz
duty cycle minimum, %ON(MIN) = 0.66
$t_{ON(MIN)} = 30\mu s$

The inductance tolerance of L2 has some impact on these calculations. In the following equations, a new $L_{(MIN)}$ based on the manufacturer's tolerance specification is used. This example assumes ±10% tolerance, so 90% of the nominal inductance is used.

Assume that the maximum coil resistance, $R_{COIL(MAX)}$ is:

$$R_{COIL(MAX)} = 0.15\Omega$$

The maximum total charging resistance, $R_{(MAX)}$ is:

$$R_{(MAX)} = R_{DSON(MAX)} + R_{COIL(MAX)} = 0.82\Omega$$

At the end of the ON period:

$$I'_{pk} = \frac{V_{IN(MIN)}}{R_{(MAX)}} \times [1-e^{-R_{(MAX)}\, t_{ON(MIN)}/L_{(MIN)}}]$$

The energy stored in the in the coil is:

$$E_{COIL} = \frac{L_{(MIN)} \times I'^{2}_{pk}}{2}$$

And the power put into the coil is:

$$P_{COIL} = f_{0(MAX)} \times E_{COIL}$$

$$= \frac{L_{(MIN)} \times I'^{2}_{pk} \times f_{0(MAX)}}{2}$$

The minimum available DC output current, I_{OUT}, is:

$$I_{OUT} = \frac{P_{LOAD}}{V_{LOAD}} = \frac{P_{COIL} - P_{LOSS}}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}}$$

$$= \frac{P_{COIL} - I'^{2}_{pk} \times R_{COIL(MAX)}/3 \times (1-\%ON_{(MIN)})}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}}$$

Using a 47 ±10% µH coil with a resistance of 0.15Ω and an input voltage of 1.1V, the minimum available 5V output current at the highest output voltage (5.5V) would be 36.3mA. This assumes a 0.3V forward drop in the IN5818 diode.

When selecting a coil, care should be exercised to insure that the minimum inductance value, including all the manufacturing tolerances, is never lower than the calculated inductance. Otherwise, the peak current rating of LX2 may be exceeded. In addition, the current rating of the coil should be greater than the peak current used in the calculation (1.5A normally) to avoid saturating the core.

If the worst case output current is too small, either the minimum input voltage must be increased or the maximum input voltage should be decreased. It is always desireable to decrease the ratio between maximum and

Low Voltage Step-Up DC-DC Converters

Table 1. Operation with Common Batteries

MAXIM PART #	BATTERY TYPE	BATTERY VOLTAGE		OUTPUT		COIL SPECIFICATIONS (L2)		
		MIN	MAX			µH*	OHMS	PART #
MAX654	1 NiCad	1.15V	1.35V	5V	43mA	39	0.05	6860-08
MAX654	1 Alkaline	1.2V	1.55V	5V	43mA	47	0.05	6860-09
MAX654*	1 Alkaline	1.2V	1.55V	5V	10mA	120	0.14	6860-14
MAX655	2 NiCads	2.3V	2.7V	5V	64mA	68	0.07	6860-11
MAX655	2 Alkalines	2.4V	3.1V	5V	62mA	82	0.07	6860-12
MAX655	1 Lithium	2.6V	3.6V	5V	64mA	100	0.10	6860-13
MAX656**	1 NiCad	1.15V	1.35V	5V	250mA	12	0.025	6860-02
MAX656**	1 Alkaline	1.2V	1.55V	5V	275mA	12	0.01	7200-02
MAX657	1 Alkaline	1.2V	1.55V	3V	60mA	39	0.05	6860-08

* Coils are from Caddell-Burns Co. NY (516) 746-2310. Inductance (µH) is the MINIMUM allowed for the listed battery voltage range (Battery Voltage: MIN, MAX). Lower values are not recommended, except when using the MAX656/658 converters since they use an external MOSFET. If less current than listed in the Output column is needed, a higher inductance coil will reduce losses. The optimum inductance varies inversely with required output current if all other conditions are unchanged. For example, refer to line 3 and the 10mA output. 120µH supplies this current more efficiently than the 39µH coil of line 2. L2 may also be calculated using the equations in the Inductor Selection Section.

** These MAX656 circuits (see Figure 4) use an IRF541 as an external current switch. Peak switch current is typically 3.5A.

minimum input voltages. The coil resistance also has a significant effect on the output current. So, selecting a coil with the lower resistance will increase the output current and increase the overall efficiency.

If no satisfactory value of inductance can be found for the desired output current, the MAX656/58 may be used with an external FET whose current rating exceeds 1.5A. The calculations are similiar for the MAX654, except the external FET's R_{DSON} and the current rating of the FET or coil (whichever is lower) should be substituted in the above equations.

If the worst case output current is significantly higher than the required load current, a higher inductance value should be used. This will tend to reduce the peak current and ripple voltage, and tend to raise the overall efficiency. Be sure to adjust the coil resistance and recalculate all values when using another coil.

When the maximum battery voltage exceeds 1.65V, the MAX655/58/59 should be used. Calculations are identical to the MAX654 calculations, except different values must be used for the duty cycle and t_{ON}.

In general, if a choice of batteries is available, higher input voltages are preferred for two reasons. First, as the input voltage approaches 1V, the load on the battery increases while the losses increase. The losses become so dominant that efficiency suffers, and little output current can be maintained. Second, certain losses, such as the coil resistance and the FET on resistance, are less significant with higher input voltages. This means higher efficiency and a greater range of input voltages are tolerable. This in turn means that more of the chemical energy can be converted into electricity.

The inductance values for commonly encountered battery-operated power supplies are tabulated in Table 1.

Capacitor Selection

The high-current, fast rise time pulses associated with switching power supplies demand good grounding and bypassing techniques. The MAX654-658 have 3 ground pins to improve grounding. In addition, the internal voltage reference is brought out for connection to an external **10nF** capacitor, minimizing noise and modulation of the reference.

In order to minimize transients, the two output voltages, V+ and +5V, should be filtered with tantalum capacitors or other types of capacitors with low effective series resisitance. If aluminum electrolytic capacitors are used, they should be paralleled with 0.1µF disc ceramic capacitors.

Rectifier Selection

The MAX654-659 use one external rectifier. To achieve specified performance at low voltages, a Schottky type, such as the 1N5818, is recommended because it combines low forward voltage drop with fast switching speed. This maximizes power conversion efficiency and output current when the DC-DC converter is in high-power mode. One drawback of Schottky rectifiers is relatively high reverse leakage current (at 5V reverse, 1N5818 leakage is typically 60µA at 25°C and 450µA at 75°C), which is quite large with respect to the circuit's quiescent current in standby mode (typical standby current MAX654/56/57: 80µA, MAX655/58/59: 40µA). If standby mode is not used or used only for short periods, reverse leakage is not a significant additional loss compared to the normal load current, and need not be considered.

If quiescent operating current is a primary concern, or if the MAX654-659 spends most of its time in standby mode, a silicon rectifier such as the 1N4933 or Unitrode UES1001 may be preferred. Silicon rectifiers have less reverse leakage current than do Schottky rectifiers (1N4933 leakage current is typically 1µA at 25°C and 50µA at 100°C). In circuits where the standby mode is the predominant mode of operation, battery life may be extended by trading conversion efficiency for lower standby quiescent current.

Output Current vs. Input Voltage

Figures 6 through 11 show output current versus input voltage using typical inductor values for each part in the MAX654-659 Family. Where curves end in the middle of the graphs, the peak current limit of the internal LX2 switch has been reached. A higher input voltage than indicated by that line (for the given inductor) may damage the device. Figures 8 and 10 assume that an IRF541 MOSFET is used (0.085Ω maximum on resistance).

Dashed lines indicate regions where the LX2 current limit hasn't been exceeded, but the current rating of the selected coil (Caddell-Burns 6860 series) has. The actual voltages where lines end or become dashed are indicated by arrows on the graphs. The output currents indicated by dashed lines can be achieved only with inductors of higher current rating than the indicated coil (such as Caddell-Burns 7200 series or a toriod, for example). The coils used in Figures 6, 7, 9, and 11 are as follows:

33µH - 6860-07	Caddell-Burns
47µH - 6860-09	(516) 746-2310
100µH - 6860-13	
150µH - 6860-15	
220µH - 6860-17	

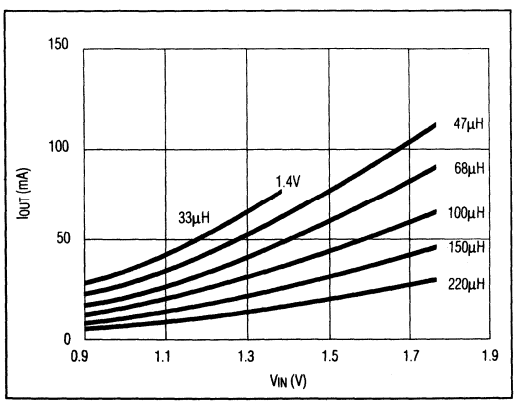


Figure 6. MAX654, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

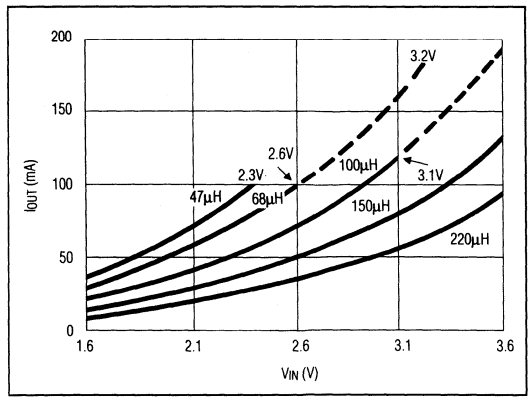


Figure 7. MAX655, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

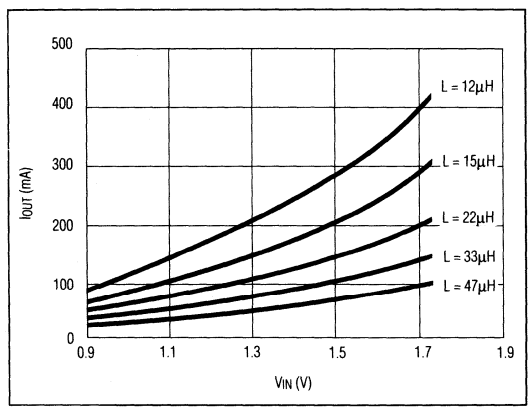


Figure 8. MAX656, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

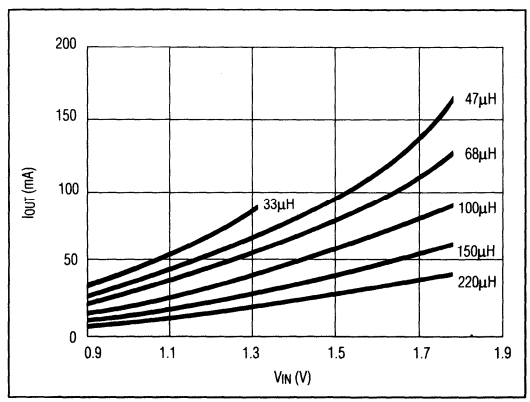


Figure 9. MAX657, I_{OUT} vs. V_{IN} (V_{OUT} = 3V)

Low Voltage Step-Up DC-DC Converters

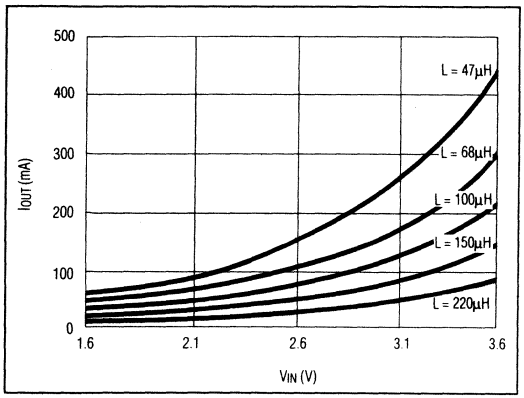


Figure 10. MAX658, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

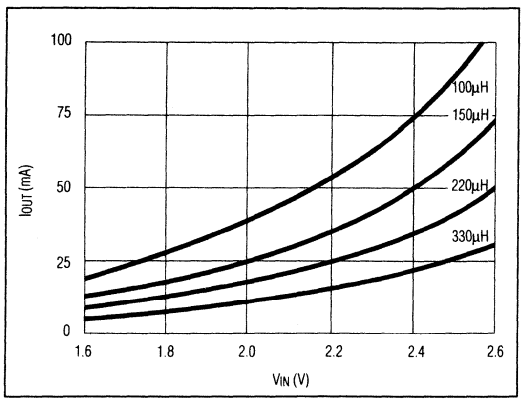


Figure 11. MAX659, I_{OUT} vs. V_{IN} (V_{OUT} = 3V)

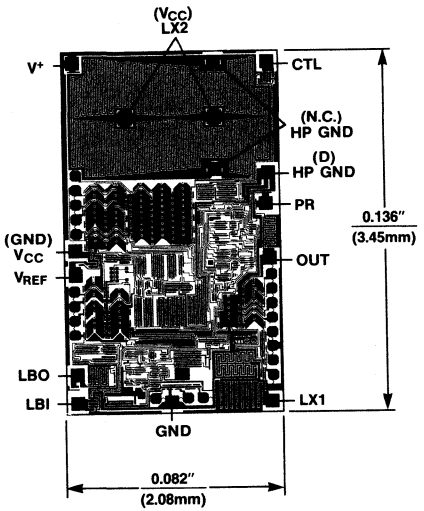
The coils used in Figures 8 and 10 are the Caddell-Burns 7200 series inductors.

The graphs in Figures 6-11 were calculated using worst case data, so individual circuits may supply more current than indicated. If the coils' current ratings are not exceeded, smaller, lower-cost coils than those indicated may be used in low-current applications. Use the equations in the text to calculate worst case peak coil/switch current to be sure that a particular coil's current rating is sufficient.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX656CPD	0°C to +70°C	14 Plastic DIP
MAX656CSD	0°C to +70°C	14 Narrow SO
MAX656C/D	0°C to +70°C	Dice
MAX656EPD	-40°C to +85°C	14 Plastic DIP
MAX656ESD	-40°C to +85°C	14 Narrow SO
MAX656MJD	-55°C to +125°C	14 CERDIP
MAX657CPD	0°C to +70°C	14 Plastic DIP
MAX657CSD	0°C to +70°C	14 Narrow SO
MAX657C/D	0°C to +70°C	Dice
MAX657EPD	-40°C to +85°C	14 Plastic DIP
MAX657ESD	-40°C to +85°C	14 Narrow SO
MAX657MJD	-55°C to +125°C	14 CERDIP
MAX658CPD	0°C to +70°C	14 Plastic DIP
MAX658CSD	0°C to +70°C	14 Narrow SO
MAX658C/D	0°C to +70°C	Dice
MAX658EPD	-40°C to +85°C	14 Plastic DIP
MAX658ESD	-40°C to +85°C	14 Narrow SO
MAX658MJD	-55°C to +125°C	14 CERDIP
MAX659CPD	0°C to +70°C	14 Plastic DIP
MAX659CSD	0°C to +70°C	14 Narrow SO
MAX659C/D	0°C to +70°C	Dice
MAX659EPD	-40°C to +85°C	14 Plastic DIP
MAX659ESD	-40°C to +85°C	14 Narrow SO
MAX659MJD	-55°C to +125°C	14 CERDIP

Chip Topography



Note: Labels in ( ) are for MAX656/MAX658 only

19-3293; Rev. 0; 3/91

MAXIM

CMOS Monolithic Voltage Converter

General Description

The MAX660 monolithic, charge-pump voltage inverter converts a +1.5V to +5.5V input to a corresponding -1.5V to -5.5V output. Using only two low-cost capacitors, the charge pump's 100mA output replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current range combined with a typical operating current of only 200µA provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX660 can also double the output voltage of an input power supply or battery, providing +9.35V at 100mA from a +5V input.

A Frequency Control (FC) pin selects either 10kHz or 45kHz operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX660 is a pin-compatible high-current upgrade of the ICL7660.

The MAX660 is available in both 8-pin DIP and small outline packages in commercial, extended, and military temperature ranges.

Applications

Laptop Computers

Medical Instruments

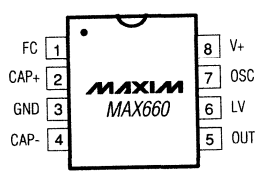
Interface Power Supplies

Handheld Instruments

Operational-Amplifier Power Supplies

Pin Configuration

TOP VIEW



DIP/SO

Features

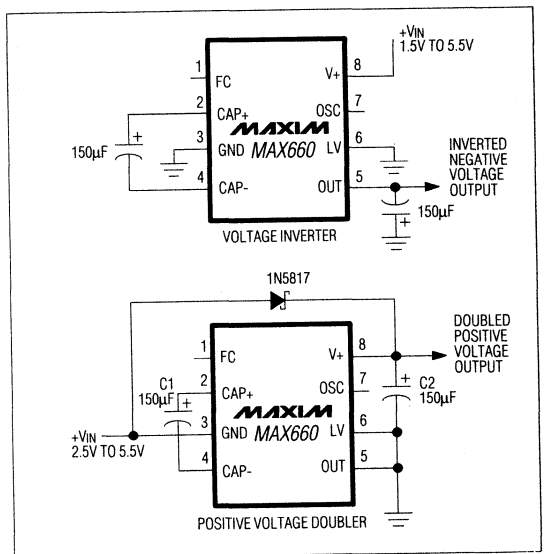
- ♦ 0.65V Typ Loss at 100mA Load
- ♦ 6.5Ω Typ Output Impedance
- ♦ Pin-Compatible High-Current ICL7660 Upgrade
- ♦ Inverts or Doubles Input Supply Voltage
- ♦ Selectable Oscillator Frequency: 10kHz/45kHz
- ♦ 88% Typ Conversion Efficiency at 100mA (I_L to GND)
- ♦ 200µA Operating Current

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX660CPA	0°C to +70°C	8 Plastic DIP
MAX660CSA	0°C to +70°C	8 SO
MAX660C/D	0°C to +70°C	Dice*
MAX660EPA	-40°C to +85°C	8 Plastic DIP
MAX660ESA	-40°C to +85°C	8 SO
MAX660MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuits



CMOS Monolithic Voltage Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to OUT) ..... +6V
LV Input Voltage ..... OUT - 0.3V to V+ + 0.3V
FC and OSC Input Voltages ..... (the least negative of OUT - 0.3V or V+ - 6V) to V+ + 0.3V
OUT and V+ Continuous Output Current 120mA
Output Short-Circuit Duration to GND (Note 1) ..... 10 sec.
Continuous Total Power Dissipation (T_A = +70°C)
Plastic DIP (derate 6.9mW/°C above +70°C) 552mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.0mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX660C _ _ ..... 0°C to +70°C
MAX660E _ _ ..... -40°C to +85°C
MAX660MJA ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V; C1, C2 = 150µF; test circuit of Figure 1; FC = open; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	R_L = 1kΩ	Inverter, LV = open	3		5.5	V
		Inverter, LV = GND	1.5		5.5	
		Doubler, LV = OUT	2.5		5.5	
Supply Current	No Load	FC = open		0.2	0.5	mA
		FC = V+		1	3	
Output Current	T_A ≤ +85°C, OUT more negative than -4V		100			mA
	T_A > +85°C, OUT more negative than -3.8V		100			
Output Resistance (Note 3)	I_L = 100mA	T_A ≤ +85°C		6.5	10	Ω
		T_A > +85°C			12	
Oscillator Frequency	FC = open			10		kHz
	FC = V+			45		
OSC Input Current	FC = open			±1.1		µA
	FC = V+			±5		
Power Efficiency	R_L = 1kΩ connected between V+ and OUT		96	98		%
	R_L = 500Ω connected between OUT and GND		92	96		
	I_L = 100mA to GND			88		
Voltage Conversion Efficiency	No Load		99	99.96		%

Note 1: In inverting mode, OUT may be shorted to GND for 10 sec. without damage, but shorting OUT to V+ may damage the device and should be avoided. In doubler mode, shorts of V+ to OUT can be tolerated indefinitely, but the Schottky diode current rating could be exceeded. In doubler mode, V+ may be shorted to GND for 10 sec. without damage.
Note 2: In the test circuit, capacitors C1 and C2 are 150µF, 0.2Ω maximum ESR, aluminum electrolytics (Maxim part # MAXC001). Capacitors with higher ESR may reduce output voltage and efficiency.
Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See *Capacitor Selection* section.

Typical Operating Characteristics

(All curves are generated using the test circuit of Figure 1 with V+ = 5V, LV = GND, FC = open, and T_A = +25°C, unless otherwise noted. The charge-pump frequency is one-half the oscillator frequency. Test results are also valid for doubler mode with GND = +5V, LV = OUT, and OUT = 0V, unless otherwise noted; however, the input voltage is restricted to +2.5V to +5.5V.

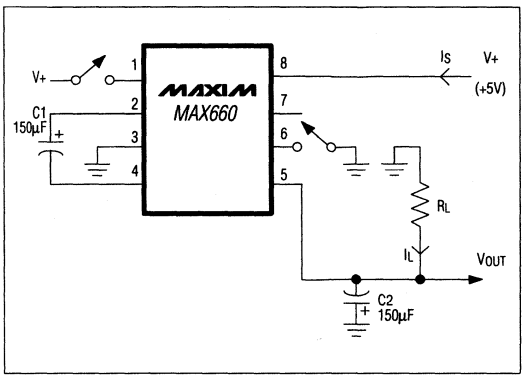
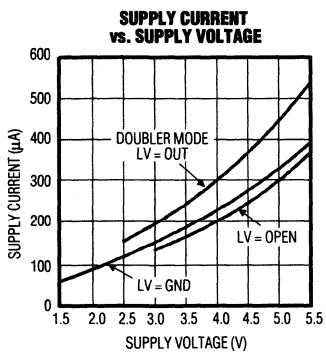
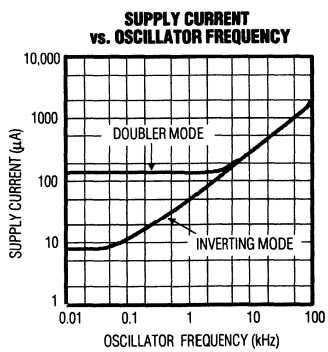
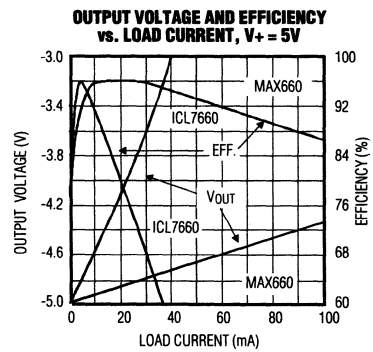
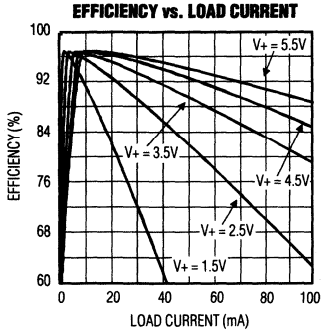


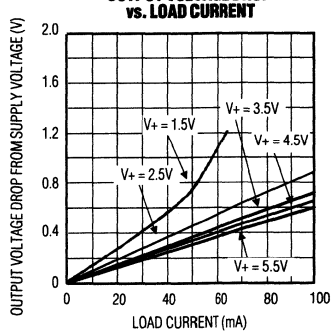
Figure 1. MAX660 Test Circuit

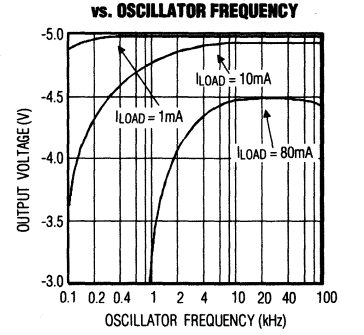








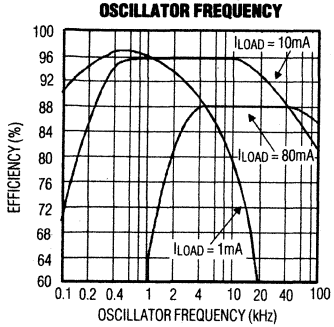




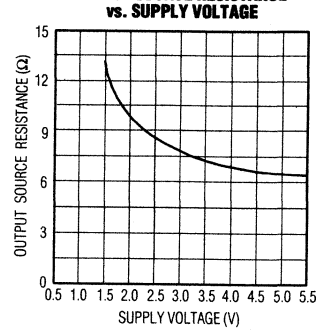
CMOS Monolithic Voltage Converter

Typical Operating Characteristics (continued)

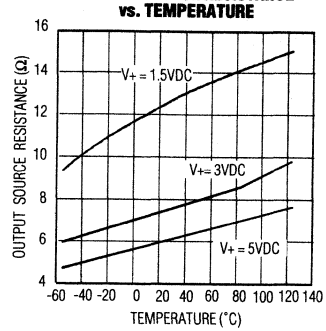
EFFICIENCY vs. OSCILLATOR FREQUENCY



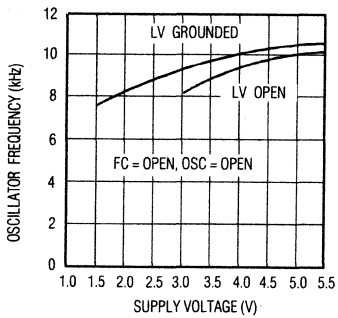
OUTPUT SOURCE RESISTANCE vs. SUPPLY VOLTAGE



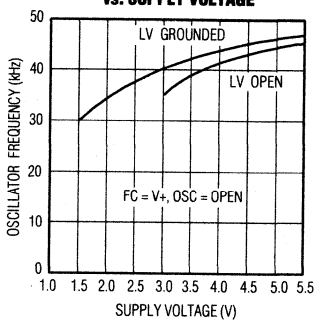
OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



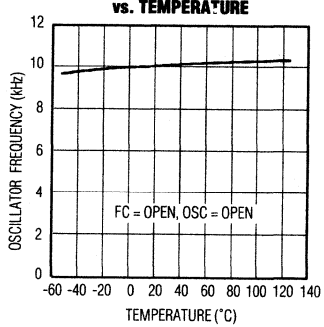
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



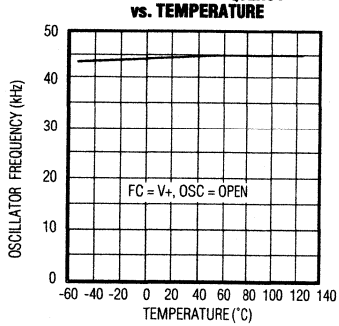
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



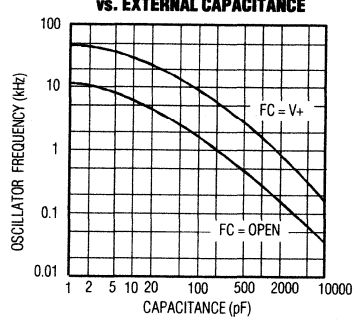
OSCILLATOR FREQUENCY vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. EXTERNAL CAPACITANCE



Pin Description

PIN	NAME	FUNCTION	
		INVERTER	DOUBLER
1	FC	Frequency Control for internal oscillator. FC = open, f_{OSC} = 10kHz typ; FC = V+, f_{OSC} = 45kHz typ; FC has no effect when OSC pin is driven externally.	Same as Inverter
2	CAP+	Charge-Pump Capacitor, Positive Terminal	Same as Inverter
3	GND	Power-Supply Ground Input	Power-Supply Positive Voltage Input
4	CAP-	Charge-Pump Capacitor, Negative Terminal	Same as Inverter
5	OUT	Output, Negative Voltage	Power-Supply Ground Input
6	LV	Low-Voltage Operation Input. Tie LV to GND when input voltage is less than 3V. Above 3V, LV may be connected to GND or left open; when overdriving OSC, LV must be connected to GND.	LV must be tied to OUT for all input voltages.
7	OSC	Oscillator Control Input. OSC is connected to an internal 15pF capacitor. An external capacitor can be added to slow the oscillator. Care must be taken to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC.	Same as Inverter; however standard logic levels cannot overdrive OSC in voltage doubler mode. Contact factory for details.
8	V+	Power-Supply Positive Voltage Input	Positive Voltage Output

Detailed Description

The MAX660 capacitive charge-pump circuit either inverts or doubles the input voltage. Two external capacitors are needed in the voltage inverting mode, while two capacitors and one diode are needed for the voltage doubling mode (see *Typical Operating Circuits*). For highest performance, low effective series resistance (ESR) capacitors should be used. See *Capacitor Selection* section for more details.

When using the inverting mode with a supply voltage less than 3V, LV must be connected to GND. This bypasses the internal regulator circuitry and provides best performance in low-voltage applications. When using the inverter mode with a supply voltage above 3V, LV may be connected to GND or left open. The part is typically operated with LV grounded, but since LV may be left open, the substitution of the MAX660 for the ICL7660 is simplified. LV must be grounded when overdriving OSC (see *Changing Oscillator Frequency* section). Connect LV to OUT (for any supply voltage) when using the doubler mode.

Application Hints

Negative Voltage Converter

The most common application of the MAX660 is as a charge-pump voltage inverter. The operating circuit uses only two external capacitors, C1 and C2 (see *Typical Operating Circuits*). In most applications these are low-cost, low-ESR, 150µF electrolytic capacitors (Refer to *Capacitor Selection* section).

Even though its output is not actively regulated, the MAX660 is very insensitive to load current changes. A typical output source resistance of 6.5Ω means that with an input of +5V the output voltage is -5V under light load, and decreases only to -4.35V with a load of 100mA. Output source resistance vs. temperature and supply voltage are shown in the *Typical Operating Characteristics* graphs.

Output ripple voltage is calculated by noting the output current supplied is solely from capacitor C2 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(f_{PUMP})\,(C2)} + I_{OUT}\,(ESR_{C2})$$

For a nominal f_{PUMP} of 5kHz (one-half the nominal 10kHz oscillator frequency) and C2 = 150µF with an ESR of 0.2Ω, ripple is approximately 90mV with a 100mA load current. If C2 is raised to 390µF, the ripple drops to 45mV.

CMOS Monolithic Voltage Converter

Positive Voltage Doubler

The MAX660 operates in the voltage-doubling mode as shown in the *Typical Operating Circuit*. The external Schottky (1N5817) diode is for start-up only. The no-load output is 2 x V_{IN} and is not reduced by the diode forward drop.

Changing Oscillator Frequency

Four modes control the MAX660's clock frequency, as listed below:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC = V+	Open	45kHz
Open or FC = V+	External Capacitor	See Typical Operating Characteristics
Open	External Clock	External Clock Frequency

When FC and OSC are unconnected (open), the oscillator runs at 10kHz typically. When FC is connected to V+, the charge and discharge current at OSC changes from 1.1µA to 5µA, thus increasing the oscillator frequency 4.5 times. In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by 4.5 times in this mode, but for a lower range of frequencies (see *Typical Operating Characterisitics*).

In the inverter mode, OSC may also be overdriven by an external clock source that swings within 100mV of V+ and GND. Any standard CMOS logic output is suitable for driving OSC. When OSC is overdriven, FC has no effect. Also, LV must be grounded when overdriving OSC. Standard logic levels cannot overdrive OSC in voltage doubler mode. Contact factory for details.

Note: In all modes, the frequency of the signal appearing at CAP+ and CAP- is one-half that of the oscillator. Also, an undesirable effect of lowering the oscillator frequency is that the effective output resistance of the charge-pump increases. This can be compensated by increasing the value of the charge-pump capacitors (see *Capacitor Selection* section and *Typical Operating Characteristics*).

In some applications, the 5kHz output ripple frequency may be low enough to interfere with other circuitry. If desired, the oscillator frequency can then be increased through use of the FC pin or an external oscillator as described above. The output ripple frequency is one-half the selected oscillator frequency. Increasing the clock frequency increases the MAX660's quiescent current, but also allows smaller capacitance values to be used for C1 and C2.

Capacitor Selection

Three factors (in addition to load current) affect the MAX660 output voltage drop from its ideal value:

1) MAX660 output resistance

2) Pump (C1) and reservoir (C2) capacitor ESRs

3) C1 and C2 capacitance

The voltage drop caused by MAX660 output resistance is the load current times the output resistance. Similarly, the loss in C2 is the load current times C2's ESR. The loss in C1, however, is larger because it handles currents that are greater than the load current during charge-pump operation. The voltage drop due to C1 is therefore about 4 times C1's ESR times the load current. Consequently, a low (or high) ESR capacitor has much greater impact on performance for C1 than for C2.

Generally, as the pump frequency of the MAX660 increases, the capacitance values required to maintain comparable ripple and output resistance diminish proportionately. The curves of Figure 2 show the total circuit output resistance for various capacitor values (the pump and reservoir capacitors' values are equal) and oscillator frequencies. These curves assume 0.25Ω capacitor ESRs and a 5.25Ω MAX660 output resistance, which is why the flat portion of the curve shows a 6.5Ω (R_O MAX660 + 4 (ESR_{C1}) + ESR_{C2}) effective output resistance. Note: R_O = 5.25Ω is used, rather than the typical 6.5Ω, because the typical specification includes the effect of the ESRs of the capacitors in the test circuit.

To reduce the output ripple caused by the charge pump, increase the reservoir capacitor C2 and/or reduce its ESR. Also, the reservoir capacitor must have low ESR if filtering high-frequency noise at the output is important.

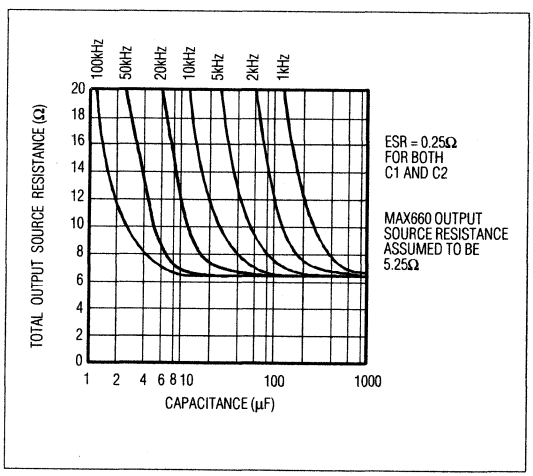


Figure 2. Total Output Source Resistance vs. C1 and C2 Capacitance (C1 = C2)

Not all manufacturers guarantee capacitor ESR in the range required by the MAX660. In general, capacitor ESR is inversely proportional to physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR. The capacitors used when testing the MAX660 are MAXC001 150µF aluminum electrolytics available from Maxim. They combine low cost, a guaranteed maximum ESR of 0.2Ω at room temperature, and a low-temperature operating limit of -25°C. If operation at lower temperatures is required, certain tantalum capacitors provide good low-temperature ESR, but at added expense.

The following is a list of manufacturers who provide low-ESR electrolytic capacitors.

MANUFACTURER	CAPACITOR	CAPACITOR TYPE
Illinois Capacitor	RZS	Aluminum Electrolytic
Mallory	TDC & TDL	Tantalum
Nichicon	PF & PL	Aluminum Electrolytic
Sprague	672D, 673D, 674D, 678D	Aluminum Electrolytic
Sprague	135D, 173D, 199D	Tantalum
United Chemi-con	LXF & SXF	Aluminum Electrolytic

Cascading Devices

To produce larger negative multiplication of the initital supply voltage, the MAX660 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the sum of the individual MAX660 R_{OUT} values. The output voltage, where n is an integer representing the number of devices cascaded, is defined by $V_{OUT} = -n (V_{IN})$.

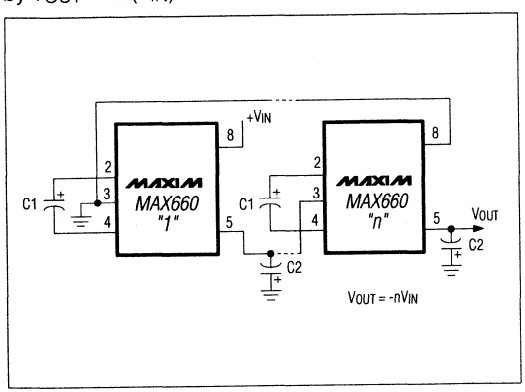


Figure 3. Cascading MAX660s to Increase Output Voltage

Paralleling Devices

Paralleling multiple MAX660s reduces the output resistance. As illustrated in Figure 4, each device requires its own pump capacitor C1, but the reservoir capacitor C2 serves all devices. The value of C2 should be increased by a factor of n, where n is the number of devices. Figure 4 shows the equation for calculating output resistance.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 5. In this circuit, capacitors C1 and C3 perform the pump and reservoir functions respectively for generation of the negative voltage. Capacitors C2 and C4 are respectively pump and reservoir for the multiplied positive voltage. This circuit configuration, however, leads to higher source impedances of the generated supplies. This is due to the finite impedance of the common charge-pump driver.

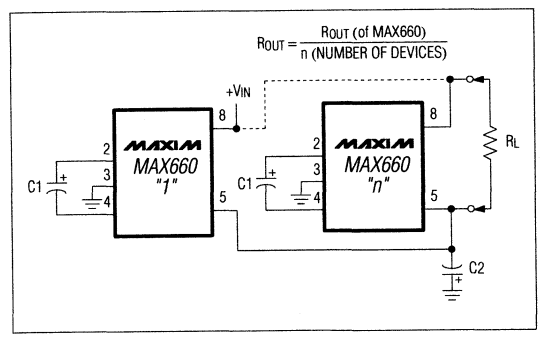


Figure 4. Paralleling MAX660s to Reduce Output Resistance

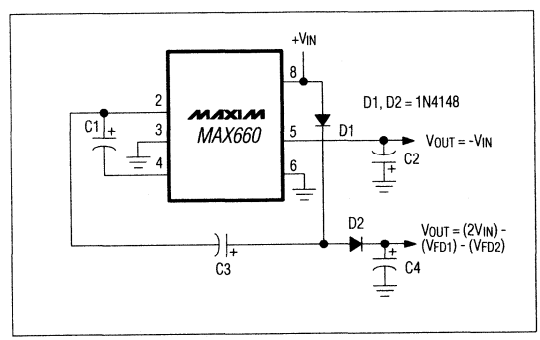


Figure 5. Combined Positive Multiplier and Negative Converter

CMOS Monolithic Voltage Converter

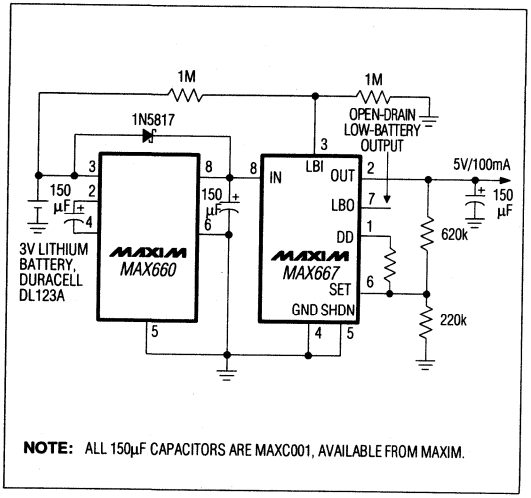
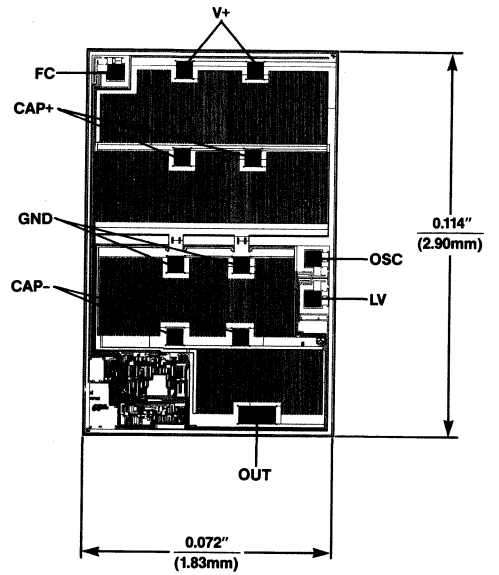


Figure 6. MAX660 generating a +5V regulated output from a 3V Lithium battery. Operates for 16 hours with 40mA load.

Chip Topography



Dual Mode™ 5V/Programmable Micropower Voltage Regulators

General Description

The MAX663/664/666 CMOS voltage regulators have a maximum quiescent current of 12μA. They can be used either as 5 volt, fixed output regulators with no additional components, or can be adjusted from 1.3V to 16V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The MAX66X series, ideally suited for battery powered systems, has an input voltage range of 2 to 16.5V, an output current capability of 40mA, and can operate with low input-output differentials. Other features include current limiting and low power shut down.

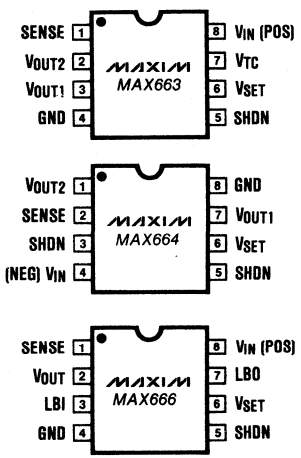
The MAX663 positive regulator and MAX664 negative regulator are both pin and electrically compatible with the ICL7663 and ICL7664 and can plug-in replace these devices, improving performance and eliminating the need for external resistors in 5V applications. The MAX666 has a positive output and includes on-chip low-battery detection circuitry.

Applications

Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition and Telemetry
Radio Controlled Devices
Long-life Battery Powered Systems

Pin Configuration

Top View



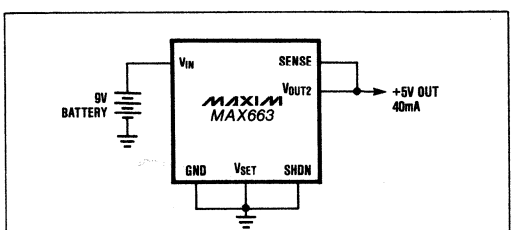
Features

- ♦ **Dual Mode Operation: Fixed +5V or Adjustable from +1.3V to +16V**
- ♦ **Low Power CMOS: 12μA Max Quiescent Current**
- ♦ **40mA Output Current, with Current Limiting**
- ♦ **Pin-Compatible Upgrade of ICL7663 and ICL7664**
- ♦ **+2V to +16.5V Operating Range**
- ♦ **Low Battery Detector (MAX666)**
- ♦ **No Output Over-Shoot on Power Up**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX663C/D	0°C to +70°C	Dice
MAX663CPA	0°C to +70°C	8 Lead Plastic DIP
MAX663CSA	0°C to +70°C	8 Lead Small Outline
MAX663EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX663ESA	-40°C to +85°C	8 Lead Small Outline
MAX663EJA	-40°C to +85°C	8 Lead CERDIP
MAX663MJA	-55°C to +125°C	8 Lead CERDIP
MAX664C/D	0°C to +70°C	Dice
MAX664CPA	0°C to +70°C	8 Lead Plastic DIP
MAX664CSA	0°C to +70°C	8 Lead Small Outline
MAX663EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX664ESA	-40°C to +85°C	8 Lead Small Outline
MAX664EJA	-40°C to +85°C	8 Lead CERDIP
MAX664MJA	-55°C to +125°C	8 Lead CERDIP
MAX666C/D	0°C to +70°C	Dice
MAX666CPA	0°C to +70°C	8 Lead Plastic DIP
MAX666CSA	0°C to +70°C	8 Lead Small Outline
MAX666EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX666ESA	-40°C to +85°C	8 Lead Small Outline
MAX666EJA	-40°C to +85°C	8 Lead CERDIP
MAX666MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



Dual Mode 5V/Programmable Micropower Voltage Regulators

ABSOLUTE MAXIMUM RATINGS

MAX663 and MAX666

Input Supply Voltage ..... +18V
Terminal Voltage
Pins 1,3,5,6, MAX663 — Pin 7, and MAX666 — Pin 2, ... GND -0.3V to V_{IN} +0.3V
MAX663 — Pin 2 ..... GND -0.3V to V_{OUT1} +0.3V
MAX666 — Pin 7 ..... GND -0.3V to +16.5V
Output Source Current
MAX663,666 — Pin 2 (V_{OUT2}, V_{OUT}) 50mA
MAX663 — Pin 3 (V_{OUT1}) 25mA
Output Sink Current, Pin 7 ..... -20mA

MAX664

Input Supply Voltage ..... -18V
Terminal Voltage
Pins 1,3,5,6,7 ..... V_{IN} -0.3V to GND +0.3V
Pin 2 ..... V_{IN} -0.3V to V_{OUT1} +0.3V
Output Sink Current, (Pins 1,7) ..... -25mA

ALL DEVICES

Power Dissipation
Plastic DIP (Derate 8.3mW/°C above +50°C) 625mW
Small Outline (Derate 6mW/°C above +50°C) 450mW
CERDIP (Derate 8mW/°C above +50°C) 800mW
Operating Temperature Range
MAX66XC ..... 0°C to +70°C
MAX66XE ..... -40°C to +85°C
MAX66XM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666

(V_{IN} = +9V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	2.0 2.2		16.5	V
Quiescent Current	I_Q	No Load, V_{IN} = +16.5V T_A = +25°C Over Temperature (C) Over Temperature (E, M)		6	 12 15 20	µA
Output Voltage	V_{OUT}	V_{SET} = GND Over Temperature (C, E) Over Temperature (M)	4.75 4.5	5.0 5.0	5.25 5.5	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	+2V ≤ V_{IN} ≤ +15V, V_{OUT} = V_{REF}		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	MAX663: 1mA ≤ I_{OUT2} ≤ 20mA MAX663: 50µA ≤ I_{OUT1} ≤ 5mA MAX666: 1mA ≤ I_{OUT} ≤ 20mA		3.0 1.0 3.0	7.0 5.0 7.0	Ω
Reference Voltage	V_{SET}	V_{OUT} = V_{SET}	1.27		1.33	V
Reference Tempco.	$\Delta V_{SET}/\Delta T$	Over Temperature		±100		ppm/°C
V_{SET} Internal Threshold for Fixed +5V or Adjustable Output	$V_{F/A}$	V_{SET} < $V_{F/A}$ for +5V Out V_{SET} > $V_{F/A}$ for Adjustable Out		50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		±0.01	±10 ±25	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI = Output Off V_{SHDN} LO = Output On	1.4		 0.3	V
Shutdown Input Current	I_{SHDN}			±0.01	±10	nA
SENSE Input Threshold	V_{OUT} - V_{SENSE}	Current Limit Threshold		0.5		V
SENSE Input Resistance	R_{SENSE}			3		MΩ
Input-Output Saturation Resistance, MAX663 - V_{OUT1}	R_{SAT}	V_{IN} = +2V, I_{OUT} = 1mA V_{IN} = +9V, I_{OUT} = 2mA V_{IN} = +15V, I_{OUT} = 5mA		200 70 50	500 150 150	Ω
Output Current, V_{OUT2} (V_{OUT} on MAX666)	I_{OUT}	+3V ≤ V_{IN} ≤ +16.5V V_{IN} - V_{OUT} = +1.5V	40			mA
Minimum Load Current	$I_{L(MIN)}$	T_A = +25°C Over Temperature (C, E) Over Temperature (M)			1.0 5.0 10.0	µA

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666 (continued)

(V_{IN} = +9V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LBI Input Threshold	V_{LBI}	MAX666	1.21	1.28	1.37	V
LBI Input Current	I_{LBI}	MAX666		±0.01	±10	nA
LBO Output Saturation Resistance	R_{SAT}	MAX666, I_{SAT} = 2mA		35	100	Ω
LBO Output Leakage Current		MAX666, LBI = +1.4V		10		nA
V_{TC} Open-Circuit Voltage (Note 1)	V_{TC}	MAX663		0.9		V
V_{TC} Sink Current (Note 1)	I_{TC}	MAX663		8.0	2.0	mA
V_{TC} Temperature Coefficient (Note 1)		MAX663		+2.5		mV/°C

Note 1: This output (MAX663 only) has a positive temperature coefficient. Using it in conjunction with the input of the regulator at V_{SET}, a negative coefficient results in the output voltage. The V_{TC} pin will not source current.

ELECTRICAL CHARACTERISTICS, MAX664

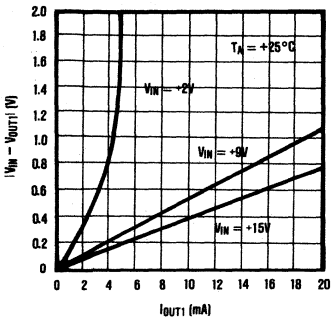
(V_{IN} = -9V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	-2.0 -2.2		-16.5	V
Quiescent Current	I_Q	No Load, V_{IN} = -16.5V T_A = +25°C Over Temperature (C) Over Temperature (E, M)		6	 12 15 20	µA
Output Voltage	V_{OUT}	V_{SET} = GND Over Temperature (C, E) Over Temperature (M)	 -4.75 -4.5	 -5.0 -5.0	 -5.25 -5.5	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$-2V \le V_{IN} \le -15V$, $V_{OUT} = V_{REF}$		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT2} connected to V_{OUT1}, $1mA \le I_{OUT} \le 15mA$		2.0	5.0	Ω
Reference Voltage	V_{SET}	$V_{OUT} = V_{SET}$	-1.27		-1.33	V
Reference Tempco.	$\Delta V_{SET}/\Delta T$	Over Temperature		±100		ppm/°C
V_{SET} Internal Threshold for Fixed -5V or Adjustable Output Operation	$V_{F/A}$	$V_{SET} < V_{F/A}$ for -5V Out, $V_{SET} > V_{F/A}$ for Variable Out		-50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		±0.01	±10 ±25	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI = Output Off V_{SHDN} LO = Output On	-1.4		 -0.3	
Shutdown Input Current	I_{SHDN}			±0.01	±10	nA
SENSE Input Threshold	$V_{OUT} - V_{SENSE}$	Current Limit Threshold		-0.6		V
SENSE Input Resistance	R_{SENSE}			3		MΩ
Input-Output Saturation Resistance	R_{SAT}	V_{OUT2} connected to V_{OUT1} V_{IN} = -2V, I_{OUT} = -1mA V_{IN} = -9V, I_{OUT} = -2mA V_{IN} = -15V, I_{OUT} = -5mA		 150 40 30	 500 80 60	Ω
Minimum Load Current	$I_{L(MIN)}$	T_A = +25°C Over Temperature (C, E) Over Temperature (M)			-1.0 -5.0 -10.0	µA

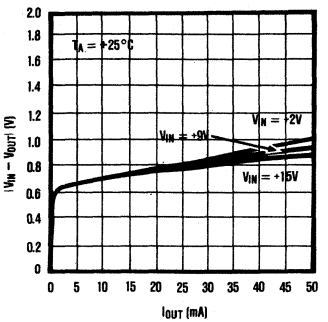
Dual Mode 5V/Programmable Micropower Voltage Regulators

Typical Operating Characteristics

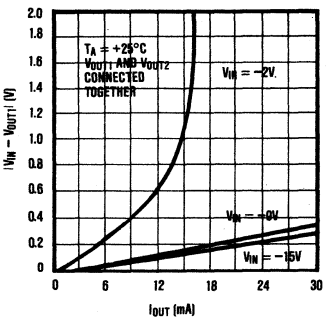
MAX663 V_{OUT1} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



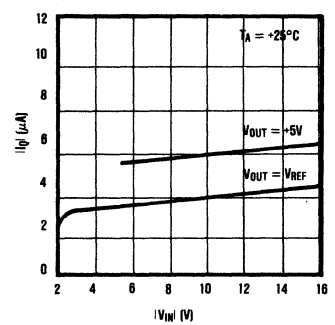
MAX663 V_{OUT2}, MAX666 V_{OUT} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



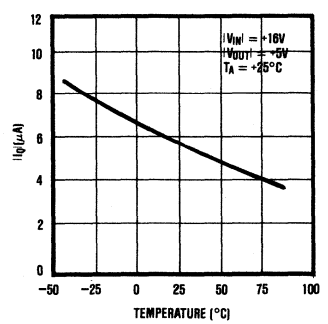
MAX664 INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



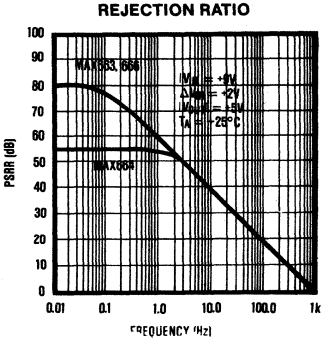
QUIESCENT CURRENT vs. INPUT VOLTAGE



QUIESCENT CURRENT vs. TEMPERATURE



INPUT POWER SUPPLY REJECTION RATIO



Pin Description

NAME	FUNCTION (See text for details)
$V_{OUT(1)(2)}$	Regulator Output(s)
V_{IN}	Regulator Input
SENSE	Current limit sense input
LBI	Low battery detection input
LBO	Low battery detection output
SHUTDOWN	Disables output for minimum power consumption
V_{SET}	Ground this pin for 5V output or Connect to external resistive divider for adjustable output
V_{TC}	Temperature-proportional voltage for negative TC output

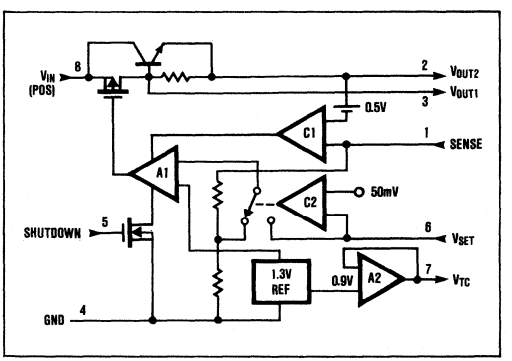


Figure 1. MAX663 Positive Regulator, Block Diagram

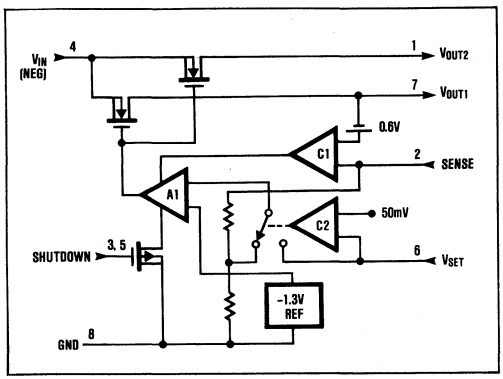


Figure 2. MAX664 Negative Regulator, Block Diagram

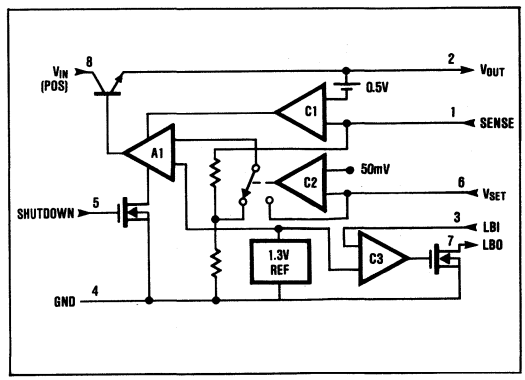


Figure 3. MAX666 Positive Regulator With Low Battery Detector, Block Diagram

Detailed Description

As shown in the block diagrams for each device (Figures 1, 2, and 3), the main elements of the MAX66X family of regulators are a micropower bandgap reference, an error amplifier, and one or two series pass output devices. A P-channel FET and an NPN transistor are used on the MAX663, two N-channel FETs are used in the MAX664 , and one NPN output transistor is used in the MAX666. All regulators also contain two comparators, one for current limiting (C1) and another which selects fixed 5V or adjustable output operation (C2).

The bandgap reference, which is trimmed to 1.30V ±30mV, is internally connected to one input of the error amplifier, A1. The feedback signal from the regulator output is supplied to the A1's other input by either an on-chip voltage divider or by two external resistors. When V_{SET} is grounded the internal divider provides the error amplifier's feedback signal for a fixed 5V output. When V_{SET} is more than 50mV above ground (below ground for the MAX664) the error amplifier's input is switched directly to the V_{SET} pin and external resistors set the output voltage.

Comparator C1 monitors the output current via the SENSE input and shuts down the regulator's output(s) by disabling A1. An external current sense resistor, R_{CL}, sets the limit value. The MAX663 and MAX666 current-limit when the voltage on R_{CL} exceeds 0.5V. The MAX664 current limits at 0.6V.

The MAX663 has an additional amplifier, A2, which provides a temperature-proportional output, V_{TC}. When this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The MAX666 has a third comparator, C3, which compares the LBI input to the internal 1.30V reference. The Low Battery Output, LBO, is an open drain FET connected to Ground. The Low Battery threshold can also be set with a voltage divider at LBI. In addition, all devices also have a SHUTDOWN input which disables the error amplifier and regulator output(s).

Basic Circuit Operation

Figure 4 shows the connections for fixed 5V output positive and negative regulators. The V_{SET} input is grounded and no external resistors are required. Figure 5 shows adjustable output operation with current limiting. The output voltage is set by R1 and R2 and the current limit threshold is set by R_{CL}. V_{OUT} should be connected to SENSE if current limiting is not used and the SHUTDOWN input should be grounded if not used.

Output Voltage Selection

If V_{SET} is not connected to Ground, the output voltage is set by the equation:

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1}, \text{ where } V_{SET} = 1.30V$$

or, to simplify resistor selection:

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30V} - 1\right)$$

Since the input bias current at V_{SET} has a maximum value of 10nA, relatively large values can be used for R1 and R2 with no loss of accuracy. 1MΩ is a typical value for R1. The tolerance on V_{SET} is guaranteed to be less than ±30mV. This allows the output to be preset without trim pots, using only fixed resistors in most cases.

Dual Mode 5V/Programmable Micropower Voltage Regulators

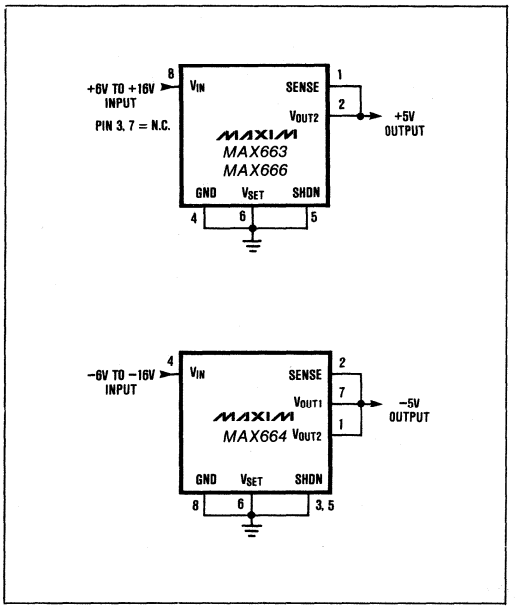


Figure 4. Connections for Fixed 5V Output

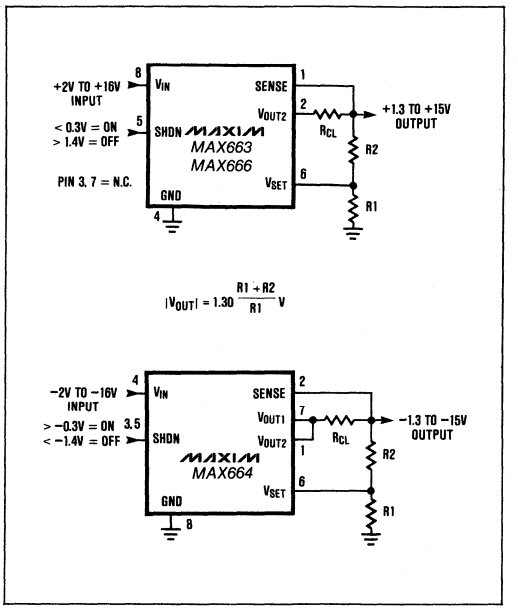


Figure 5. Connections for Adjustable Output

Current Limiting

Internal current limiting is activated on all MAX66X devices when the voltage difference between V_{OUT} and the SENSE input exceeds an internal threshold. The limit value is externally set by R_{CL} using the equation:

$$R_{CL} = \frac{V_{CL}}{I_{CL}}$$

V_{CL} = 0.5V for MAX663 and MAX666
V_{CL} = -0.6V for MAX664
($V_{CL} = V_{OUT} - V_{SENSE}$)

where R_{CL} is the current limit sense resistor and I_{CL} is the maximum current. R_{CL} should be chosen so that neither the 50mA absolute maximum output current specification nor the maximum power dissipation is exceeded.

If current limiting is used, remember that the additional voltage drop across R_{CL} must be considered when determining the regulator's dropout voltage. If current limiting is not used, the SENSE input should be connected to the output(s).

Shutdown Input

The SHUTDOWN input allows the regulator to be turned off with a logic level signal. Since the current drain in shutdown mode is limited to the regulator's quiescent current (12μA Max) this is sometimes desirable in applications where very low power consumption is needed. The SHUTDOWN input should be driven with a CMOS logic level since the input threshold is only 0.3V (-0.3V on the MAX664). In TTL systems, an open-collector driver with a pullup resistor will work with the MAX663/666 if a small collector current is used to keep the output's V_{SAT} below 0.3V. Collector currents as low as 1μA are suitable since the SHUTDOWN pin's input current is less than 10nA. Note that the MAX664's SHUTDOWN input is activated by a negative level. On both positive and negative regulators the SHUTDOWN input should be grounded for normal operation.

Low Battery Detection

The MAX666 contains on-chip circuitry for low battery or low power supply detection. If the voltage at LBI (Low Battery Input, pin 3) falls below the regulator's internal reference (1.30V) then LBO (Low Battery Output, pin 7), an open drain output, goes low. The threshold can be set to any level above the reference voltage by connecting a resistive divider to LBI (Figure 6) based on the equation:

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30V} - 1\right)$$

where V_{BATT} is the desired threshold of the Low Battery Detector and R3 and R4 are the LBI input divider resistors. Since LBI's input current is no more than 10nA, then R3 and R4 can have high

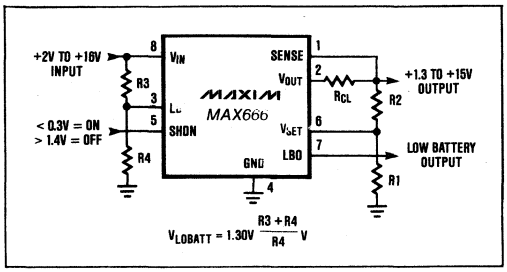


Figure 6. Adjustable Positive Output With Low Battery Detection

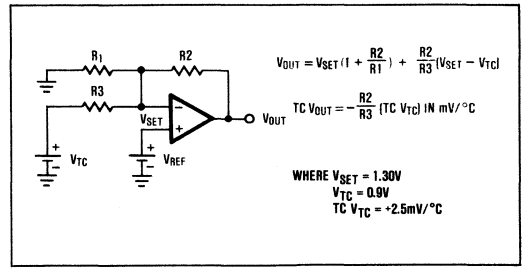


Figure 7. Temperature-Proportional Output Equations, MAX663

values to minimize loading. If, for example, V_{OUT} were 5V, then a 6V low-battery threshold could be set using 10MΩ for R3 and 2.7MΩ for R4. When megohm resistor values are used, special attention should be paid to PC board leakage which can introduce error at the LBI input.

Temperature-Proportional Output

The V_{TC} output (MAX663 only) has a positive temperature coefficient of about +2.5mV/°C. When connected to the summing junction of the error amplifier (V_{SET}) through a resistor, this positive coefficient results in a controllable negative temperature coefficient at the output of the MAX663. At 25°C the voltage at the V_{TC} output is typically 0.9V. Figure 7 shows a simplified diagram of the MAX663 and the equations for setting both the output voltage and the tempco when V_{TC} is used. When not used, V_{TC} should be left unconnected.

Negative output temperature coefficients are most commonly used in multiplexed LCD modules or display systems to compensate for the inherent negative tempco of the LCD threshold. Figure 8 shows a MAX663 generating a temperature compensated V_{DISP} for the Maxim ICM7233 triplexed LCD display driver.

Application Hints

Input-Output (Dropout) Voltage

A regulator's minimum input-output differential, or dropout voltage, determines the lowest usable input voltage. In battery powered systems this will determine the useful end-of-life battery voltage. The MAX663 and MAX666 have a dropout voltage of 1V at full output. This means that as 5V regulators, for example, they will provide a regulated 5V output at 40mA as long as the input voltage is 6V or greater.

For low current applications (I_{OUT} < 5mA) the MAX663 can operate with input-output differentials below 1V when V_{OUT1} is used. The dropout voltage will then depend on the P-channel output FET's saturation resistance multiplied by the load current (see MAX663 Electrical Specifications, R_{SAT}).

The MAX664 (negative output) uses two N-channel FETs as output devices so its dropout voltage is also a function of R_{SAT} times its load current (see Electrical Specifications).

Output Connections

When using V_{OUT1} on the MAX663 for low current, low dropout applications, V_{OUT2} and V_{OUT1} must be connected together since the current limit circuitry is referenced only to V_{OUT2} (Figure 1). V_{OUT2} does not supply load current in this configuration since the base of the NPN output transistor is shorted by the output connection. For high current operation V_{OUT2} should be used alone and V_{OUT1} should be left unconnected. V_{OUT1} is not provided on the MAX666. On the MAX664, V_{OUT1} and V_{OUT2} should always be connected together for proper operation and lowest dropout voltage.

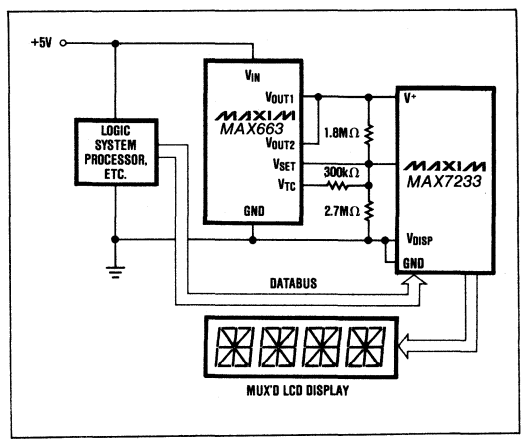


Figure 8. Driving a Multiplexed LCD Display. Consistent operation over more than 40°C temperature span, as opposed to about 10°C with fixed drive voltage, is allowed by negative temperature coefficient drive voltage to the displays. Based on EPSON LDB-728 Display or equivalent.

Dual Mode 5V/Programmable Micropower Voltage Regulators

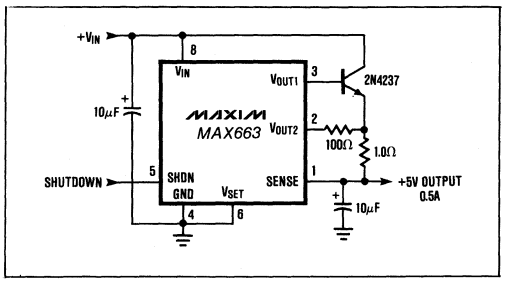


Figure 9. Positive Regulator With Boosted Output, Current Limit, and Low I_Q Shutdown

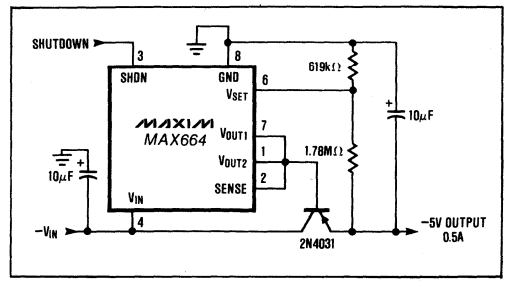


Figure 10. Negative Regulator With Boosted Output and Low I_Q Shutdown

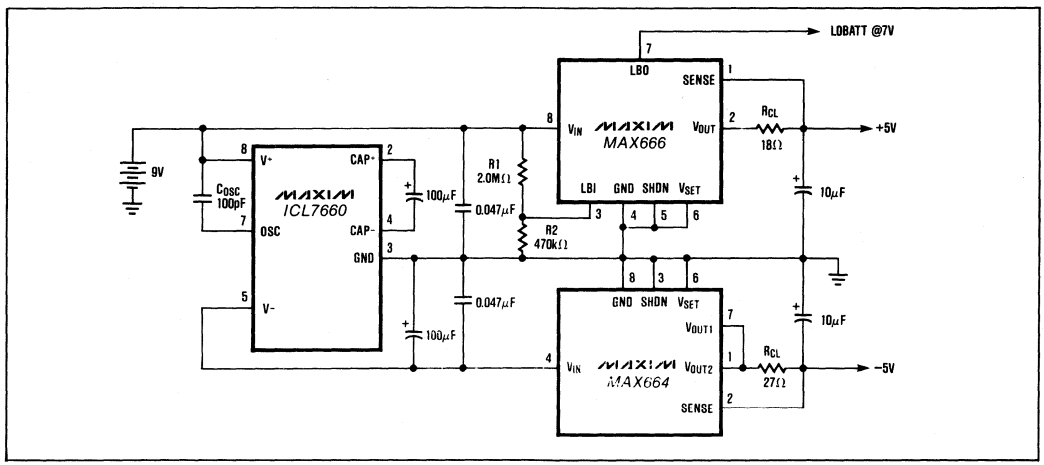


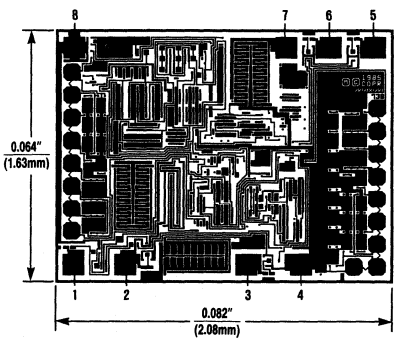
Figure 11. ±5V Power Supply Using One 9V Battery

Bypass Capacitors

The MAX66X series of CMOS regulators is designed primarily for low quiescent current battery powered systems and has limited line and load regulation at frequencies above 10Hz. The high frequency performance is easily improved by adding an output filter capacitor across the load. 10µF is a good typical value. If high frequency performance is not an issue then an output bypass capacitor is not required.

In battery powered systems an input capacitor helps to reduce noise, improve dynamic performance, and reduce the input rate-of-rise at the regulator's input. In extreme cases excessive voltage rate-of-rise at the inputs of CMOS devices can cause SCR latch-up. The low impedance of Ni-Cad and Lead-Acid batteries make this possible when they are switched directly to the regulator input with no current limiting resistance, inductance, or input filtering. The addition of a 0.1µF or greater input capacitor limits the input rate-of-rise to a safe level.

Chip Topography



(See Pin Configurations (front page) for pin functions)

19-3894;Rev. 0; 4/91

+5V/Programmable Low-Dropout Voltage Regulator

General Description

The MAX667 low-dropout, positive, linear voltage regulator supplies up to 250mA of output current. With no load, it has a typical quiescent current of 20µA. At 200mA of output current, the input/output voltage differential is typically 150mV. Other features include a low-voltage detector to indicate power failure as well as early warning and low-dropout detectors to indicate an imminent loss of output-voltage regulation. A shutdown control disables the output and puts the circuit into a low quiescent-current mode.

The MAX667 employs Dual Mode™ operation. One mode uses internally-trimmed feedback resistors to produce +5V. In the second mode, the output may be varied from +1.3V to +16V by connecting two external resistors.

The MAX667 is a pin-compatible upgrade of the MAX666 in most applications where the input voltages are above +3.5V. Choose the MAX667 when high output currents and/or low dropout voltages are desired as well as for improved performance at higher temperatures.

Applications

Battery-Powered Devices

Pagers and Radio Control Receivers

Portable Instruments

Solar-Powered Instruments

Features

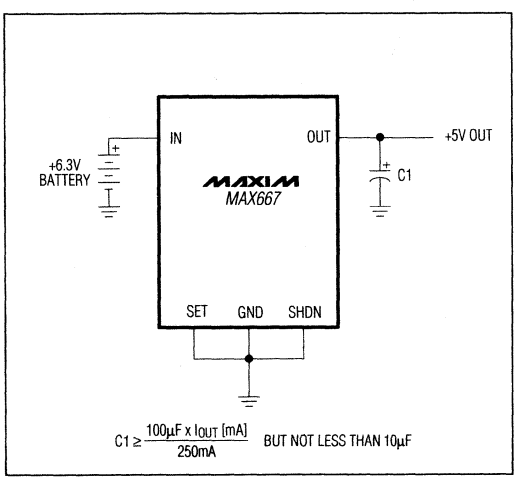
- ♦ **350mV Max Dropout at 200mA**
- ♦ **250mA Output Current**
- ♦ **Normal Mode: 20µA Typ Quiescent Current**
- ♦ **Shutdown Mode: 0.2µA Typ Quiescent Current**
- ♦ **Low-Battery Detector**
- ♦ **Fixed +5V (Min Component Count) or Adjustable Output**
- ♦ **+3.5V to +16.5V Input**
- ♦ **Dropout Detector Output**

Ordering Information

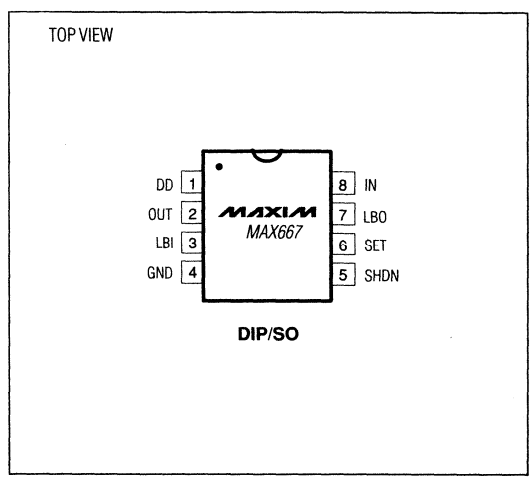
PART	TEMP. RANGE	PIN-PACKAGE
MAX667CPA	0°C to +70°C	8 Plastic DIP
MAX667CSA	0°C to +70°C	8 SO
MAX667C/D	0°C to +70°C	Dice*
MAX667EPA	-40°C to +85°C	8 Plastic DIP
MAX667ESA	-40°C to +85°C	8 SO
MAX667MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



+5V/Programmable Low-Dropout Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... +18V
Output Short Circuited to Ground ..... 1 sec
LBO Output Sink Current 50mA
LBO Output Voltage ..... GND to V_{OUT}
SHDN Input Voltage ..... -0.3V to (V_{IN} + 0.3)V
Input Voltages LBI, SET ..... -0.3V to (V_{IN} - 1.0)V
Continuous Total Power Dissipation
  Plastic DIP (derate 8.3mW/°C above +50°C) 625mW
  SO (derate 6mW/°C above +50°C) 450mW
  CERDIP (derate 8mW/°C above +50°C) 800mW

Operating Temperature Ranges:
  MAX667CPA/CSA/CD ..... 0°C to +70°C
  MAX667EPA/ESA ..... -40°C to +85°C
  MAX667MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

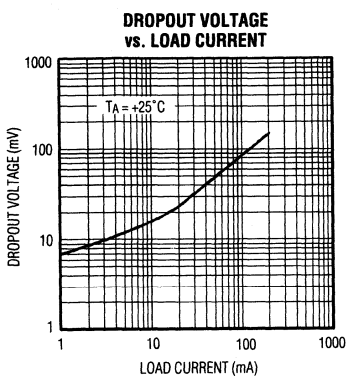
(GND = 0V, V_{IN} = +9V, V_{OUT} = +5V, unless otherwise specified.)

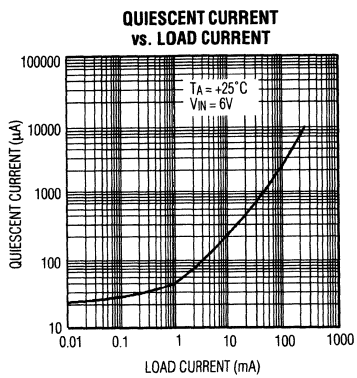
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN} to T_{MAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage	V_{IN}					3.5		16.5	V
Output Voltage	V_{OUT}	V_{SET} = 0V, V_{IN} = 6V, I_{OUT} = 10mA		5		4.8		5.2	V
Maximum Output Current	I_{OUT}	V_{IN} = 6V, 4.5V < V_{OUT} < 5.5V	250			250			mA
Quiescent Current	I_{GND}	V_{SHDN} = 2V		0.2	1			2	µA
		V_{SHDN} = 0V, V_{SET} = 0V							
		I_{OUT} = 0µA		20	25			35	µA
		I_{OUT} = 100µA		20	30			50	µA
		I_{OUT} = 200mA		5	15			20	mA
Dropout Voltage (Note 1)		I_{OUT} = 100µA		5	60			75	mV
		I_{OUT} = 200mA		150	250			350	mV
Load Regulation		I_{OUT} = 10-200mA		50	100			250	mV
Line Regulation		V_{IN} = 6V to 10V, I_{OUT} = 10mA		5	10			15	mV
SET Reference Voltage	V_{SET}			1.255		1.23		1.28	V
SET Input Leakage Current	I_{SET}	V_{SET} = 1.5V		0.01	±10			±1000	nA
Output Leakage Current	I_{OUT}	V_{SHDN} = 2V		0.1				1	µA
Short-Circuit Current	I_{OUT}	(Note 2)			400			450	mA
Low-Battery Detector Reference Voltage	V_{LBI}			1.255		1.215		1.295	V
Low-Battery Detector Input Leakage Current	I_{LBI}	V_{LBI} = 1.5V		0.01	±10			±1000	nA
Low-Battery Detector Output Voltage	V_{LBO}	V_{IN} = 9V, V_{LBI} = 2V, I_{LBO} = 10mA			0.25			0.4	V
Shutdown Threshold	V_{SHDN}		1.5			1.5			V
Shutdown Input Leakage Current	I_{SHDN}	V_{SHDN} = 0 to V_{IN}		0.01	±10			±1000	nA
Dropout Detector Output Voltage	V_{DD}	V_{SET} = 0V, V_{SHDN} = 0V, R_{DD} = 100kΩ, V_{IN} = 7V, I_{OUT} = 10mA						0.25	V
		V_{SET} = 0V, V_{SHDN} = 0V, R_{DD} = 100kΩ, V_{IN} = 4.5V, I_{OUT} = 10mA					4		V

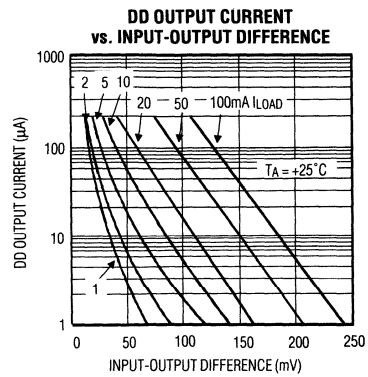
Note 1: Dropout Voltage is V_{IN}-V_{OUT} when V_{OUT} falls to 0.1V below its value at V_{IN} = V_{OUT} +2V.
Note 2: Short-Circuit Current is pulse tested to maintain junction temperature. Short-circuit duration is limited by package dissipation.

+5V/Programmable Low-Dropout Voltage Regulator

Typical Operating Characteristics







Pin Description

PIN	NAME	FUNCTION
1	DD	Dropout Detector Output - the collector of a PNP pass transistor. Normally an open circuit, it sources current as dropout is reached.
2	OUT	Regulated Output Voltage. OUT falls to 0V when SHDN is above 1.5V. SET determines output voltage when SET is above 50mV; otherwise, it is 5V. OUT must be connected to an output filter capacitor.
3	LBI	Low-Battery Detector. A CMOS input to an internal 1.255V comparator whose output is the LBO pin.
4	GND	Ground.
5	SHDN	Shutdown Input. Connect to GND for normal operation (output active). Pull above 1.5V to disable OUT, LBO, and DD and to reduce quiescent current to <1µA.
6	SET	(Output) Voltage Set, CMOS Input. Connect to GND for 5V output. For other voltages, connect external resistive divider from OUT.
7	LBO	Low-Battery Output. An open-drain N-channel transistor that sinks current to GND when LBI is less than 1.255V.
8	IN	Positive Input Voltage (unregulated)

Detailed Description

Figure 1 shows a micropower bandgap reference, an error amplifier, a PNP pass transistor, and two comparators as the main elements of the MAX667. One comparator, C1, selects the fixed 5V or adjustable operation with an external voltage divider. The other comparator, C2, is a low-battery detector.

The bandgap reference, which is trimmed to 1.255V, connects internally to one input of the error amplifier, A1. The feedback signal from the regulator output supplies the other input of A1 from either an on-chip voltage divider or two external resistors. When SET is grounded, the internal divider provides the error amplifier feedback signal for a fixed 5V output. When SET is more than 50mV above ground, the error amplifier's input switches directly to SET while an external resistor divider from OUT determines the output voltage.

A second comparator, C2, compares the LBI input to the internal reference voltage. LBO is an open-drain FET connected to GND. The low-battery threshold can also be set with a voltage divider at LBI. In addition, the MAX667 has a shutdown input (SHDN) that disables the load and the device while reducing quiescent current when it is pulled high.

+5V Output

Figure 2 shows the connection for fixed 5V output. The SET input is grounded, and no external resistors are required. Figure 3 shows adjustable output operation. R1 and R2 set the output voltage. SHDN should be grounded if not used.

+5V/Programmable Low-Dropout Voltage Regulator

Output-Voltage Selection

If SET is connected to a resistive voltage divider (Figure 3), the output voltage is set by the equation:

$V_{OUT} = V_{SET} \times (R1 + R2)/R1$,
where $V_{SET} = 1.255V$

To simplify resistor selection:

$R2 = R1 \times (V_{OUT}/V_{SET} - 1)$

Since the input bias current at SET has maximum value of 10nA, relatively large values can be used for R1and R2 with no loss of accuracy. 1MΩ is a typical value for R1. The V_{SET} tolerance is less than ±25mV. This allows the output to be preset without trim pots, using only fixed resistors in most cases. However, when resistor values >1MΩ are used, pay special attention to printed circuit board leakage that can introduce error at the SET input.

Shutdown (Standby) Mode

SHDN puts the device into standby mode to conserve power. When this pin is held low, the IC operates normally. If it is driven above 1.5V, the chip shuts down. Quiescent current of the MAX667 is then reduced to <1µA, and OUT turns off.

Note that the voltage for SHDN must never be more than 0.3V higher than V_{IN}.

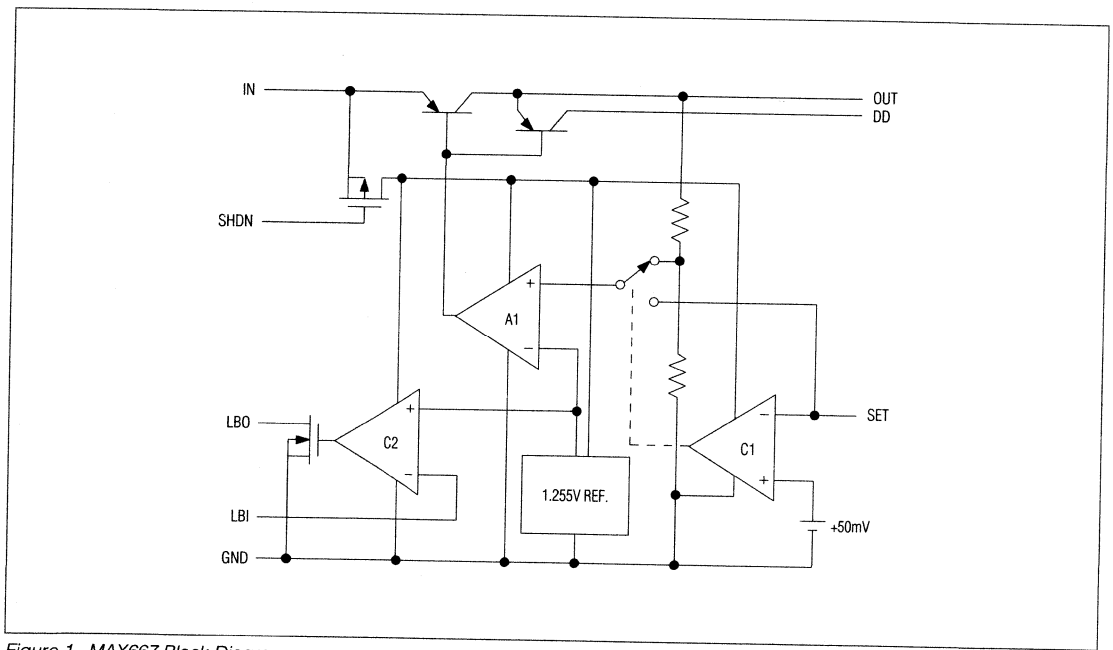


Figure 1. MAX667 Block Diagram

+5V/Programmable Low-Dropout Voltage Regulator

Low-Battery Function

The MAX667 contains circuitry for low-battery detection. If the voltage at LBI falls below the regulator's internal reference (1.255V), LBO, an open-drain output, sinks current to GND. The threshold can be set to any level above the reference voltage by connecting a resistive divider to LBI based on the equation:

$$R3 = R4 \times (V_{BATT}/V_{LBI} - 1)$$

where V_{BATT} is the desired threshold of the low-battery detector, and R3 and R4 are the LBI input divider resistors.

Since LBI input current is no more than 10nA, high values for R3 and R4 minimize loading. If V_{OUT} is 5V, a 5.5V low-battery threshold can be set using 8.2MΩ for R3 and 2.4MΩ for R4. When resistor values >1MΩ are used, pay special attention to PC board leakage that can introduce error at the LBI input.

When the voltage at LBI is below the internal threshold, LBO sinks current to GND. A pull-up resistor of 10kΩ or more connected to OUT can be used with this pin when driving CMOS circuits. Any pull-up resistor connected to LBO should NOT be returned to a voltage source greater than V_{OUT}. When LBI is above the threshold or the MAX667 is in SHDN mode, the LBO output is off.

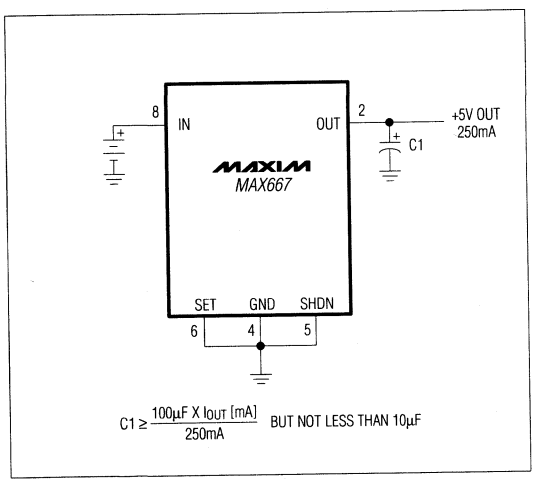


Figure 2. Fixed +5V Regulator

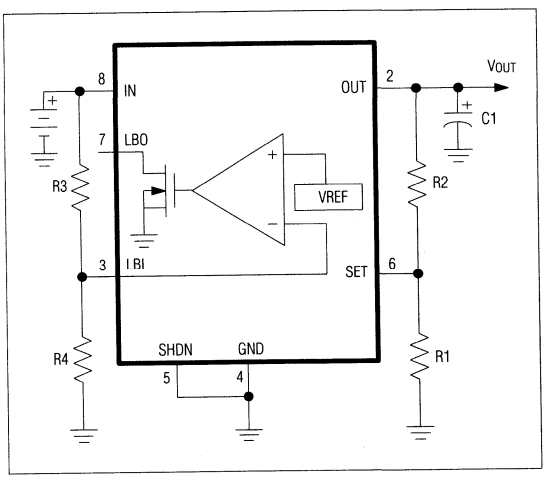


Figure 3. Adjustable Output and Low-Battery Detector

4

+5V/Programmable Low-Dropout Voltage Regulator

Dropout Detector

The minimum input-output differential, or dropout voltage, determines the regulator's lowest usable input voltage. In battery-operated systems, this determines the useful end-of-life battery voltage. The MAX667 features very low dropout voltage (*Electrical Characteristics*). In addition, the MAX667 has a dropout detector output, DD, that changes as the dropout voltage approaches its limit. DD is an open collector of a PNP transistor. The dropout voltage and the dropout detector both depend on the output current and temperature. When the input voltage is more than 300mV above the output voltage, the dropout detector will not conduct. As the differential decreases below 300mV, the DD source current increases abruptly. This current signals a warning that regulation is about to be lost.

Connecting a resistor (typically 100kΩ) from DD to ground develops a voltage that can be monitored by analog circuits or changed to digital levels by a comparator. LBI may be used for this purpose.

Applications Information

Output Capacitor

As with all PNP output regulators, an output capacitor (C1, Figure 2) is required to maintain stability. The value ranges from 10µF to 100µF, depending on load current. Most electrolytic types perform well; however, those with high equivalent series resistance (ESR) may not maintain stability, particularly with high load current and at low temperatures where capacitor ESR tends to rise. It is recommended that capacitors with ESR below 0.2Ω at +25°C be used. The 150µF MAXC001, available from Maxim, meets this requirement.

Battery Drain

The MAX667 uses a PNP output transistor. When the input voltage falls below the desired output voltage, the PNP transistor is turned on fully as regulation is lost. Even with a load current of a few microamperes, the base current will be driven above 5mA. Figure 6 shows how this base current may be significant. Consequently, a mostly discharged battery can be further discharged at end-of-life.

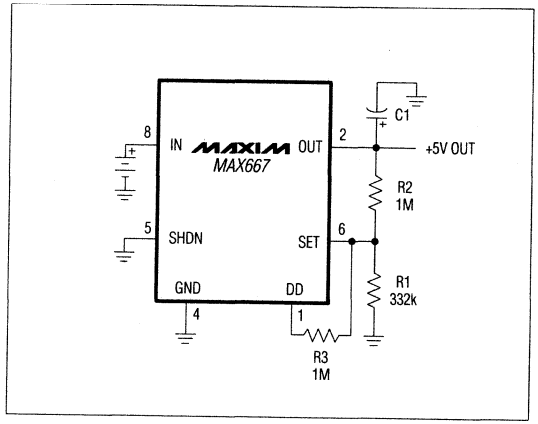


Figure 5. Connection for Minimum Quiescent Current Near Dropout

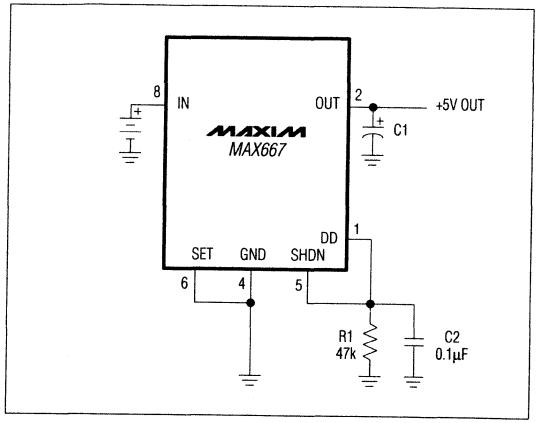


Figure 4. Quiescent-Current Reduction Below Dropout

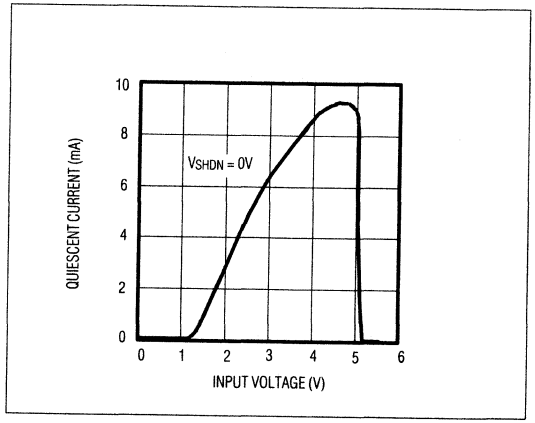


Figure 6. Quiescent Current Below Dropout for Circuit of Figure 2

+5V/Programmable Low-Dropout Voltage Regulator

Figure 4 shows how this condition can be modified by connecting DD to SHDN with a 47kΩ resistor, R1, paralleled with a 0.1µF capacitor to GND. This modification reduces the no-load quiescent current to approximately 160µA when dropout is reached (Figure 7), but increases the dropout voltage by about 0.1V. The output voltage drops to approximately 3V once DD begins to activate SHDN, but it does not fall to zero because SHDN is only partially activated.

A second alternate connection (Figure 5) further reduces quiescent current near the dropout voltage, compared to the circuit in Figure 4. The output must be set with external resistors (R1, R2), so DD lowers the output voltage as the input voltage falls by sourcing current into SET via R3. Quiescent current remains low for inputs down to 3.5V, and peaks before falling to 0 at low input voltages. Although the current peak is higher than with the connection in Figure 4, this may be more useful because the quiescent current peaks at an input voltage well below the useful range of most batteries (Figure 7). Also, as IN falls below 5V, OUT tracks IN minus the dropout voltage. This connection still allows separate use of the SHDN input.

Power Dissipation

The MAX667 can regulate currents as high as 250mA and withstand input-output differential voltages as high as 15.2V, but not simultaneously. The maximum power dissipation is dependent on the package and the temperature (see *Absolute Maximum Ratings*). Figure 8 shows the maximum output current at various input-output differential voltages for the plastic DIP and SO packages. The MAX667 can withstand short-circuit loads up to 1 second.

Operation From AC Sources

The MAX667 is a micropower CMOS regulator intended principally for battery operation. When operating from AC sources, consider power-supply ripple rejection. The MAX667's error amplifier produces very low gain bandwidth, and the input power-supply rejection ratio (PSRR) is therefore not specified. Since the output must be connected to a 10µF or larger filter capacitor, the capacitor characteristics dominate the PSRR. Large values of input and output capacitors reduce the ripple.

In addition, both DD and LBI/LBO can trigger on the lowest DC component of the ripple, particularly at high load currents. In the case of the low-battery detector, the ripple can be effectively filtered out by placing a capacitor to ground in parallel with the LBI input pin. The high resistance values that can be used for the voltage divider allow relatively small capacitance values to form an effective lowpass filter at 120Hz. When power is first applied, however, this filter tends to hold LBO low longer than normal.

Transient Considerations

The low operating current and gain-bandwidth product of the internal reference and amplifier result in limited rejection of fast-step input changes. Negative-going steps, which occur in under 100µs, may turn off the output for several milliseconds. An input filter (nominally 10µF) is recommended if input changes greater than 1V and faster than 100µs (other than turn-on or turn-off) are anticipated.

The MAX667 is not abnormally affected by step changes in its load. Figure 9 shows output response to a 4V/100µs input change (no input filter), while Figure 10 shows output response to a 10mA/100mA instantaneous load step.

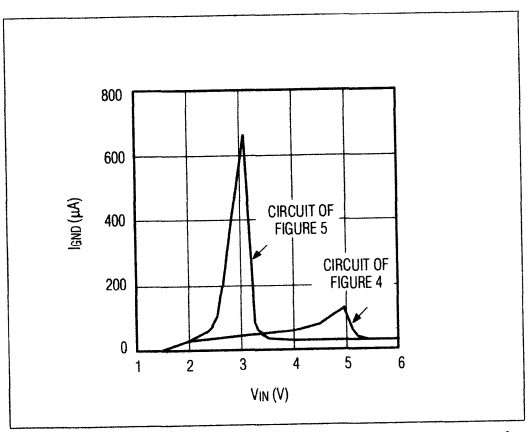


Figure 7. Quiescent Current Below Dropout with Connections of Figures 4 and 5

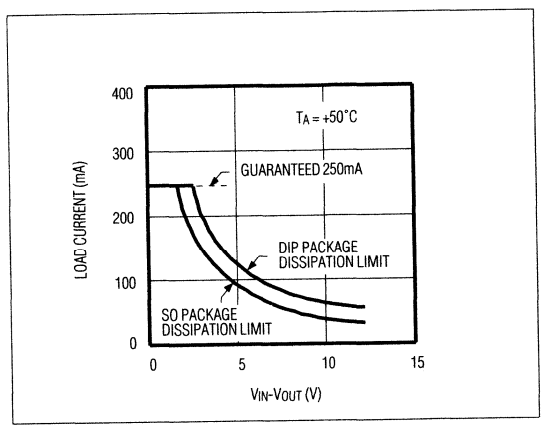


Figure 8. MAX667 Load Current vs. Input-Output Differential Voltage

+5V/Programmable Low-Dropout Voltage Regulator

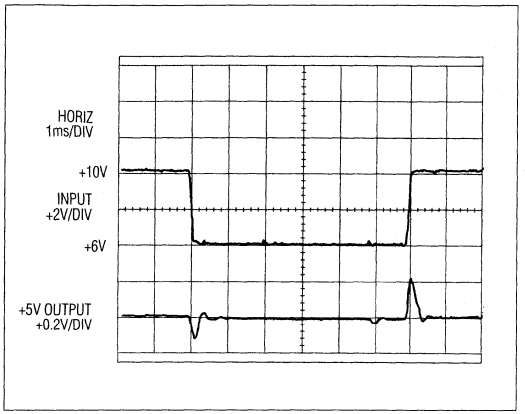


Figure 9. Output Response to +4V/100µs Input Step

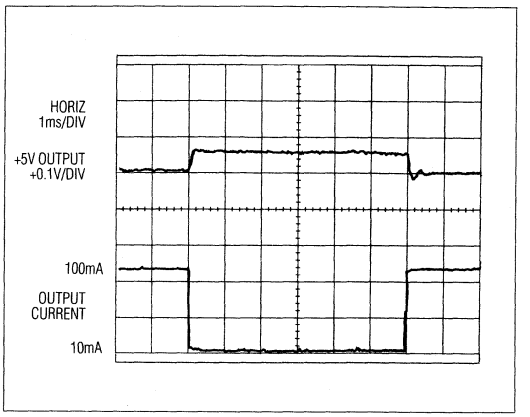
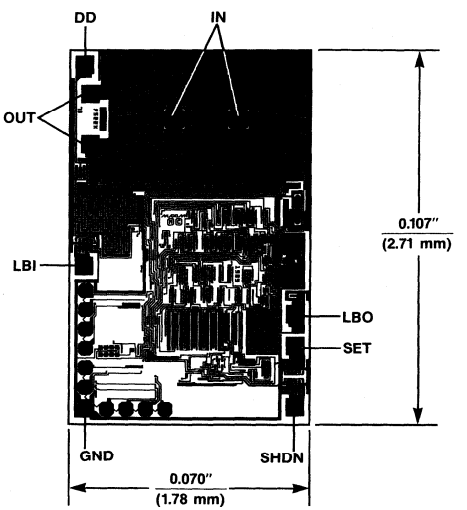


Figure 10. Output Response to +10V/100mA Load Step

Chip Topography



Note: Substrate must be left unconnected.
Transistor Count: 65

+5V to ±10V Voltage Converters

General Description

The MAX680/MAX681 are monolithic CMOS dual charge pump voltage converters that provide ±10V outputs from a +5V input voltage. The MAX680/MAX681 provide both a positive stepup charge pump to develop +10V from +5V input and an inverting charge pump to generate the -10V output. Both parts have an on-chip 8kHz oscillator. The MAX681 has the capacitors internal to the package, and the MAX680 requires 4 external capacitors to produce both positive and negative voltages from a single supply.

The output source impedances are typically 150Ω, providing useful output currents up to 10mA. The low quiescent current and high efficiency make this device suitable for a variety of applications that need both positive and negative voltages generated from a single supply.

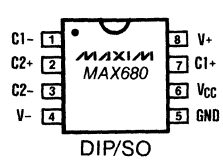
Applications

The MAX680/MAX681 can be used wherever a single positive supply is available and positive and negative voltages are required. Common applications include the generation of ±6V from a 3V battery and generation of ±10V from the standard +5V logic supply for use with analog circuitry. Typical applications include:

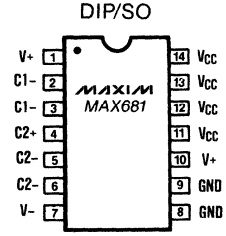
±10V from +5V Logic Supply
±6V from a 3V Lithium Cell
Handheld Instruments
Battery Operated Equipment
Data Acquisition Systems
Panel Meters
Operational Amplifier Power Supplies

Pin Configurations

Top View



DIP/SO



DIP

Features

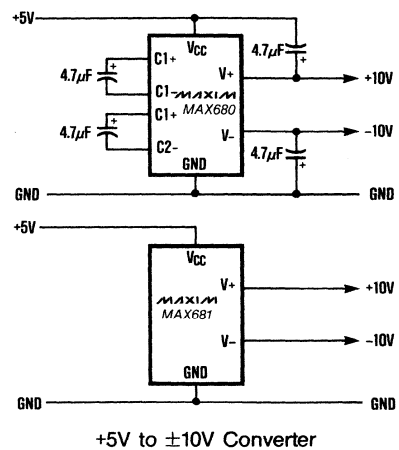
- ♦ 95% Voltage Conversion Efficiency
- ♦ 85% Power Conversion Efficiency
- ♦ Wide Voltage Range: +2.0V to +6.0V
- ♦ Only 4 External Capacitors Required — MAX680
- ♦ No Capacitors Required — MAX681
- ♦ 500μA Supply Current
- ♦ Monolithic CMOS Design

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX680CPA	0°C to +70°C	8 Plastic DIP
MAX680CSA	0°C to +70°C	8 Narrow SO
MAX680C/D	0°C to +70°C	Dice
MAX680EPA	-40°C to +85°C	8 Plastic DIP
MAX680ESA	-40°C to +85°C	8 Narrow SO
MAX680EJA	-40°C to +85°C	8 CERDIP
MAX680MJA	-55°C to +125°C	8 CERDIP
MAX681CPD	0°C to +70°C	14 Plastic DIP
MAX681BCPD	0°C to +70°C	14 Plastic DIP
MAX681EPD	-40°C to +85°C	14 Plastic DIP

4

Typical Operating Circuit



+5V to ±10V Converter
MAX681 ONLY 4 PINS REQUIRED

+5V to ±10V Voltage Converters

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +6.2V
V+ ..... +12V
V- ..... -12V
V- Short-Circuit Duration ..... Continuous
V+ Current 75mA
V_{CC} dV/dT 1V/μs

Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

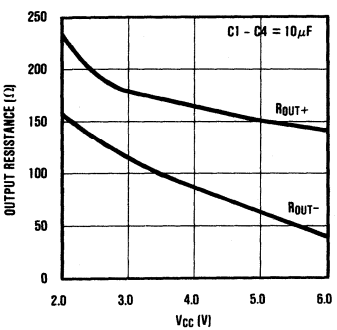
ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = +25°C, test circuit Figure 1, unless otherwise noted.)

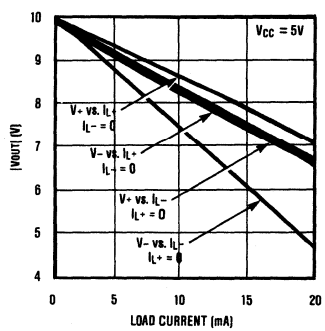
PARAMETER	CONDITIONS	MAX680/MAX681			MAX681B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	V_{CC} = 3V, T_A = +25°C, R_L = ∞		0.5	1		0.5	1	mA
	V_{CC} = 5V, T_A = +25°C, R_L = ∞		1	2		1	2	
	V_{CC} = 5V, 0°C ≤ T_A ≤ +70°C, R_L = ∞			2.5			2.5	
	V_{CC} = 5V, -40°C ≤ T_A ≤ +85°C, R_L = ∞			3				
	V_{CC} = 5V, -55°C ≤ T_A ≤ +125°C, R_L = ∞			3				
Supply Voltage Range	MIN. ≤ T_A ≤ MAX., R_L = 10kΩ	2.0	1.5 to 6.0	6.0	2.0	1.5 to 6.0	6.0	V
Positive Charge Pump Output Source Resistance	I_L+ = 10mA, I_L- = 0mA, V_{CC} = 5V, T_A = +25°C		150	250		150	250	Ω
	I_L+ = 5mA, I_L- = 0mA, V_{CC} = 2.8V, T_A = +25°C		180	300		180	300	
	I_L+ = 10mA, I_L- = 0mA, V_{CC} = 5V							
	0°C ≤ T_A ≤ +70°C			325		380	600	
	-40°C ≤ T_A ≤ +85°C			350				
	-55°C ≤ T_A ≤ +125°C			400				
Negative Charge Pump Output Source Resistance	I_L- = 10mA, I_L+ = 0mA, V+ = 10V, T_A = +25°C		90	150		175	300	
	I_L- = 5mA, I_L+ = 0mA, V+ = 5.6V, T_A = +25°C		110	175		180	325	
	I_L- = 10mA, I_L+ = 0mA, V+ = 10V							
	0°C ≤ T_A ≤ +70°C			200		300	500	
	-40°C ≤ T_A ≤ +85°C			200				
	-55°C ≤ T_A ≤ +125°C			250				
Oscillator Frequency		4	8		4	8		kHz
Power Efficiency	R_L = 10kΩ		85			85		%
Voltage Conversion Efficiency	V+, R_L = ∞	95	99		95	99		
	V-, R_L = ∞	90	97		90	97		

Typical Operating Characteristics

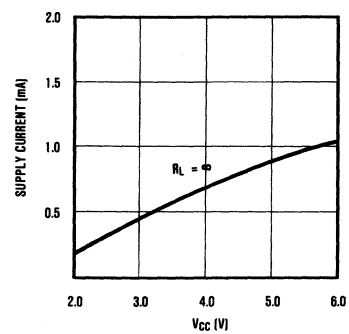
OUTPUT RESISTANCE vs. V_{CC}



V_{OUT} vs. LOAD CURRENT

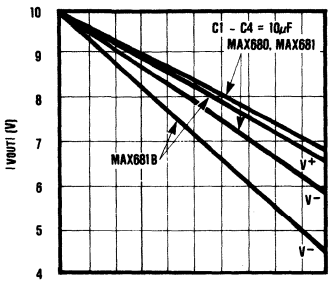


SUPPLY CURRENT vs. V_{CC}

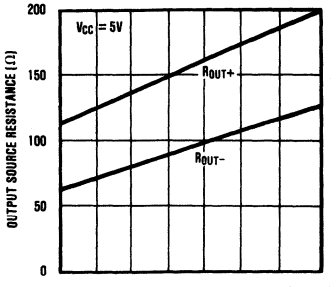


Typical Operating Characteristics

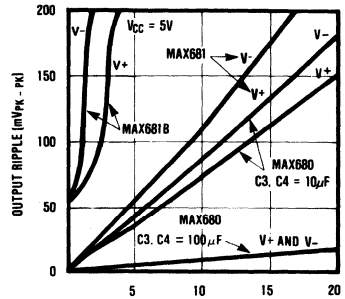
OUTPUT VOLTAGE vs. OUTPUT CURRENT FROM V+ TO V-



OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



OUTPUT RIPPLE vs. OUTPUT CURRENT



Detailed Description

All circuitry needed to implement a dual charge pump is contained in the MAX681. Only four capacitors are needed on the MAX680. These may be inexpensive electrolytic capacitors with values in the range of 1µF to 100µF. The MAX681B contains 1µF capacitor and exhibits somewhat more output ripple than the MAX681. See Typical Operating Characteristics.

Figure 2A illustrates the idealized operation of the positive voltage converter. The on-chip oscillator generates a 50% duty cycle clock signal. During the first half of the cycle, switches S2 and S4 are open, switches S1 and S3 are closed, and the capacitor C1 is charged to the input voltage V_{CC}. During the second half cycle, switches S1 and S3 are open, S2 and S4 are closed, and the capacitor C1 is translated upward by V_{CC} volts. Assuming ideal switches and no load on C3, charge is transferred onto C3 from C1 such that the voltage on C3 will be $2V_{CC}$, generating the positive supply.

Figure 2B illustrates the negative converter. The switches of the negative converter are out of phase from the positive converter. During the second half of the clock cycle, S6 and S8 are open, S5 and S7 are closed, thus charging C2 from V+ (pumped up to

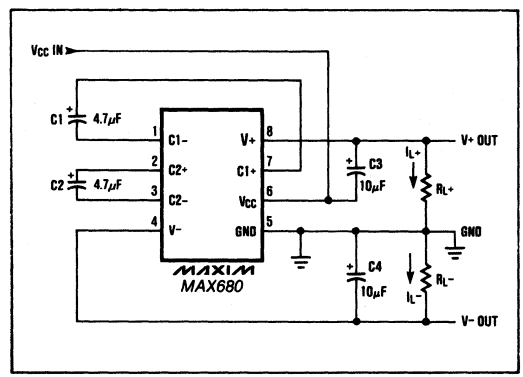


Figure 1. Test Circuit

$2V_{CC}$ by the positive charge pump) to GND. In the first half of the clock cycle, S5 and S7 are open, S6 and S8 are closed, and the charge on C2 is transferred to C4, generating the negative supply. The eight switches are CMOS power MOSFETs. Switches S1, S2, S4 and S5 are P-channel devices while switches S3, S6, S7, and S8 are N-channel devices.

+5V to ±10V Voltage Converters

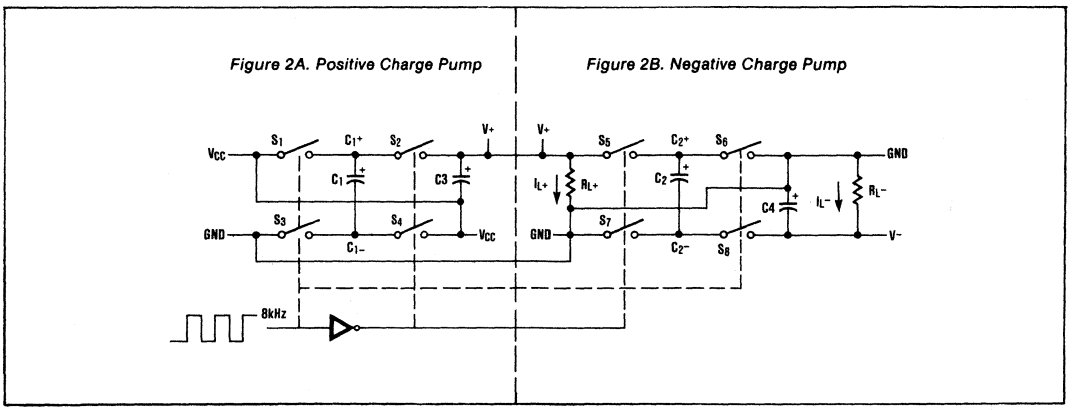


Figure 2. Idealized Voltage Quadrupler

Efficiency Considerations

Theoretically a charge pump voltage multiplier can approach 100% efficiency under the following conditions:

- The charge pump switches have virtually no offset and extremely low on resistance
- Minimal power is consumed by the drive circuitry
- The impedances of the reservoir and pump capacitors are negligible

For the MAX680/681, the energy loss per clock cycle is the sum of the energy loss in the positive and negative converters as below:

$$Loss_{TOT} = Loss_{POS} + Loss_{NEG}$$

$$= \tfrac{1}{2} C_1[(V+)^2 - 2(V+)(V_{CC})] + \tfrac{1}{2} C_2[(V+)^2 - (V-)^2]$$

There will be a substantial voltage difference between (V+ - V_{CC}) and V_{CC} for the positive pump and between V+ and V- if the impedances of the pump capacitors C1 and C2 are high with respect to their respective output loads.

Larger values of reservoir capacitors C3 and C4 will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency.

Maximum Operating Limits

The MAX680/MAX681 have on-chip zener diodes that clamp V_{CC} to approximately 6.2V, V+ to 12.4V, and V- to -12.4V. Never exceed the maximum supply voltage or excessive current may be shunted by these diodes, potentially damaging the chip. The MAX680/MAX681 will operate over the entire operating temperature range with an input voltage of 2V to 6V.

Applications

Positive and Negative Converter

The most common application of the MAX680/MAX681 is as a dual charge pump voltage converter which provides positive and negative outputs of two times a positive input voltage. For applications where PC board space is at a premium, the MAX681 with its capacitors internal to the package offers the smallest footprint. The simple circuit of Figure 3 performs the same function using the MAX680 and external capacitors, C1 and C3 for the positive pump and C2 and C4 for the negative pump. In most applications, all four capacitors are low-cost 10μF or 22μF polarized electrolytics. When using the MAX680 for low current applications, 1μF may be used for C1 and C2 charge pump capacitors, and 4.7μF for the reservoir capacitors C3 and C4. Capacitors C1 and C3 must be rated at 6V or greater, and capacitors C2 and C4 must be rated at 12V or greater.

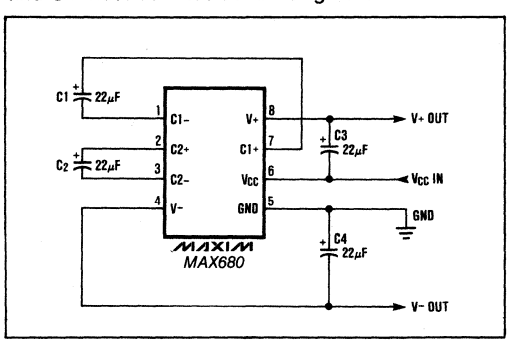


Figure 3. Positive and Negative Converter

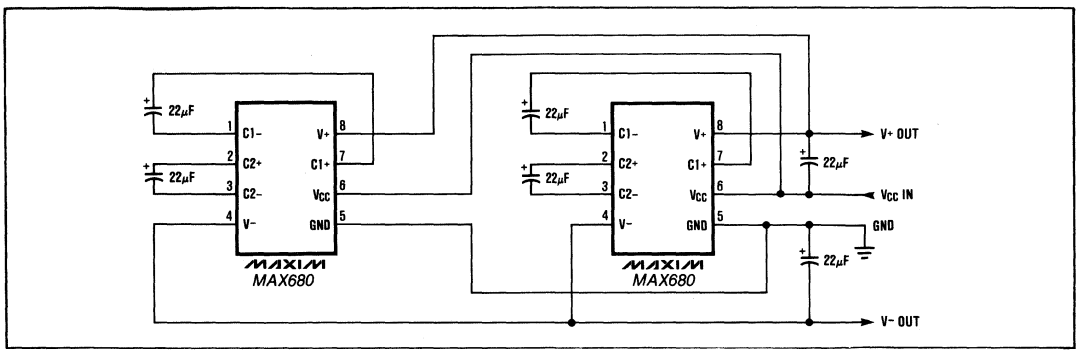


Figure 4. Paralleling MAX680s For Lower Source Resistance

The MAX680/MAX681 are NOT voltage regulators: the output source resistance of either charge pump is approximately 150Ω at room temperature with V_{CC} at 5V. This means that with an input V_{CC} of 5V, under light load V+ will approach +10V and V- will be at -10V, but BOTH V+ and V- will droop towards GND as the current drawn from EITHER V+ or V- increases since the negative converter draws its power from the output of the positive converter. To predict the output voltages, treat the chips as two separate converters and analyze them separately. First, the droop of the negative supply (V_{DROP}-) equals the current drawn from V- - (I_L-) times the source resistance of the negative converter (RS-):

$$V_{DROP^-} = I_{L^-} \times RS-$$

Likewise, the droop of the positive supply (V_{DROP}+) equals the current drawn from the positive supply (I_L+) times the source resistance of the positive converter (RS+), except that the current drawn from the positive supply is the sum of the current drawn by the load on the positive supply (I_L+) plus the current drawn by the negative converter (I_L-):

$$(V_{DROP^+}) = I_{L^+} \times RS+ = (I_{L^+} + I_{L^-}) \times RS+$$

The positive output voltage will be:

$$V+ = 2V_{CC} - V_{DROP^+}$$

The negative output voltage will be:

$$V- = (V+ - V_{DROP}) = -(2V_{CC} - V_{DROP^+} - V_{DROP^-})$$

The positive and negative charge pumps are tested and specified separately to provide the separate values of output source resistance for use in the above formulas. When the positive charge pump is tested, the negative charge pump is unloaded. When the negative charge pump is tested, the positive supply V+ is from an external source, isolating the negative charge pump.

The ripple voltage on either output can be calculated by noting that the current drawn from the output is supplied by the reservoir capacitor alone during one half cycle of the clock. This results in a ripple of:

$$V_{RIPPLE} = \frac{1}{2} IOUT\ (1/f_{PUMP})\ (1/CR)$$

For the nominal f_{PUMP} of 8kHz with 10µF reservoir capacitors, the ripple will be 30mV with I_{OUT} at 5mA. Remember that in most applications, the I_{OUT} of the positive charge pump is the load current PLUS the current taken by the negative charge pump.

Paralleling Devices

Paralleling multiple MAX680/MAX681s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure 4, each MAX680 requires separate pump capacitors C1 and C2, but all can share a single set of reservoir capacitors.

±5V Regulated Supplies From A Single 3V Battery

Figure 5 shows a complete ±5V power supply using one 3V battery. The MAX680/MAX681 provide +6V at V+, which is regulated to +5V by the MAX666, and -6V, which is regulated to -5V by the MAX664. The

+5V to ±10V Voltage Converters

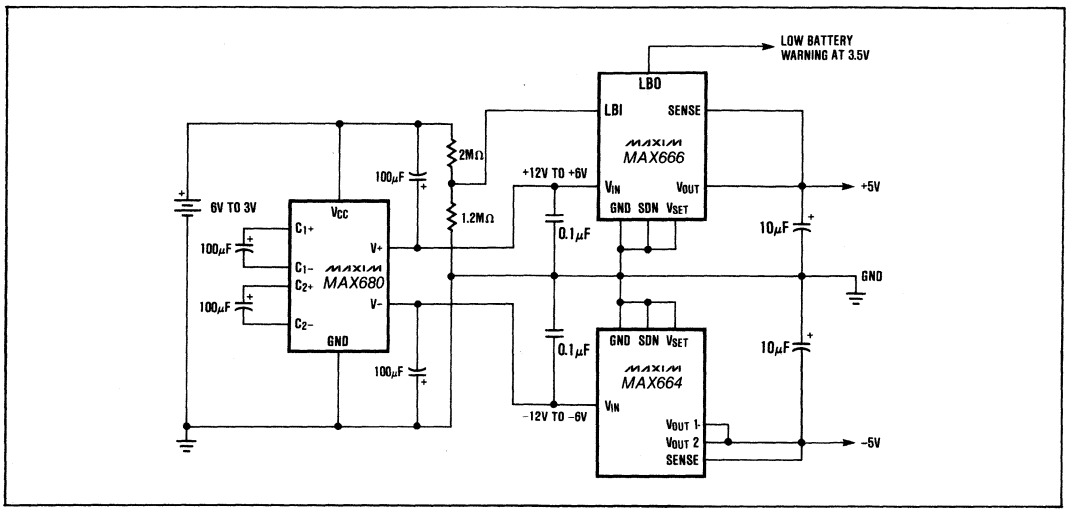
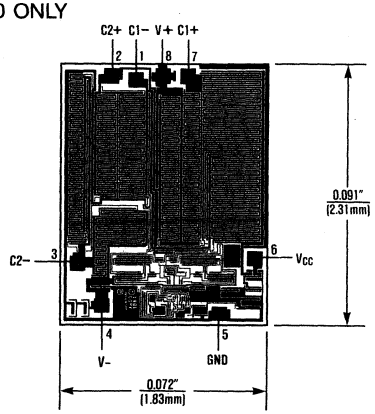


Figure 5. Regulated +5V and -5V From a Single Battery

MAX666 and MAX664 are pre-trimmed at wafer sort and require no external setting resistors, minimizing parts count. The combined quiescent current of the MAX680/MAX681, MAX663, and MAX664 is less than 500µA, while the output current capability is 5mA. The input to the MAX680/MAX681 can vary from 3V to 6V without affecting regulation appreciably. With higher input voltage, more current can be drawn from the outputs of the MAX680/MAX681. With 5V at V_{CC}, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150Ω source resistance for both converters, with (I_L+ + I_L-) = 20mA, the positive charge pump will droop 3V, providing +7V for the negative charge pump. The negative charge pump will droop another 1.5V due to its 10mA load, leaving -5.5V at V- sufficient to maintain regulation for the MAX664 at this current.

Chip Topography

MAX680 ONLY



Note: Connect substrate to V+.

MAXIM

Battery-Powered Supply Systems

General Description

The MAX714/715/716 battery-powered supply systems combine multiple regulated voltage outputs with microprocessor supervisory functions that are optimized for battery-powered supplies. High-level integration and low-power CMOS simplify high-efficiency power-supply design in portable and battery-operated instruments.

The MAX716 combines circuitry for four low-dropout linear regulators, three DC-DC switching regulators, and power-supervisory functions on a single IC. All but one regulator output is logic controlled so that loads may be shut down to extend battery life. Linear-regulator outputs are pre-trimmed to +5V and operate with only 0.1V input-output differential. In addition, three DC-DC switching regulators generate a fixed negative output (-5V, -12V, or -15V), a software-adjustable negative output (-5V to -26V) to power LCD displays, and a positive boosted output voltage. Other functions include backup-battery switchover, low-voltage warning, and power-fail reset.

The MAX716 is supplied in 28-pin plastic DIP and wide SO packages. The MAX715, in 24-pin narrow plastic DIP and CERDIP packages, eliminates one linear-regulator output. The MAX714, in 16-pin packages, includes two linear regulators and the LCD display DC-DC converter.

Applications

Portable Computers

Battery-Powered, Microprocessor-Based Systems

Handheld Instruments, Terminals

Bar-Code Readers

Remote Data-Acquisition Systems

Features

- ♦ **Four Logic-Controlled +5V Regulators**
- ♦ **Three Switching Regulators**
- ♦ **20µA Quiescent Current in Standby Mode**
- ♦ **100mV Dropout on Linear Regulators**
- ♦ **CMOS RAM Battery-Switchover Circuit**
- ♦ **Microprocessor Reset and Interrupt Outputs**
- ♦ **Hardware-On Signal**

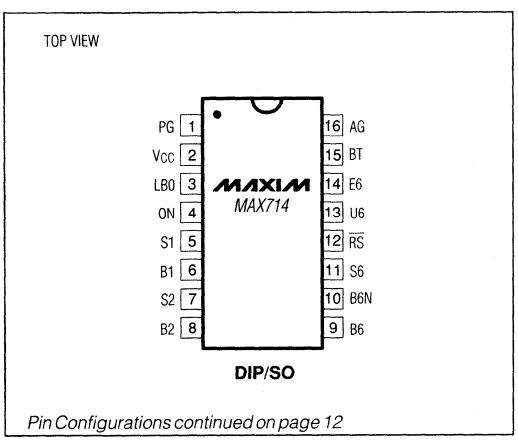
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX714CPE	0°C to +70°C	16 Plastic DIP
MAX714CWE	0°C to +70°C	16 Wide SO
MAX714C/D	0°C to +70°C	Dice*
MAX714EPE	-40°C to +85°C	16 Plastic DIP
MAX714EWE	-40°C to +85°C	16 Wide SO
MAX714MJE	-55°C to +125°C	16 CERDIP
MAX715CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX715CWG	0°C to +70°C	24 Wide SO
MAX715C/D	0°C to +70°C	Dice*
MAX715ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX715EWG	-40°C to +85°C	24 Wide SO
MAX715MRG	-55°C to +125°C	24 Narrow CERDIP

Ordering Information continued on page 12.

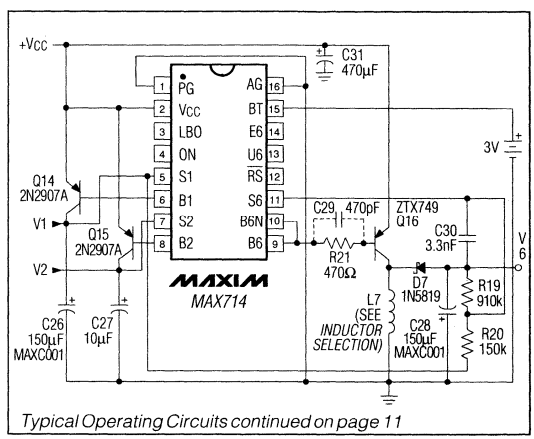
**Contact factory for dice specifications.*

Pin Configurations



Pin Configurations continued on page 12

Typical Operating Circuits



Typical Operating Circuits continued on page 11

MAXIM

+5V Step-Down Current-Mode PWM Regulators

General Description

The MAX730/MAX738 are +5V-output CMOS, step-down, DC-DC switch-mode regulators. The MAX738 accepts inputs from +6.0V to +16.0V and delivers up to 750mA of DC current. The MAX730 delivers up to 300mA and accepts inputs from +5.2V to +11.0V. Typical efficiencies exceed 90%. The MAX730/MAX738 require only a single inductor value to function over their entire range so no inductor design is necessary. Accuracy is guaranteed over temperature, line, and load variations. The MAX730/MAX738 use a current-mode pulse-width modulation (PWM) controller to provide precise output regulation and low subharmonic noise. Typical quiescent supply current is 1.7mA. The MAX730/MAX738 oscillator frequencies are 170kHz and 160kHz, respectively, allowing easy filtering of ripple and noise and use of small external components.

The MAX730/MAX738 feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection.

For adjustable versions of these devices refer to the MAX750 and MAX758 data sheet(s). For lower-power step-down applications refer to the MAX638. Inductors and capacitors to complement the MAX730/MAX738 can be ordered directly from Maxim in production quantities (see *Ordering Information*). Refer to the MAXL001 and MAXC001 data sheets for detailed product specifications.

Applications

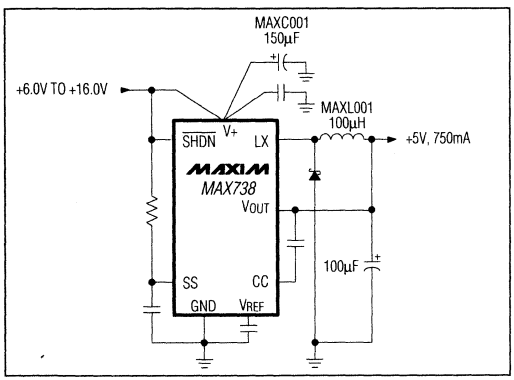
Portable Instruments

Distributed Power Systems

Computer Peripherals

DC-DC Converter Module Replacements

Typical Operating Circuit



Features

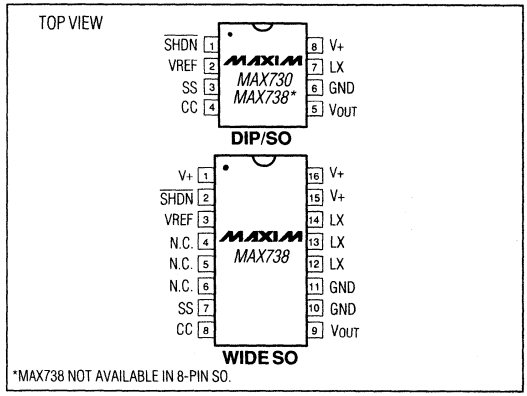
- ♦ **Load Currents to 750mA with No External MOSFET – (300mA for the MAX730)**
- ♦ **165kHz High Frequency Current-Mode PWM**
- ♦ **Small Inductor & No Component Design Required**
- ♦ **90% Typical Efficiencies**
- ♦ **Overcurrent, Soft-Start, and Shutdown Protection**
- ♦ **8-Pin DIP, 16-Pin Wide SO (MAX738)**
- ♦ **8-Pin DIP, 8-Pin SO (MAX730)**
- ♦ **Regulates Down to 5.2V Input (6.0V for the MAX738)**
- ♦ **Shutdown Pin**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX730CPA	0°C to +70°C	8 Plastic DIP
MAX730CSA	0°C to +70°C	8 SO
MAX730C/D	0°C to +70°C	Dice*
MAX730EPA	-40°C to +85°C	8 Plastic DIP
MAX730ESA	-40°C to +85°C	8 SO
MAX730MJA	-55°C to +125°C	8 CERDIP
MAX738CPA	0°C to +70°C	8 Plastic DIP
MAX738CWE	0°C to +70°C	16 Wide SO
MAX738C/D	0°C to +70°C	Dice*
MAX738EPA	-40°C to +85°C	8 Plastic DIP
MAX738EWE	-40°C to +85°C	16 Wide SO
MAX738MJA	-55°C to +125°C	8 CERDIP
MAXC001	-25°C to +105°C	150µH ±20%
MAXL001	-55°C to +105°C	100µH ±15%

** Contact factory for dice specifications.*

Pin Configurations



*MAX738 NOT AVAILABLE IN 8-PIN SO.

ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

-5V Inverting Current-Mode PWM Regulators

General Description

The MAX735/MAX739 are fixed-output, -5V inverting switch-mode regulators with internal power MOSFETs. The MAX739's guaranteed output current is 250mA when powered from a +4.5V input, and exceeds 300mA when powered from +12V. Quiescent supply current is typically 2mA, and falls to less than 1µA in shutdown mode. These power-conserving features, in highly efficient small packages, make the MAX735 and MAX739 ideal for a broad range of on-card and portable equipment applications.

A high-performance, current-mode PWM control scheme coupled with a simple buck-boost switching topology provides tight output voltage regulation and low noise. The oscillator is factory-trimmed to a fixed frequency of 165kHz. The MAX735/MAX739 are production tested in the actual application circuit, guaranteeing output accuracy at ±5% over all line, load, and temperature conditions.

Part	Input Voltage	Load Capability
MAX735	+4V to +11V	200mA
MAX739	+4V to +16V	300mA

For adjustable output versions, refer to the MAX755 and MAX759 data sheets.

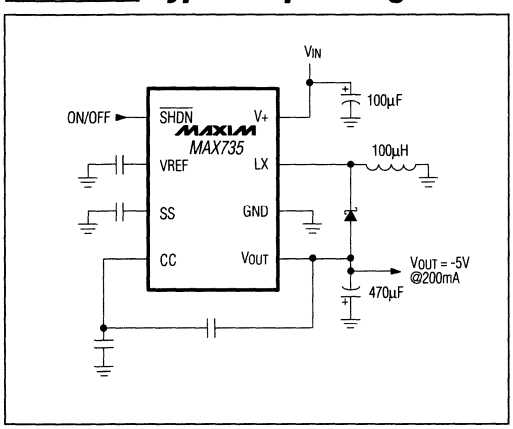
Applications

Board-Level DC-DC Conversion

Battery-Powered Equipment

Computer Peripherals

Typical Operating Circuit



Features

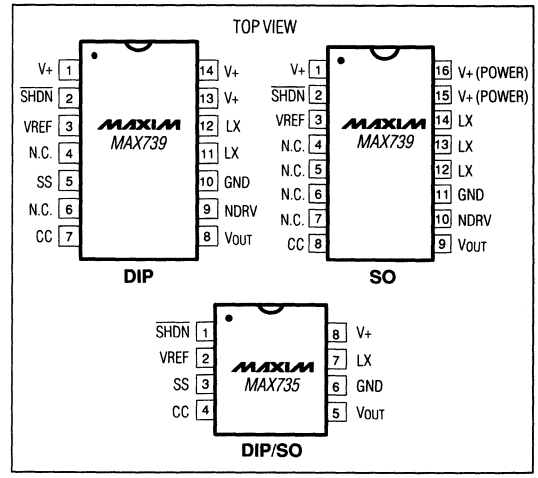
- ♦ **Converts Positive Voltages to Negative**
- ♦ **Guaranteed 300mA at -5V (MAX739)**
- ♦ **80% Typical Efficiency**
- ♦ **2mA Typical Quiescent Current**
- ♦ **1µA Shutdown Mode**
- ♦ **Current-Mode PWM–Low Noise and Ripple**
- ♦ **Undervoltage Lockout and Soft-Start**
- ♦ **Cycle-by-Cycle Current Limiting**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX735CPA	0°C to +70°C	8 Plastic DIP
MAX735CSA	0°C to +70°C	8 SO
MAX735C/D	0°C to +70°C	Dice*
MAX735EPA	-40°C to +85°C	8 Plastic DIP
MAX735ESA	-40°C to +85°C	8 SO
MAX735MJA	-55°C to +125°C	8 CERDIP
MAX739CPD	0°C to +70°C	14 Plastic DIP
MAX739CWE	0°C to +70°C	16 Wide SO
MAX739C/D	0°C to +70°C	Dice*
MAX739EPD	-40°C to +85°C	14 Plastic DIP
MAX739EWE	-40°C to +85°C	16 Wide SO
MAX739MJD	-55°C to +125°C	14 CERDIP

** Contact factory for dice specifications.*

Pin Configurations



MAXIM

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

General Description

The MAX742 DC-DC converter is a controller for dual-output power supplies in the 3W to 60W range. Relying on simple two-terminal inductors rather than transformers, the MAX742 regulates both outputs independently to within ±4% over all conditions of line voltage, temperature, and load current.

The MAX742 has high efficiency (up to 92%) over a wide range of output loading. Two independent PWM current-mode feedback loops provide tight regulation and operation free from subharmonic noise. The MAX742 can operate at 100kHz or 200kHz, so it can be used with small and lightweight external components. Also, ripple and noise are easy to filter. The MAX742 provides a regulated output for inputs ranging from 4.2V to 10V (and higher with additional components).

External power MOSFETs driven directly from the MAX742 are protected by cycle-by-cycle overcurrent sensing. The MAX742 also features undervoltage lockout, thermal shutdown, and programmable soft-start.

Inductors and capacitors to complement the MAX742 can be ordered directly from Maxim in production quantities (see Ordering Information). Refer to the MAXL001 and MAXC001 data sheets for detailed product specifications. If 3W of load power or less is needed, refer to the MAX743 data sheet for a device with internal power MOSFETS.

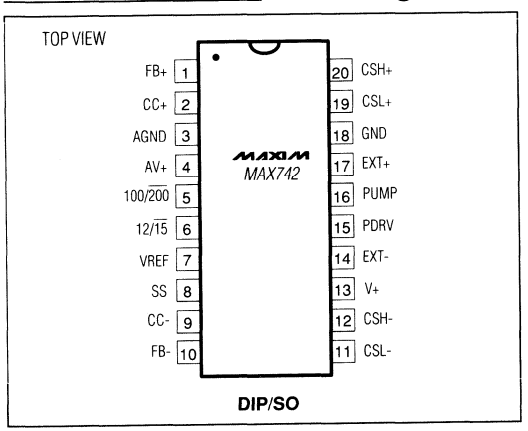
Applications

DC-DC Converter Module Replacement

Distributed Power Systems

Computer Peripherals

Pin Configuration



Features

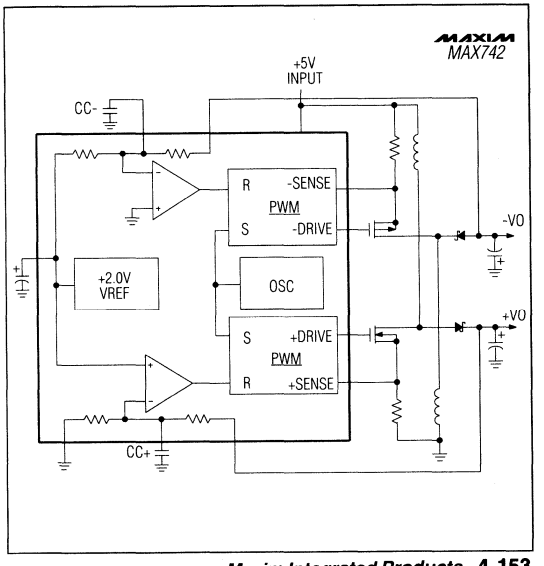
- ♦ **Specs Guaranteed for In-Circuit Performance**
- ♦ **Load Currents to ±2A**
- ♦ **4.2V to 10V Input-Voltage Range**
- ♦ **Switches From ±15V to ±12V Under Logic Control**
- ♦ **±4% Output Tolerance Max Over Temp, Line, and Load**
- ♦ **90% Typ Efficiency**
- ♦ **Low-Noise, Current-Mode Feedback**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **Undervoltage Lock-Out and Soft-Start**
- ♦ **100kHz or 200kHz Operation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX742CPP	0°C to +70°C	20 Plastic DIP
MAX742CWP	0°C to +70°C	20 Wide SO
MAX742C/D	0°C to +70°C	Dice
MAX742EPP	-40°C to +85°C	20 Plastic DIP
MAX742EWP	-40°C to +85°C	20 Wide SO
MAX742MJP	-55°C to +125°C	20 CERDIP

Ordering Information continued on page 15.

Simplified Block Diagram



Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

ABSOLUTE MAXIMUM RATINGS

V+, AV+ to AGND, GND ..... -0.3V to +12V
PDRV to V+ ..... +0.3V to -17V
FB+, FB- to GND ..... ±25V
Input Voltage to GND
(CC+, CC-, CSH+, CSL+, CSH-, CSL-, SS, 100/$\overline{200}$K, 12/$\overline{15}$V) ..... -0.3V to (V+)+0.3V
Output Voltage to GND
(EXT+, PUMP) ..... -0.3V to (V+)+0.3V
EXT- to PDRV ..... -0.3V to (V+)+0.3V

Power Dissipation (any Package) to +75°C 500mW
Derates Above +75°C by ..... 10mw/°C
Operating Temperature Ranges
MAX742C_ _ ..... 0°C to +70°C
MAX742E_ _ ..... -40°C to +85°C
MAX742MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, +4.5V < V+ < +5.5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage, ±15V Mode (Notes 1, 2)		0 < I_L < 100mA, 12/$\overline{15}$V = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}	 14.55 14.40		 15.45 15.60	V
Output Voltage, ±12V Mode (Notes 1, 2)		0 < I_L < 125mA, 12/$\overline{15}$V = V+ T_A = 25°C T_A = T_{MIN} to T_{MAX}	 11.64 11.52		 12.36 12.48	V

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V+ = +5V, 100/$\overline{200}$K = 12/$\overline{15}$ = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation		V+ = 4.5V to 5.5V, PDRV from PUMP			0.01	0.05	%/%
Load Regulation (Note 2)		I_{LOAD} = 0 to 100mA			30	100	mV
No-Load Supply Current		No EXT+, EXT- or PUMP Load, FB+ = FB- = open circuit	V+ = +5V V+ = +10V			3 10	mA
Undervoltage Lock-Out	UVLO			3.8		4.2	V
Undervoltage Lock-Out Hysteresis					0.2		V
Reference Output Voltage					2.0		V
Oscillator Frequency	fOSC	100/$\overline{200}$K = 0V 100/$\overline{200}$K = V+		170 75	200 100	230 125	kHz
PUMP Frequency					fOSC/2		
Duty-Cycle Limit (Note 3)		EXT+ or EXT-		85	90		%
Positive Current-Limit Threshold (CSH+ to CSL+)		CSL+ = 0V, FB+ = open circuit		150	225	300	mV
Negative Current-Limit Threshold (CSH- to CSL-)		CSH- = V+, FB- = open circuit		150	225	300	mV

ELECTRICAL CHARACTERISTICS (Continued)

(Circuit of Figure 2, V+ = +5V, 100/200K = 12/15V = 0V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage High	V_{OH}	EXT+, EXT-, IL = 1mA, V+ = 4.5V, PDRV = -3V		4.3			V
Output Voltage Low	V_{OL}	EXT+, EXT-, IL = -1mA, V+ = 4.5V, PDRV = -3V				-2.8	V
Output Sink Current		V+ = 4.5V, PDRV = -3V, T_A = 25°C	EXT+ = 4.5V EXT- = 4.5V	100 200	200 350		mA
Output Source Current		V+ = 4.5V, PDRV = -3V, T_A = 25°C	EXT+ = 0V EXT- = -3V		-200 -350	-100 -200	mA
Output Rise/Fall Time		EXT+, C_{LOAD} = 2nF EXT-, C_{LOAD} = 4nF, PDRV = -3V			70 100		ns
PUMP Output Voltage (Note 4)		V+ = 4.5V, IL = -5mA, T_A = 25°C				-3	V
Compensation Pin Impedance		CC+, CC-			10		kΩ
Thermal-Shutdown Threshold					190		°C
Soft-Start Source Current		SS = 0V		3		7	µA
Soft-Start Sink Current		V+ = 3.8V, SS = 2V			-2	-0.5	mA

Note 1: Devices are 100% tested to these limits under 0mA to 100mA and to 125mA load conditions using automatic test equipment. The ability to drive loads up to 1A is guaranteed by the current-limit threshold, output swing, and the output current source/sink tests. See Figures 2 and 3.

Note 2: Actual load capability of the circuit of Figure 2 is ±200mA in ±15V mode and ±250mA in ±12V mode. Load regulation is tested at lower limits due to test equipment limitations.

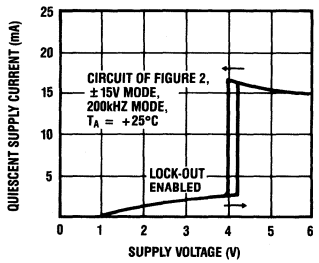
Note 3: Guaranteed by design.

Note 4: Measured at Point A, circuit of Figure 2, with PDRV disconnected.

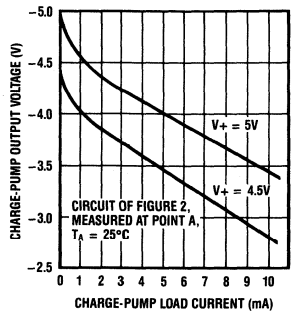
Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

Typical Operating Characteristics

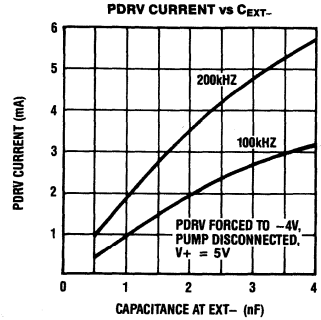
UNDERVOLTAGE LOCK-OUT HYSTERESIS



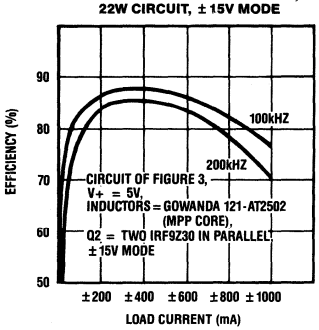
CHARGE-PUMP LOAD REGULATION



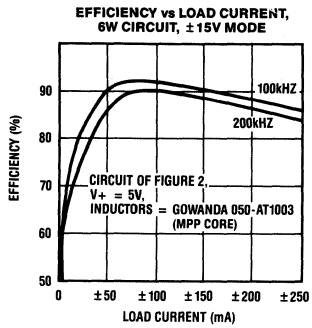
PDRV CURRENT vs C_{EXT-}



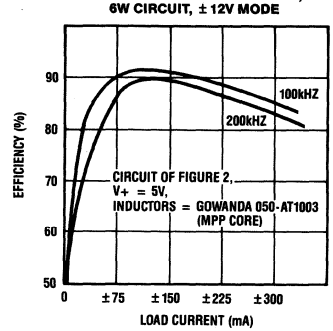
EFFICIENCY vs LOAD CURRENT, 22W CIRCUIT, ±15V MODE



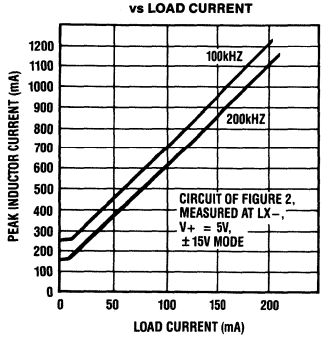
EFFICIENCY vs LOAD CURRENT, 6W CIRCUIT, ±15V MODE



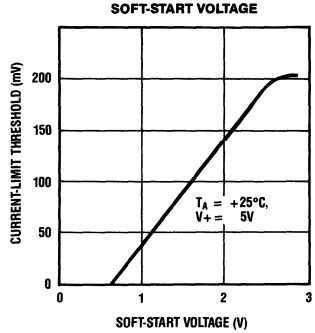
EFFICIENCY vs LOAD CURRENT, 6W CIRCUIT, ±12V MODE



PEAK INDUCTOR CURRENT vs LOAD CURRENT



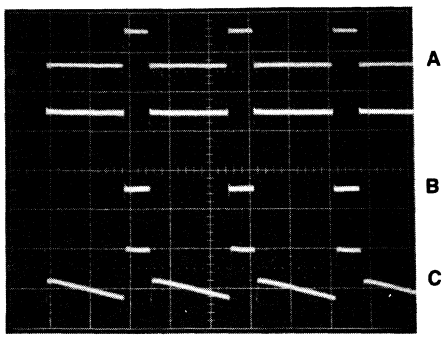
CURRENT-LIMIT THRESHOLD vs SOFT-START VOLTAGE



Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

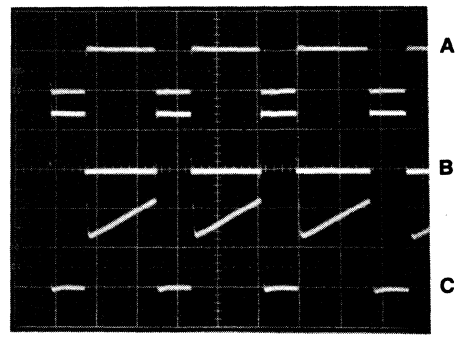
Typical Operating Characteristics (continued)

SWITCHING WAVEFORMS Inverting Section



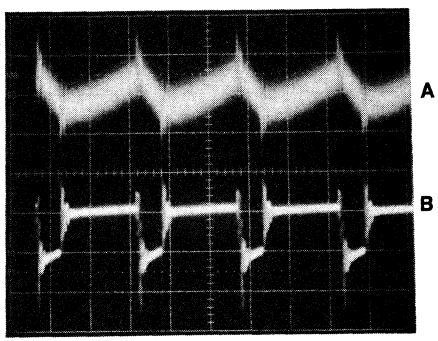
A = Gate Drive, 5V/div
B = Switch Voltage, 10V/div
C = Switch Current, 0.2A/div
Horizontal=2μs/div
I_{LOAD} =100mA
Circuit of Figure 2

SWITCHING WAVEFORMS Step-up Section



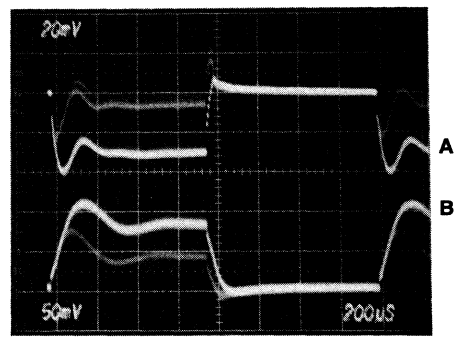
A = Gate Drive, 5V/div
B = Switch Voltage, 10V/div
C = Switch Current, 0.2A/div
Horizontal=2μs/div
I_{LOAD} =100mA
Circuit of Figure 2

OUTPUT-VOLTAGE NOISE, FILTERED AND UNFILTERED



A = Noise with PI Filter, 1mV/div
B = Noise without Filter, 20mV/div
Horizontal=2μs/div
Measured at $-V_{OUT}$
I_{LOAD} =100mA
V+=5V
BW=5MHz
Circuit of Figure 2

LOAD TRANSIENT RESPONSE



A = +VO, 20mV/div
B = −VO, 50mV/div
Horizontal=200μs/div
I_{LOAD} =0 to ±100mA
Circuit of Figure 2

4

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

Pin Description

PIN	NAME	FUNCTION
1	FB+	Step-Up Feedback Input
2	CC+	Step-Up Compensation Capacitor
3	AGND	Analog Ground
4	AV+	Analog Supply Voltage Input (+5V)
5	100/$\overline{200}$	Selects Osc Frequency. Ground for 200kHz, or tie to V+ for 100kHz.
6	12/$\overline{15}$	Selects V_{OUT}. Ground for ±15V, or tie to V+ for ±12V.
7	VREF	Reference Voltage Output (+2.00V) (force to GND or V+ to disable chip).
8	SS	Soft-Start Timing Capacitor (sources 5µA)
9	CC-	Inverting Compensation Capacitor
10	FB-	Inverting Section Feedback Input
11	CSL-	Current Sense Low (Inverting Section)
12	CSH-	Current Sense High (Inverting Section)
13	V+	High-Current Supply Voltage Input (+5V)
14	EXT-	Push-Pull Output - drives external P-channel MOSFET.
15	PDRV	Voltage Input - negative supply for P-channel MOSFET driver.
16	PUMP	Charge-Pump Driver - clock output at 1/2 Oscillator Frequency.
17	EXT+	Push-Pull Output - drives external logic-level N-channel MOSFET.
18	GND	High-Current Ground
19	CSL+	Current Sense Low (Step-Up Section)
20	CSH+	Current Sense High (Step-Up Section)

Operating Principle

Each current-mode controller consists of a summing amplifier that adds three signals: the current waveform from the power switch FET, an output-voltage error signal, and a ramp signal for AC compensation generated by the oscillator. The output of the summing amplifier resets a flip-flop, which in turn activates the power FET driver stage (Figure 1).

Both external transistor switches are synchronized to the oscillator and turn on simultaneously when the flip-flop is set. The switches turn off individually when their source currents reach a trip threshold determined by the output-voltage error signal. This creates a duty-cycle modulated pulse train at the oscillator frequency, where the on time is proportional to both the output-voltage error signal and the peak inductor current. Low peak currents or high output-voltage error signals result in a high duty cycle (up to 90% maximum).

AC stability is enhanced by the internal ramp signal applied to the error amplifier. This scheme eliminates regenerative "staircasing" of the inductor current, otherwise a problem when in continuous current mode and >50% duty cycle. Note that the slope of the ramp signal generated by the current-sense resistor must always be proportional to this internal ramp signal. Lower sense-resistor values necessitate lower inductor values in order to maintain the correct slope. As a rough guide for selecting an inductor value based on the value of the sense resistor, multiply by 0.001:

L (Henries) = R_{SENSE} (Ohms) x 0.001

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

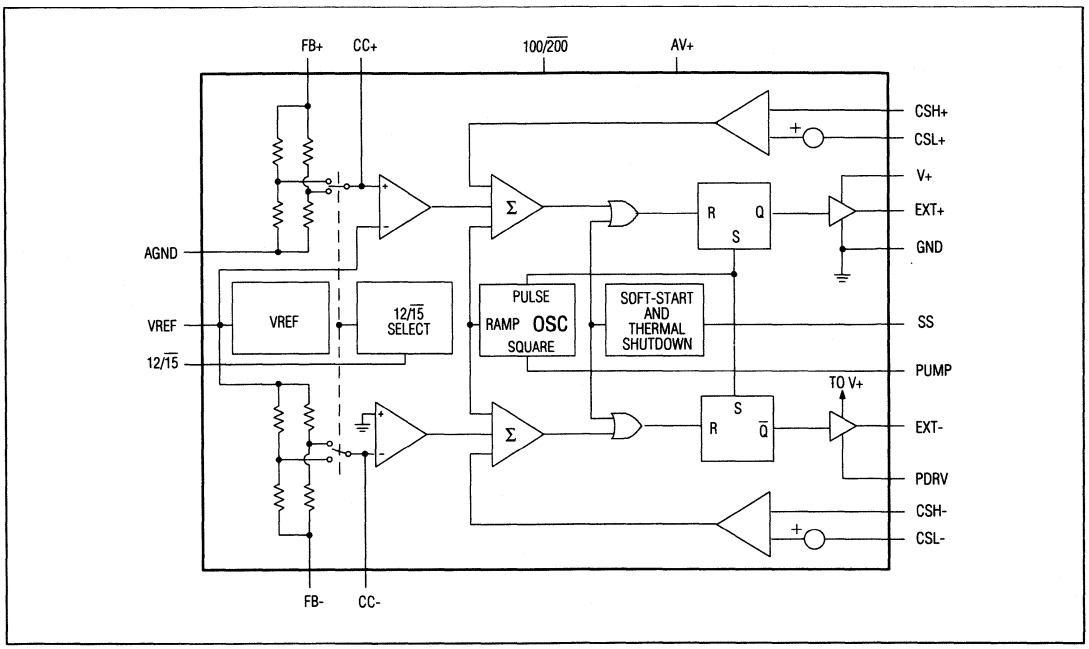


Figure 1. MAX742 Detailed Block Diagram

Detailed Description

100kHz/200kHz Oscillator

The MAX742 oscillator frequency is generated without external components and can be set at 100kHz or 200kHz by pin strapping. Operating the device at 100kHz results in lower supply current and improved efficiency, particularly with light loads. However, component stresses are increased and noise becomes more difficult to filter. For a given inductor value, the lower operating frequency results in slightly higher peak currents in the inductor and switch transistor (see Typical Operating Characteristics, Peak Inductor Current vs. Load Current graph). When the lower frequency is used in conjunction with a LC-type output filter (optional components in Figure 2), larger component values are required for equivalent filtering.

Charge-Pump Voltage Inverter

The charge-pump (PUMP) output is a rail-to-rail square wave at half the oscillator frequency. The square wave drives an external diode-capacitor circuit to generate a negative DC voltage (Point A in Figure 2), which in turn biases the inverting-output drive stage via PDRV. The charge pump thus increases the gate-source voltage applied to the external P-channel FET. The low on resistance resulting from increased gate drive ensures high efficiency and guarantees start-up under heavy loads. If a -5V to -10V supply is already available, it can be tied directly to PDRV and all of the charge-pump components removed. For input voltages greater than 8V, ground PDRV to prevent overvoltage. Observe PDRV Absolute Maximum Ratings.

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

Supply-Voltage Range

Although designed for operation from a +5V logic supply, the MAX742 works well from 4.2V (the upper limit of the undervoltage lock-out threshold) to +10V (absolute maximum rating plus a safety margin). The upper limit can be further increased by limiting the voltage at V+ with a zener shunt or series regulator (see MAX742/MAX743 Application Notes). To ensure AC stability, the inductor value should be scaled linearly with the nominal input voltage. For example, if the application circuit of Figure 3 is powered from a nominal 9V source, the inductor value should be increased to 40µH or 50µH. At high input voltages (>8V), the charge pump can cause overvoltage at PDRV. If the input can exceed 8V, ground PDRV and remove the capacitors and diodes associated with the charge pump.

In-Circuit Testing for Guaranteed Performance

The circuit in Figure 2 has been tested at all extremes of line, load, and temperature. Refer to the Electrical Characteristics table for guaranteed in-circuit specifications. Successful use of this circuit requires no component calculations.

For designs that differ significantly from the basic applications, or for those who have an academic interest in the MAX742, design and component information is covered in detail in UM-3, MAX742/MAX743 Application Notes.

Standard 6W Application

The 6W supply (Figure 2) generates ±200mA at ±15V, or ±250mA at ±12V. By heatsinking the power FETs, using cores with higher current capability (such as Gowanda #050AT1003), and using higher filter capacitance, output capability is increased to 10W or more.

Ferrite and MPP inductor cores optimize efficiency and size. Iron-powder toroids designed for high frequencies (such as MAXL001) are economical, but are larger. Efficiency with MAXL001 inductors is about 80% at full load.

With MAXL001 inductors and MAXC001 or equivalent output filter capacitors, output-voltage ripple at full load is about 100mVp-p at the oscillator frequency (200kHz). Ripple is directly proportional to filter capacitor equivalent series resistance (ESR). In addition, about 250mV transient noise occurs at the LX switch transitions. A very short scope probe ground lead or a shielded enclosure is needed for making accurate measurements of transient noise. Extra filtering, as shown in Figure 2, reduces both noise components.

High-Power 22W Application

The 22W application circuit (Figure 3) generates ±15V at ±750mA or ±12V at ±950mA. Noninductive wire-wound resistors with Kelvin current-sensing connections replace the metal-film resistors of the previous (6W) circuit. Gate drive for the P-channel FET is bootstrapped from the negative supply via diode D6. The 2.7V zener (D5) is required in 15V mode to prevent overvoltage. The charge pump (D3, D4, and C6) may not be necessary if the circuit is lightly loaded (<100mA) on start-up. AIE part #415-0963 is a ferrite pot-core inductor that can be used in place of the smaller, more expensive Gowanda molypermalloy toroid inductor (L1, L2). Higher efficiencies can be achieved by adding extra MOSFETs in parallel. Load levels above 10W make it necessary to add heatsinks, especially to the P-channel FET.

Printed Circuit Layouts

A good layout is essential to clean, stable operation. Use the layouts and component placement diagrams given in Figures 4 through 7. Other construction methods may result in marginal performance. In particular, avoid plastic plug-in protoboards.

Grounding is especially important for low-noise operation. Connect output loads directly across the output filter caps. A top-side ground plane will reduce switching noise and interaction between sections. The short analog ground strip on the pin 1 side of the IC should be connected to ground only by way of pin 2 (AGND). A short connection between this strip and AGND minimizes noise injected into the reference and compensation capacitors. Do not leave 12/15, 100/200, or FB floating.

Component suppliers for the two standard applications are listed at the end of this data sheet.

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

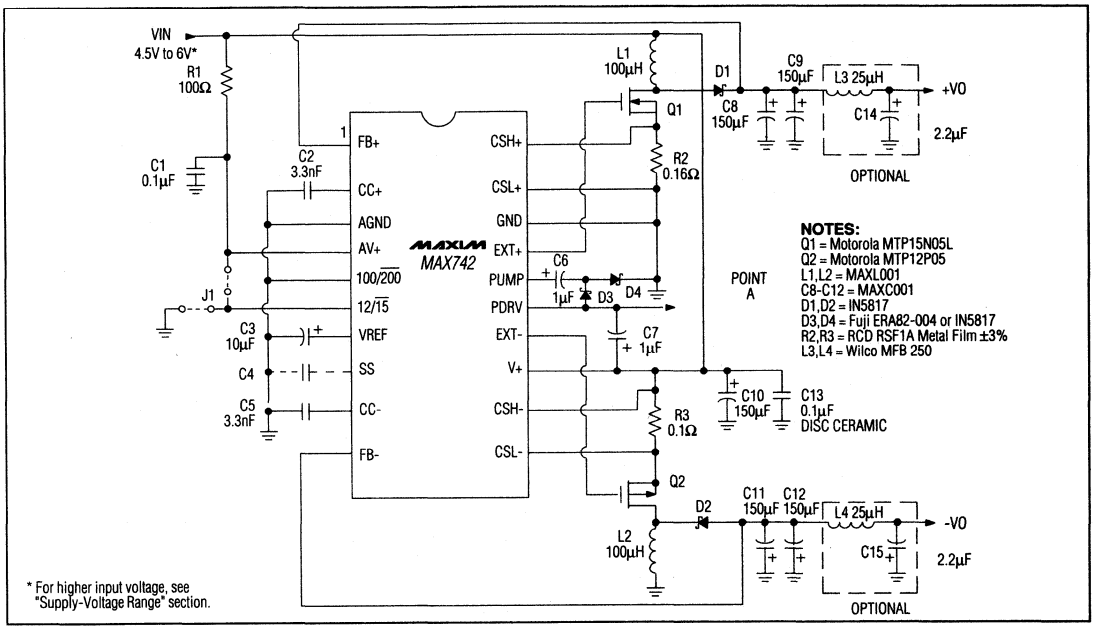


Figure 2. Standard 6W Application Circuit

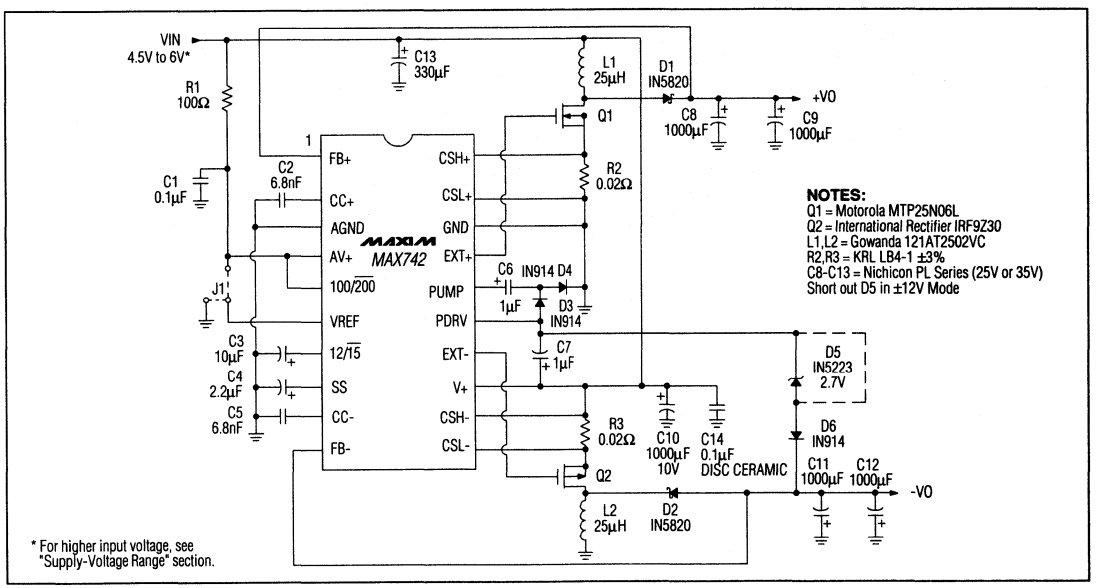


Figure 3. 22W Application Circuit

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

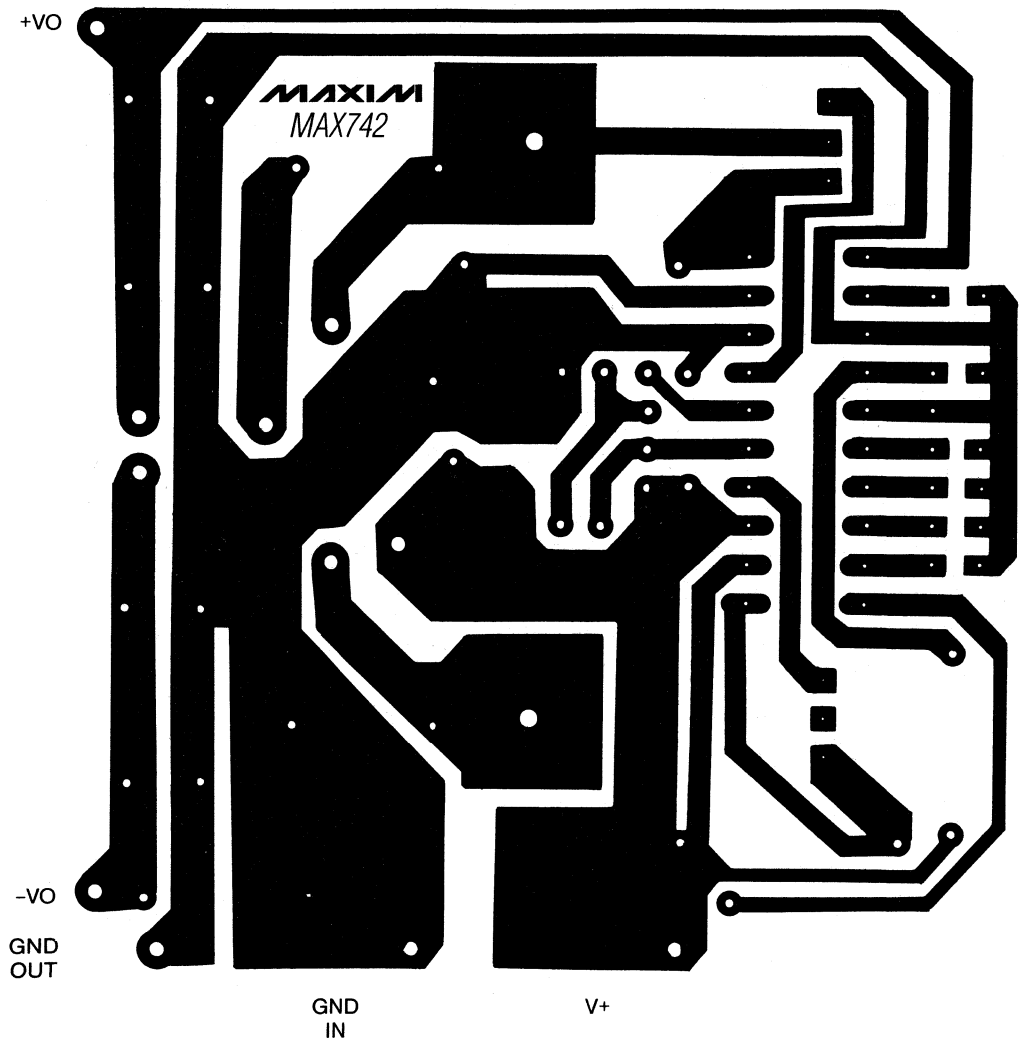


Figure 4. PC Layout for Standard 6W Application (2X Scale, Trace Side View)

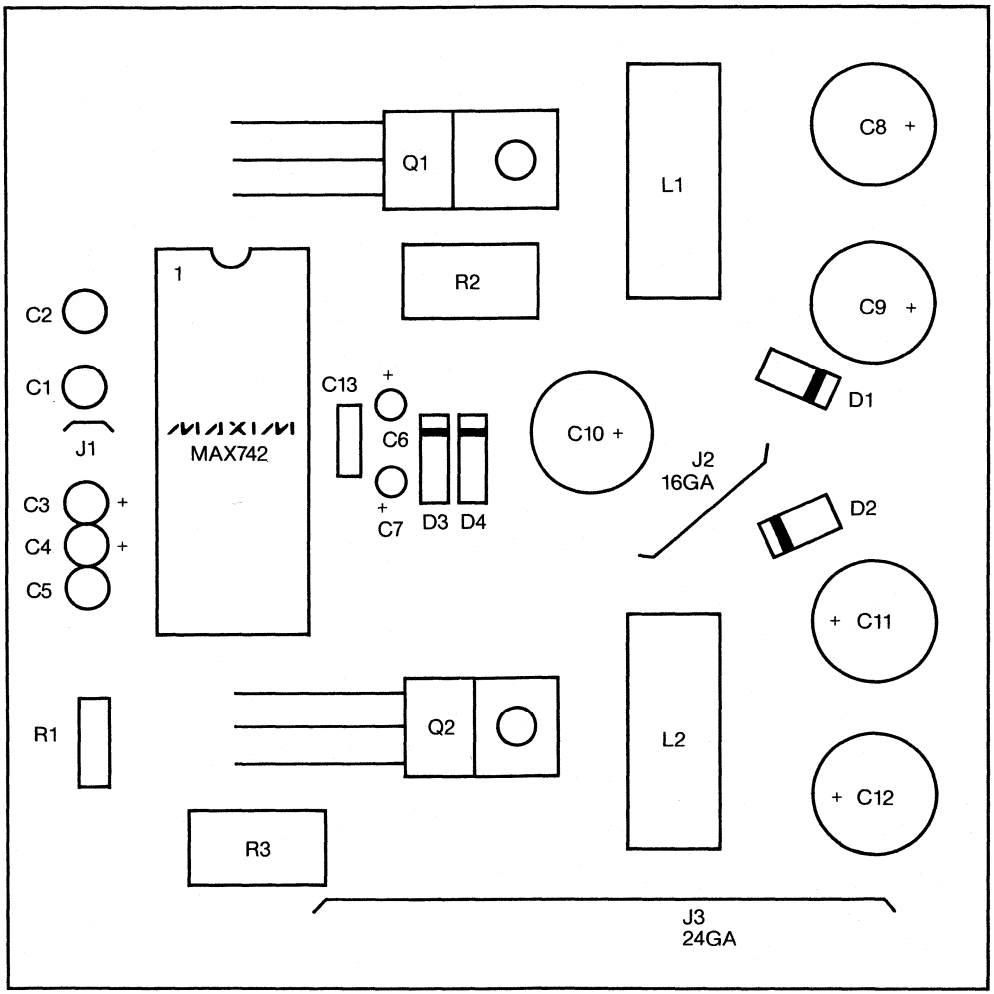


Figure 5. Component Placement for 6W Layout (Top View)

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

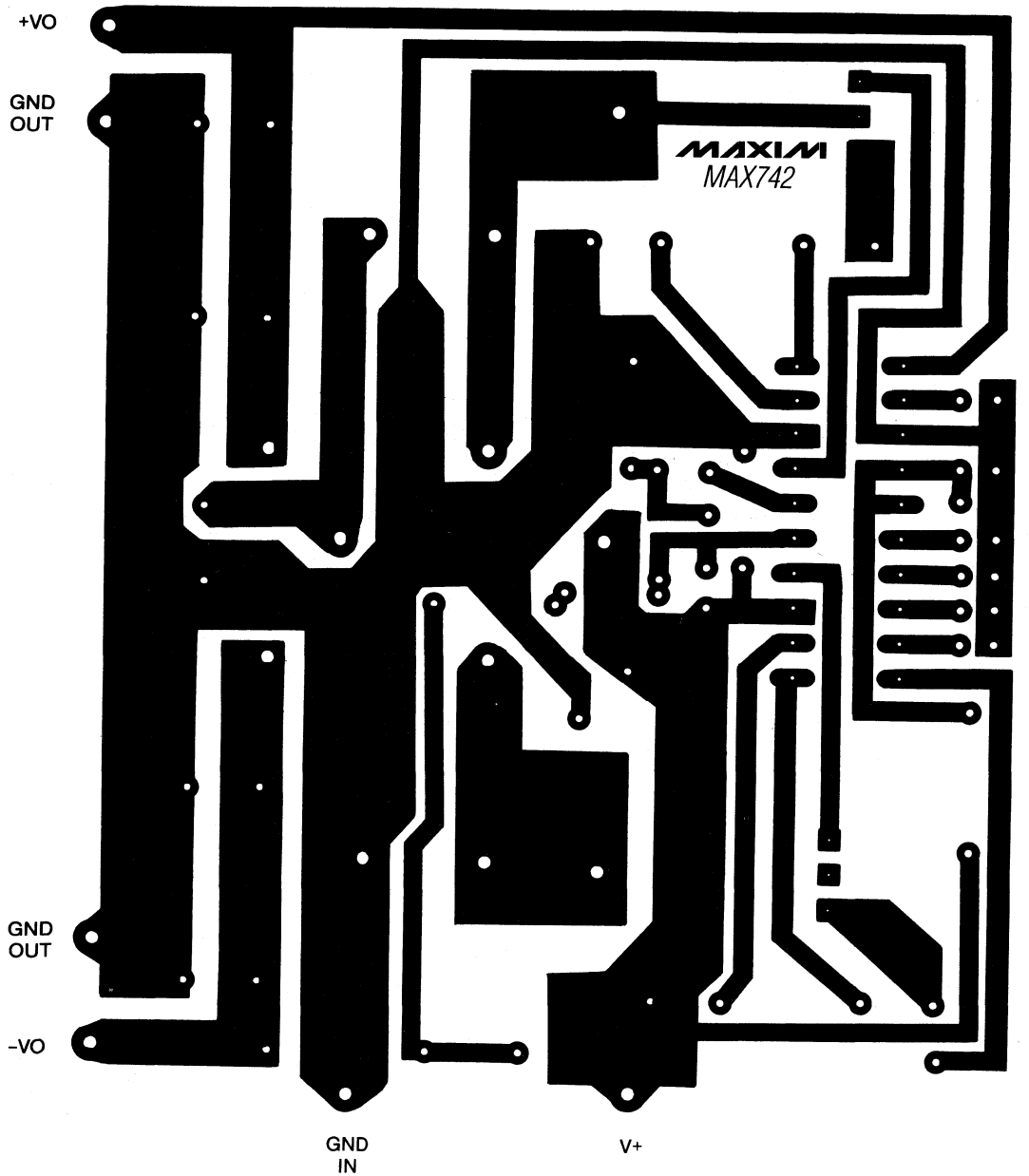


Figure 6. PC Layout for 22W Application (2X Scale, Trace Side View)

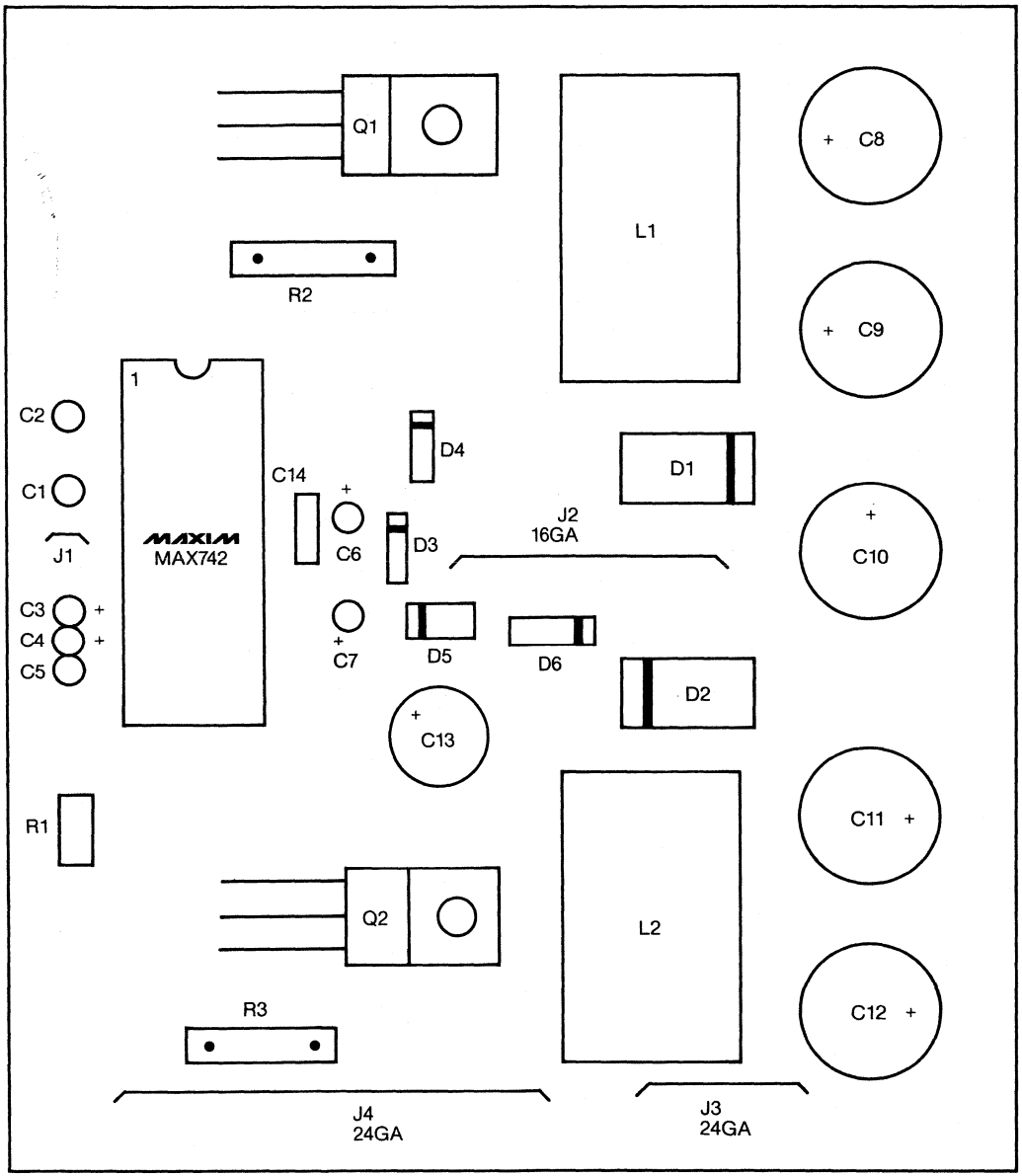


Figure 7. Component Palcement for 22W Layout

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

Soft-Start

A capacitor connected between Soft-Start (SS) and ground limits surge currents at power-up. As shown under Typical Operating Characteristics, the peak switch current limit is a function of the voltage at SS. SS is internally connected to a 5µA current source and is diode-clamped to 2.6V (Figure 8). Soft-start timing is therefore set by the SS capacitor value. As the SS voltage ramps up, peak inductor currents rise until they reach normal operating levels. Typical values for the SS capacitor, when it is required at all, are in the range of 1µF to 10µF.

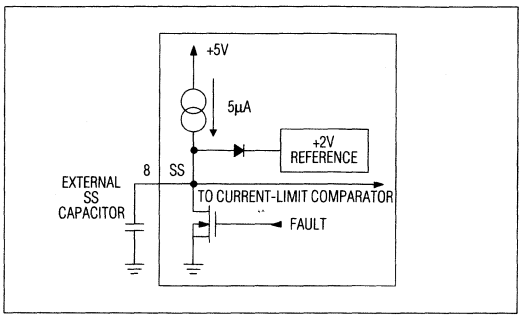


Figure 8. Soft-Start Equivalent Circuit

Fault Conditions Enabling SS Reset

In addition to power-up, the soft-start function is enabled by a variety of fault conditions. Any of the following conditions will cause an internal pull-down transistor to discharge the SS capacitor, triggering a soft-start cycle:

Undervoltage lock-out
Thermal shutdown
VREF shorted to ground or supply
VREF losing regulation

Table 1. Trouble Shooting Chart

SYMPTOM	CORRECTION
Unstable Output. Noise or jitter on output ripple waveform. Scope may not trigger correctly.	Loop stability problem. A. CC+ or CC- disconnected. B. EMI: Move inductor away from IC or use shielded inductors. Keep noise sources away from CC- and CC+. C. Grounding: Tie AGND directly to the filter capacitor ground lead. Ensure that current spikes from GND do not cause noise at AGND or compensation capacitor or reference bypass ground leads. Use wide PC traces or a ground plane. D. Bypass: Tie 10µF or larger between AGND and VREF. Use 150µF to bypass the input right at AV+. If there is high source resistance, 1000µF or more may be required. E. Current Limiting: Reduce load currents. Ensure that inductors are not saturating. F. Slope Compensation: Inductor value not matched to sense resistor.
Noisy Output. Switching is steady, but large inductive spikes are seen at the outputs.	A. Ground noise: Probe ground is picking up switching EMI. Reduce probe ground lead length (use probe tip shield) or put circuit in shielded enclosure. B. Poor HF response: Add ceramic or tantalum capacitors in parallel with output filter capacitors.
Self-destruction. Transistors or IC die on power-up.	A. Input overvoltage: Never apply more than +12V. B. FB+ or FB- disconnected or shorted. This causes runaway and output overvoltage. C. CC+ or CC- shorted. D. Output filter capacitor disconnected.
Poor Efficiency. Supply current is high. Output will not drive heavy loads.	A. Inductor saturation: Peak currents exceed coil ratings. B. MOSFET on resistance too high. C. Switching losses: Diode is slow or has high forward voltage. Inductor has high DC resistance. Excess capacitance at LX nodes. D. Inductor core losses: Hysteresis losses cause self-heating in some core materials. E. Loop instability: See **Unstable Output** above.
No Output. +VO = 5V or less, -VO = 0V.	A. Check connections. VREF should be +2V. B. When input voltage is less than +4.2V, undervoltage lock-out is enabled.
No Switching. ±VO are correct, but no waveform is seen at LX+ or LX-.	Output is unloaded. Apply ±30mA or greater load to observe waveform.

Dual-Output, Switch-Mode Regulator (+5V to ±12V or ±15V)

Component Suppliers

AIE Magnetics
2801 72nd Street N.
St. Petersburg, FL 33710
(813) 347-2181

Collmer Semiconductor (Fuji)
14368 Proton Street
Dallas, TX 75244
(800) 527-0251

Gowanda Electronics
1 Industrial Place
Gowanda, NY 14070
(716) 532-2234

International Rectifier
233 Kansas Street
El Segundo, CA 90245
(213) 772-2000

KRL-Bantry Components
160 Bouchard Street
Manchester, NH 03103
(603) 668-3210

Motorola Semiconductor
P.O. Box 20912
Phoenix, AZ 85036
(602) 244-6900

Nichicon America
927 East State Parkway
Schaumberg, IL 60173
(708) 843-2798

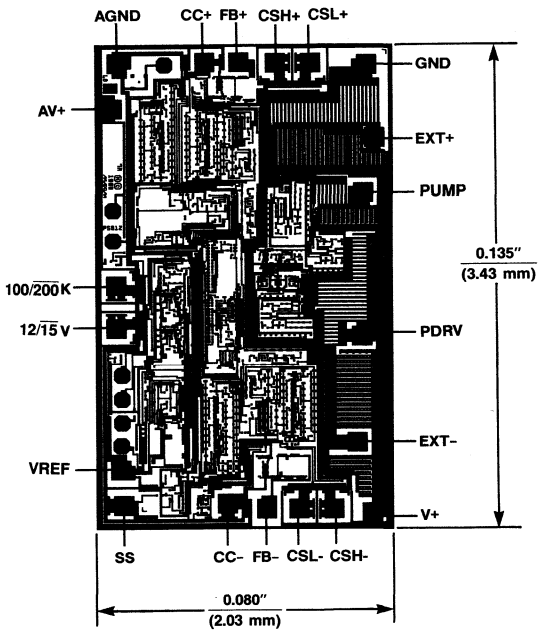
RCD Components
520 E. Industrial Park
Manchester, NH 03103
(603) 669-5455

Wilco Corporation
6451 Saguaro Court
Indianapolis, IN 46268
(317) 293-9300

External Component Ordering Information

PART	DESCRIPTION
MAXL001	100µH Toroid Inductor
MAXC001	150µF Aluminum Electrolytic Capacitor

Chip Topography



NOTE: SUBSTRATE IS CONNECTED TO V+

MAXIM

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

General Description

The MAX743 DC-DC converter IC contains all the active circuitry needed to build small, dual-output power supplies. Relying on simple two-terminal inductors rather than transformers, the MAX743 regulates both outputs independently to within ±4% over all conditions of line voltage, temperature, and load current.

The MAX743 typically provides 75% to 82% efficiency over most of the load range. It operates with current-mode feedback at 200kHz, so it can be used with small, lightweight external components. Also, ripple and noise are easy to filter.

The MAX743 is inherently reliable due to its internal power transistors and monolithic construction. Thermal shutdown prevents overheating, and cycle-by-cycle current sensing protects the power-switch transistors. Other features include undervoltage lock-out and programmable soft-start.

Inductors, capacitors, and diodes to complement the MAX743 can be ordered directly from Maxim in production quantities (page 11). An evaluation kit for prototyping (MAX743EVKIT) is also available (page 9).

If higher load currents are needed, refer to the MAX742 data sheet for a device that drives external power MOSFETs.

Applications

DC-DC Converter Module Replacement

Distributed Power Systems

Computer Peripherals

Portable Instruments

Features

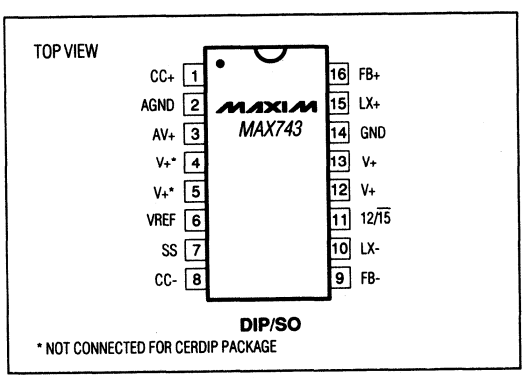
- ♦ **Generates ±100mA or ±125mA**
- ♦ **Specs Guaranteed for In-Circuit Performance**
- ♦ **±4% Output Tolerance Max Over Temp, Line, and Load**
- ♦ **82% Typ Efficiency**
- ♦ **Low-Noise, Current-Mode Feedback**
- ♦ **On-Board Current Limiting**
- ♦ **Thermal Shutdown Protection**
- ♦ **Undervoltage Lock-Out and Soft-Start**
- ♦ **Switches From ±15V to ±12V Under Logic Control**
- ♦ **Evaluation Kit Available**
- ♦ **Internal Power MOSFETs**

Ordering Information

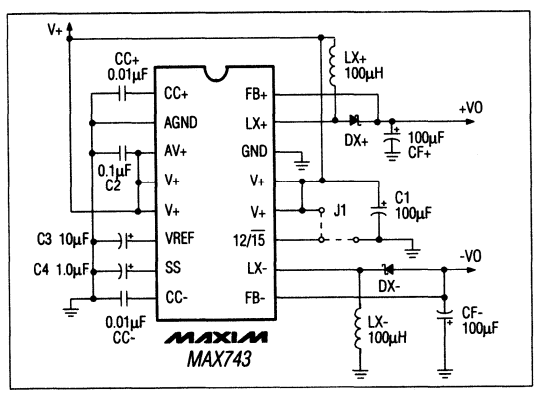
PART	TEMP. RANGE	PIN-PACKAGE
MAX743CPE	0°C to +70°C	16 Plastic DIP
MAX743CWE	0°C to +70°C	16 Wide SO
MAX743C/D	0°C to +70°C	Dice
MAX 743EPE	-40°C to +85°C	16 Plastic DIP
MAX743EWE	-40°C to +85°C	16 Wide SO
MAX743MJE	-55°C to +125°C	16 CERDIP

Ordering information continued on page 11.

Pin Configuration



Typical Operating Circuit



Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, +4.5V < V+ < +5.5V, Note1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage						
±15V Mode	0mA < I_{LOAD} < 100mA 12/15 = 0V	T_A = +25°C	14.55		15.45	V
		T_A = T_{MIN} to T_{MAX}	14.40		15.60	
±12V Mode	0mA < I_{LOAD} < 125mA 12/15 = V+	T_A = +25°C	11.64		12.36	V
		T_A = T_{MIN} to T_{MAX}	11.52		12.48	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +5.0V, 12/$\overline{15}$ pin = 0V, I_{LOAD} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Efficiency	I_{LOAD} = ±50mA	LX = MAXL001		79		%
		LX = MPP Toroid		82		
Supply Current (Note 2)				20	30	mA
Standby Current	VREF = +5V, includes VREF current			2.2	4	mA
Line Regulation	V+ = +4.5V to +5.5V				0.05	%/%
Load Regulation	I_{LOAD} = 0 to 100mA				1	%
Reference Voltage	VREF			2.0		V
Oscillator Frequency			170	200	230	kHz
Undervoltage Lock-Out	Measured at V+		3.8		4.2	V
Thermal Shutdown Threshold				+190		°C
LX+ On Resistance (Note 3)				1.2	3.0	Ω
LX- On Resistance (Note 3)				1.0	2.2	Ω
LX+ Leakage Current (Note 4)	LX+ = +17V, V+ = 6V				100	µA
LX- Leakage Current (Note 4)	LX- = -17V, V+ = 6V				-100	µA
Compensation Pin Impedance	CC+, CC-			10		kΩ
Soft-Start Source Current	SS = 0V		3.0		7.0	µA
Soft-Start Sink Current	SS = 2V, V+ = 3.8V		0.5	2.0		mA

Note 1: All devices tested to full-load conditions with 50ms pulsed loads using automatic test equipment. In continuous operation, the maximum allowable output current is determined by package thermal characteristics and passive component ratings.
Note 2: Total supply current including inductor current. The worst case for supply current occurs at low input voltage.
Note 3: Guaranteed by design, not 100% tested. Output currents are 100% tested.
Note 4: Tested at wafer level only, not in packaged form.

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
(V+ or AV+ to GND) ..... +7V, -0.3V (±12V Mode)
+6V, -0.3V (±15V Mode)
Output Switch Voltages (LX+ to GND) ..... +17V, -0.3V
(LX- to V+) ..... -23V, +0.3V
Output Switch Currents
(LX+ Sink Current, Peak) 2.0A
(LX- Source Current, Peak) ..... -2.0A
Power Dissipation ..... See Figure 2

Operating Temperature Range
MAX743C_ _ ..... 0°C to +70°C
MAX743E_ _ ..... -40°C to +85°C
MAX743MJE ..... -55°C to +125°C
Junction Temperature
MAX743C/E ..... +150°C
MAX743MJE ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION - OBSERVE PROTOTYPING PRECAUTIONS BELOW

- **DO NOT INSERT DEVICE INTO SOCKET WITH POWER APPLIED.**
- **BE CERTAIN THAT OUTPUT FILTER CAPACITORS ARE CONNECTED.**
- **DO NOT SOLDER OR WORK ON CIRCUIT WHILE POWER IS APPLIED.**
- **OBSERVE SUPPLY VOLTAGE RATINGS CAREFULLY.**

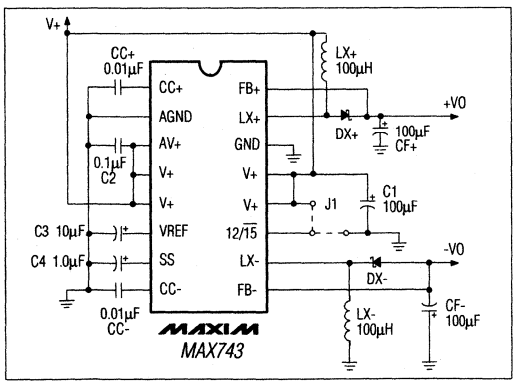


Figure 1. Basic Application Circuit

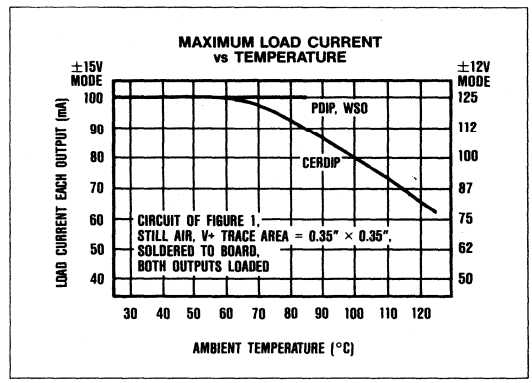


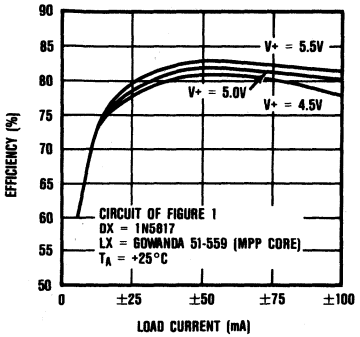
Figure 2. Maximum Load Current Vs. Temperature

Notes: LX Inductors: MAXL001 or equivalent.
CF Filter Capacitors: MAXC001 or 100µF low-ESR equivalent.
C1 Bypass Capacitor: MAXC001 or 22µF 16V Tantalum or equivalent.
C4 Soft-Start Capacitor is optional.
DX Schottky Diodes: 1N5817 or equivalent.

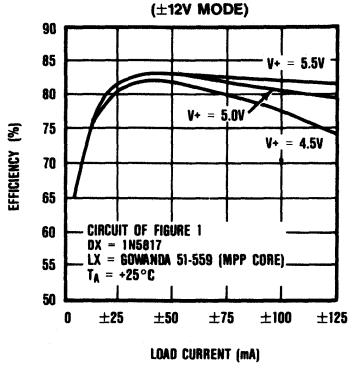
Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

Typical Operating Characteristics

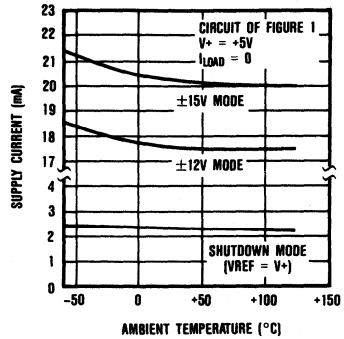
EFFICIENCY vs LOAD CURRENT (±15V MODE)



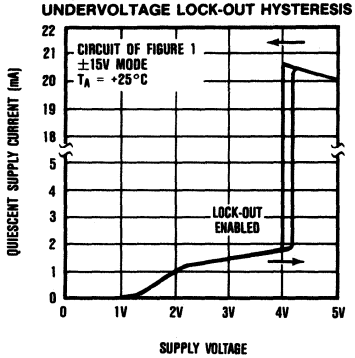
EFFICIENCY vs LOAD CURRENT (±12V MODE)



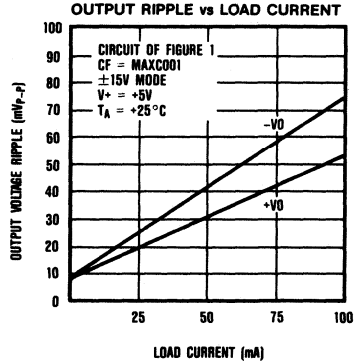
QUIESCENT SUPPLY CURRENT vs TEMPERATURE



UNDERVOLTAGE LOCK-OUT HYSTERESIS



OUTPUT RIPPLE vs LOAD CURRENT



Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

Pin Description

PIN	NAME	FUNCTION
1	CC+	Step-Up Compensation Capacitor
2	AGND	Analog Ground
3	AV+	Analog Supply Voltage Input (+5V)
4, 5	V+	High-Current Supply Voltage Input (+5V); N.C. for CERDIP Package
6	VREF	Reference Voltage Output (+2.00V)
7	SS	Soft-Start Timing Capacitor (Sources 5µA)
8	CC-	Inverting Compensation Capacitor
9	FB-	Inverting-Section Feedback Input
10	LX-	Inverting-Section Switch Output
11	12/$\overline{15}$	Selects VOUT: Ground for ±15V or tie to V+ for ±12V
12, 13	V+	High-Current Supply Voltage Input (+5V)
14	GND	High-Current Ground
15	LX+	Step-Up Section Switch Output
16	FB+	Step-Up Section Feedback Input

Operating Principle

Each current-mode controller consists of a summing amplifier that adds three signals: the current waveform from the power switch FET, a VOUT-VREF error signal, and a ramp signal for AC compensation generated by the oscillator (Figure 3). The output of the summing amplifier gates a flip-flop, which in turn drives the power FET switch.

Both switches are synchronized to the oscillator and turn on simultaneously when the flip-flops are set. The transistors turn off individually when their switch currents reach a trip threshold determined by the VOUT-VREF error signal. This creates a duty-cycle modulated pulse train at 200kHz, where the on time is proportional to both the output voltage error signal and the peak inductor current. Low peak currents or high output voltage error signals result in a high duty cycle (up to 90% maximum).

The MAX743 oscillator frequency is generated without external components and is not adjustable. The device is laser-trimmed to 200kHz at wafer level, resulting in clean, predictable operation.

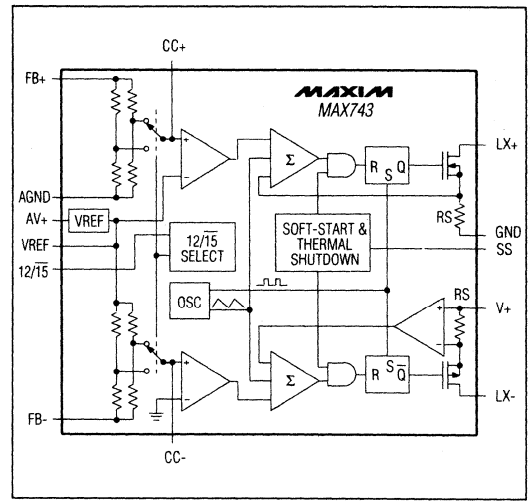


Figure 3. MAX743 Block Diagram

In-Circuit Testing for Guaranteed Performance

The circuit in Figure 1 has been tested at all line, load, output current, and temperature limits. Refer to the Electrical Characteristics table for guaranteed in-circuit specifications. Successful use of this circuit requires no component calculations.

Many modifications of this basic circuit, such as remote shutdown, reduced noise, nonstandard passive components, and oddball input/output voltages, are explored in an application note. Refer to UM-3, MAX742/MAX743 Application Notes.

Standard 3W Application

With MAXL001 inductors and MAXC001 or equivalent output filter capacitors, output voltage ripple at full load is about 75mVp-p at the oscillator frequency (200kHz). In addition, about 250mV transient noise occurs at the LX switch transitions. Extra filtering (Figure 9) reduces both noise components.

The choice of inductor type involves a trade off, which optimizes either cost and size or EMI and noise performance. Suggested design approaches for mainstream applications are given in the Component Design Chart of Table 1.

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

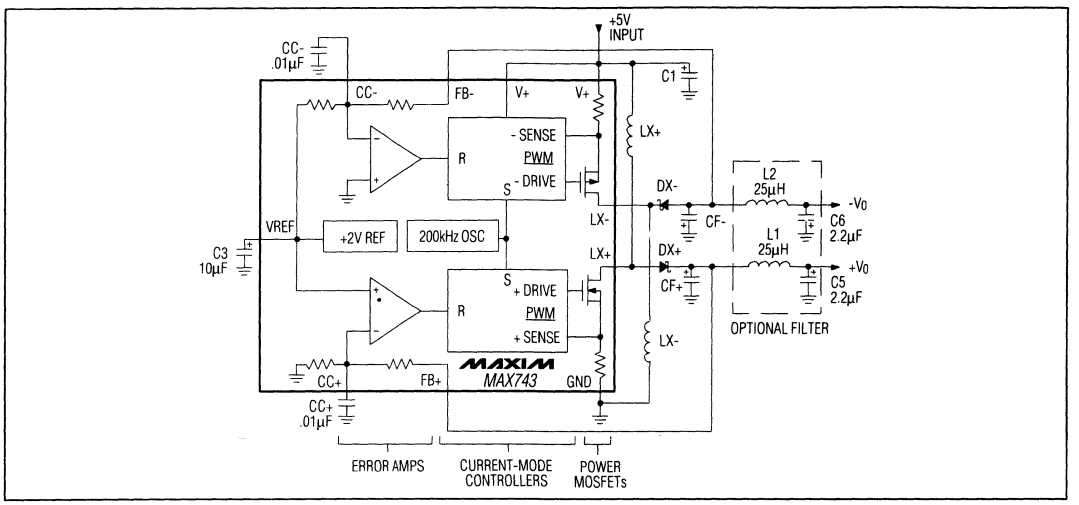


Figure 4. Functional Diagram with Optional Pi Filter

Table 1. Component Design Chart

DESIGN REQUIREMENT				
LOW COST, LOW NOISE	**LOWEST COST**	**WIDE TEMP RANGE**	**MINIATURE**	**SURFACE MOUNT**
INDUCTOR				
Iron-Powder Toroid	Ferrite Bobbin	Many Types OK	Hi-Flux (MPP) Toroid	Hi-Flux (MPP) Toroid
* 0.6" Diameter * Low EMI * 79% Efficiency	* 0.6" Long * Some Noise * 82% Efficiency		* 0.28" Diameter * Low EMI * 80% Efficiency	* Surface Mount Version
MAXL001 Sold by Maxim G # 51-548	C # 7070-25 G # GA10-103K I # LS4-100	All Listed Inductors	Gowanda Corp. Part # 51-559	Gowanda Corp. Part # 51-560
CAPACITOR				
150µF Low-ESR Aluminum Electrolytic	220µF Standard Aluminum Electrolytic	Solid Tantalum (Sintered Anode)	47µF Tantalum// 4.7µF Ceramic	33µF Tantalum// 33µF Tantalum
* -25°C to +105°C * Lowers Ripple * Radial Mount	* 0°C to +85°C * 16V or up	* -55°C to +125°C * Lowers Ripple	* 0°C to +70°C * May Need Additional Compensation	* 0°C to +70°C
MAXC001 Sold by Maxim Nichicon PL Series	Multiple Suppliers	THF Series Mallory	RPE230 Series Murata Erie	267 Series Matsuo
RECTIFIER				
1N5817	1N5817	1N5802 (UES1102)	MBR030 Motorola	PRLL5817 Amperex/Phillips
PRINTED CIRCUIT LAYOUT				
See Figure 6	See UM-3 MAX742/743 Application Notes	Modify Layout of Figure 6	Modify Layout of Figure 6	See UM-3 MAX742/743 Application Notes

C = Caddell-Burns (516) 746-2310 G = Gowanda (716) 532-2234 I = Inductor Supply (714) 978-2277

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

Printed Circuit Layout for Radial-Mount Components

Clean, stable operation requires a good layout (Figure 6). Grounding is especially important for low-noise operation. Do not connect the short analog-ground strip on the Pin 1 side of the IC to the ground plane or any other ground. A short connection between this strip and AGND minimizes noise coupled to the reference and compensation capacitors. All V+ pins on plastic DIP and wide SO packages are connected to a lead frame designed for low thermal resistance. For maximum heatsinking, solder Pins 4, 5, 12, and 13 directly to a large copper trace. For ±12V operation, cut the thin trace connected to 12/15 and install jumper, J1.

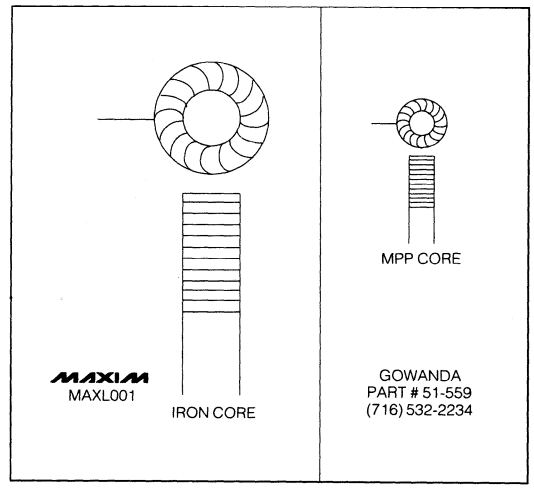


Figure 5. 100µH Low-EMI Inductors for 3W Supplies (Actual Sizes) (See Table 1)

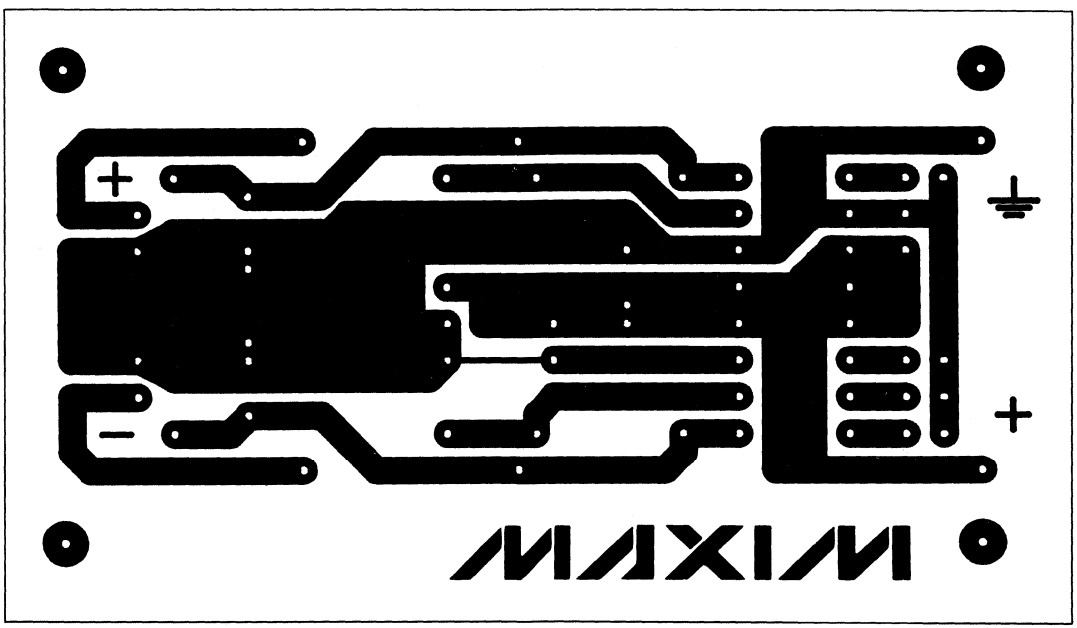


Figure 6. PC Layout for Circuit of Figure 4 Using MAXL001/MAXC001 (2X Scale)

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

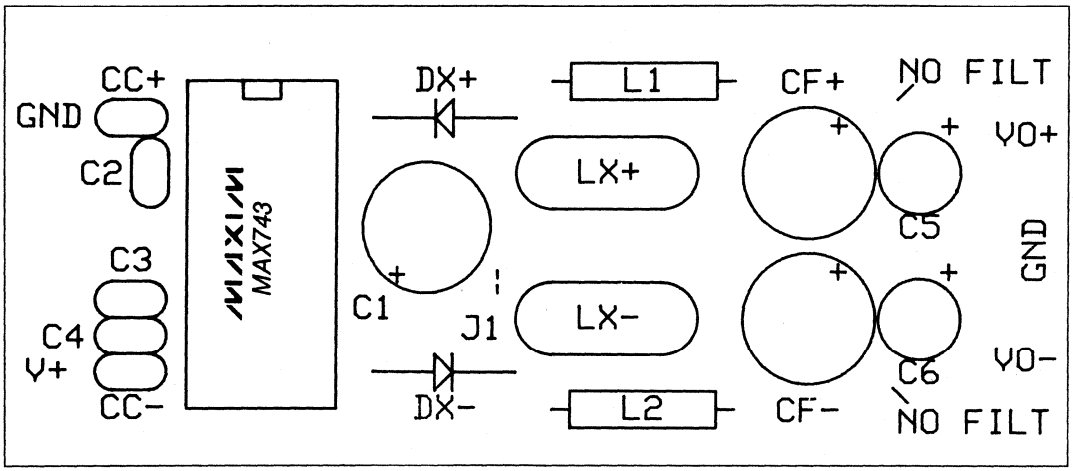


Figure 7. Component Placement Diagram for PC Layout of Figure 6

Table 2. Trouble Shooting Chart

SYMPTOM	CORRECTION
Unstable Output. Noise or jitter on output ripple waveform. Scope may not trigger correctly.	Loop stability problem. A. CC+ or CC- disconnected. B. EMI: Move inductor away from IC or use shielded inductors. Keep noise sources away from CC- and CC+. C. Grounding: Tie AGND directly to the filter capacitor ground lead. Ensure that current spikes from GND do not cause noise at AGND or any of the comp capacitor or reference bypass ground leads. Use wide PC traces or a ground plane. D. Bypass: Tie 1.0µF ceramic or larger between AGND and VREF. Use 22µF tantalum to bypass the input right at AV+. If there is high source resistance, 1000µF or more may be required. E. Current Limiting: Reduce load currents. Ensure that inductors are not saturating.
Noisy Output. Switching is steady, but large inductive spikes are seen at the outputs.	A. Ground noise: Probe ground is picking up switch noise. Reduce probe ground lead length (use probe tip shield). B. Poor HF response: Add ceramic or tantalum capacitors in parrallel with output filter capacitors.
Self-destruction. Parts die on power-up.	A. Input overvoltage: Never apply more than +6V to V+ in ±15V mode or +7V in ±12V mode. B. FB+ or FB- disconnected or shorted. This causes runaway and output overvoltage. C. CC+ or CC- shorted. D. Filter capacitor disconnected.
Poor Efficiency. Supply current is high. Output will not drive heavy loads.	A. Inductor saturation: Peak currents exceed coil ratings. B. Inductor value too low or too high. C. Switching losses: Diode is slow or has high forward voltage. Inductor has high DC resistance. Excess capacitance at LX nodes. D. Inductor core losses: Eddy currents cause self-heating in some core materials. E. Loop instability: See **Unstable Output** above.
No Output. +VO = 5V or less, -VO = 0V.	A. Check connections. VREF should be +2V. B. When input voltage is less than +4.2V, undervoltage lock-out is enabled.
No Switching. ±VO are correct, but no waveform is seen at LX+ or LX-.	Output is unloaded. Apply ±10mA or greater load to observe waveform.

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

MAX743EVKIT
Power-Supply Evaluation Kit (+5V to ±15V or ±12V)

Description

The MAX743EVKIT Evaluation Kit demonstrates the output capabilities and noise performance of the MAX743 standard application circuit (Figure 1). The kit includes main switching components identical to those found in the high-volume production kit described on page 11 (MAX743CPEKIT). With a few quick modifications, the circuit can also serve as a low-noise test bed to evaluate other components, such as the miniature MPP toroid inductor of Figure 5. The kit includes optional Pi filters shown in the Functional Diagram (Figure 4), which reduce output noise to less than 2mVp-p.

Evaluation Kit Contents

(1) Single-Sided FR4 PC Board with Low-Noise Layout

(1) MAX743CPE Plastic DIP IC

(2) MAXL001 Toroid Inductors (LX+, LX-)

(2) 1N5817 Schottky Diodes (DX+, DX-)

(3) MAXC001 Filter and Bypass Capacitors (C1, CF+, CF-)

(1) 0.1µF Ceramic Capacitor (C2)

(2) 0.01µF Ceramic Capacitors (CC+, CC-)

(1) 10µF Tantalum Capacitor (C3)

(2) 2.2µF Tantalum Capacitors (Pi Filter: C5, C6)

(2) 25µH Bobbin Inductors (Pi Filter: L1, L2)

(1) 1Ω 1/2W Carbon Resistor

(2) 180Ω 2W Carbon Resistors

Evaluation Kit Assembly and Test Instructions

Tools: Soldering iron, rosin-core solder, 22 AWG stranded hookup wire, side cutters, wire strippers, utility knife, +5V @ 1A supply, oscilloscope, 10X probe, and a DC voltmeter.

1. Build Circuit. Assemble the PC board according to the component placement diagram of Figure 7 and the schematic of Figure 4. 3 resistors will be left over (and used for testing). The extra holes near LX and CF are options for nonstandard component sizes. Do not install jumper, J1, or C4.

2. Apply Power. Apply a +5V source with 1A load capability to V+, and measure the outputs. CAUTION: Measure the source carefully before applying power because overvoltage may damage the device. Be careful while handling the board to avoid shorting CC+ and CC- while power is applied.

3. Load Outputs. Connect a 180Ω 2W resistor across each output to observe full-load characteristics. The oscillator can be monitored indirectly by observing, via a scope probe, the inductive-switching waveforms on LX- or LX+. Some ringing at these nodes is normal.

4. Observe Noise. Move the output hookup wire connections from VO to the terminals marked NO FILT, and remove the 2.2µF capacitors (C5 and C6) to route the outputs around the small inductors. This demonstrates performance without extra filtering components. The 25µH bobbin inductor has a maximum resistance of 1.5Ω, so the filter can introduce 150mV of added load regulation error in ±15V mode (100mA x 1.5Ω).

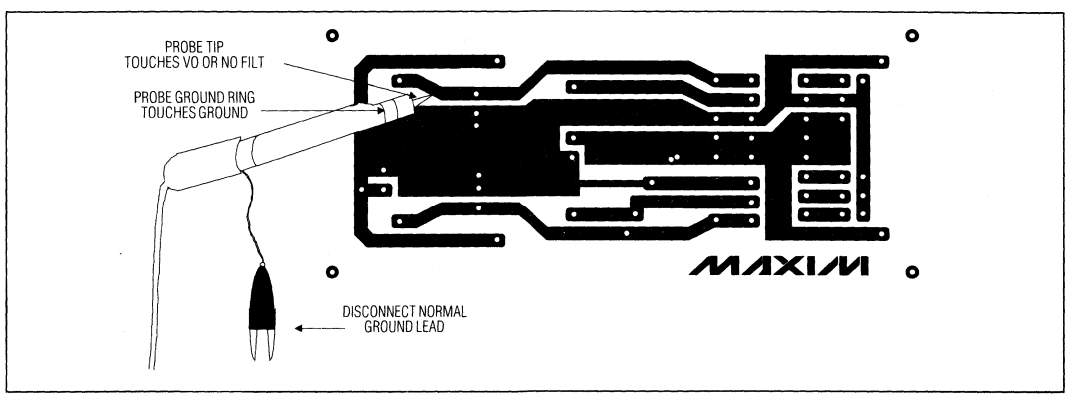


Figure 8. Noise Measurement

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

5. Noise: Real or Not? A very short scope probe ground lead **must** be used to eliminate induced switching noise unless the board is placed in a shielded enclosure. Many probes have a ground ring near the tip (underneath the probe tip cover) normally used to insert the tip into a BNC jack. Place the probe so this probe ground ring touches the filter capacitor ground lead while the probe tip touches VO (Figure 8). Also, ground noise can often be reduced by connecting the case (earth) ground of the +5V source to circuit ground.

6. Observe Inductor-Current Waveform. Insert the 1Ω resistor provided between the LX- inductor and ground. Put the scope probe on the resistor (DC coupling). At full load, the inductor current will not decay to 0 with each cycle, and the waveform will appear as a triangle superimposed on a large (400mA) negative DC pedestal.

7. Verify Feedback Action. Varying the supply voltage causes distinct changes in duty cycle, which can be seen in the inductor-current waveform. If a decade resistor box or power rheostat is available, overcurrent protection can be exercised. The current-limit circuit functions as an output power limiter, so as load resistance is reduced, the output voltage gradually decreases.

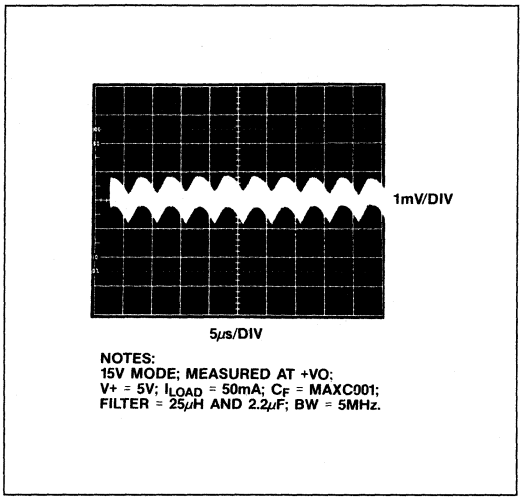


Figure 9. Output Noise Voltage with Pi Filter

Soft-Start

Normally, the Soft-Start pin (SS) can be left open. However, to limit surge current at start-up, a capacitor can be connected between SS and ground.

As shown in Figure 10, the peak switch current limit is a function of the voltage at the Soft-Start pin. The SS pin is connected to a 5µA current source that is diode clamped to 2.6V, so the duration of soft-start current limiting can be set by attaching a capacitor between SS and ground. Additionally, the fault conditions that normally disable the IC also turn on an N-Channel MOSFET and rapidly discharge the SS capacitor to ground (Figure 11).

Fault Conditions Enabling SS Reset

Undervoltage Lock-out
Thermal Shutdown
VREF shorted to GND or supply
VREF losing regulation

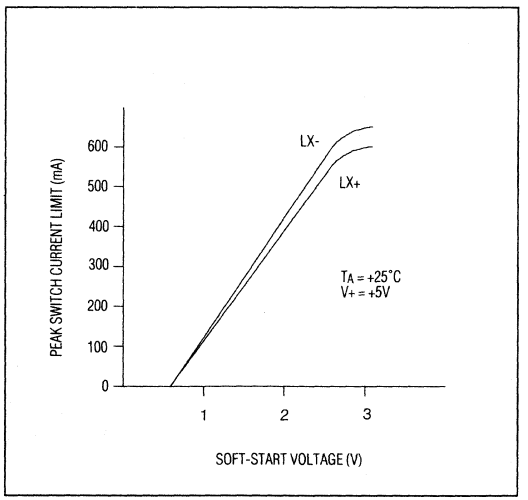


Figure 10. Typical Peak Switch Current Limit vs. Soft-Start Voltage

Dual-Output, Switch-Mode Regulator (+5V to ±15V or ±12V)

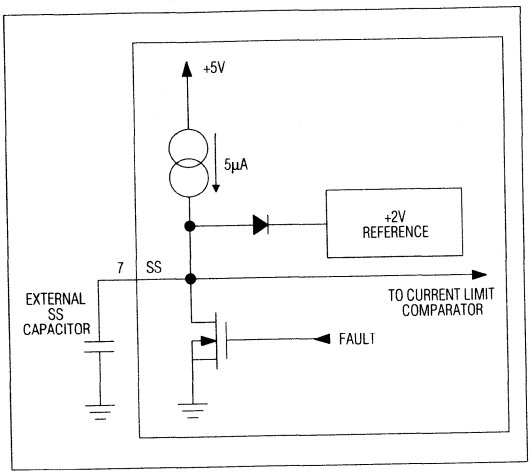


Figure 11. Soft-Start Equivalent Circuit

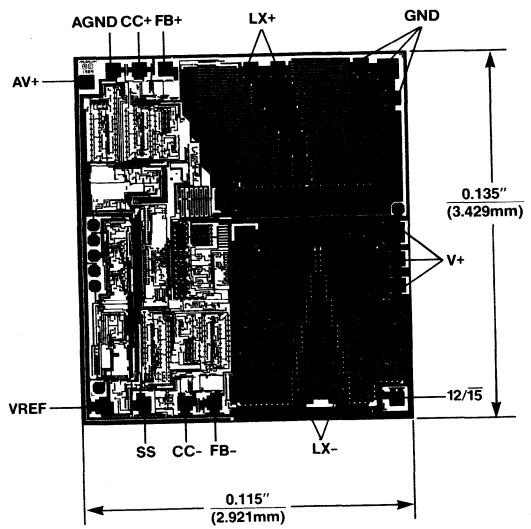
Production and Evaluation Kits

Production kits for high-volume manufacturing as well as evaluation kits for prototyping can be ordered directly from Maxim. Both kits include key external components, such as MAXL001 low-loss iron-powder inductors and MAXC001 low-ESR capacitors, but the evaluation kit also includes a PC board, optional Pi filter components, and compensation capacitors. MAXL001 and MAXC001 can also be ordered individually. The production kit is available in commercial and extended temperature ranges.

Production Kit Contents

(1) MAX743 Integrated Circuit (Plastic DIP)
(3) MAXC001 150µF Capacitors
(2) MAXL001 100µH Inductors
(2) 1N5817 Schottky Rectifiers

Chip Topography



Ordering Information (continued)

PART	DESCRIPTION
MAX743EVKIT	Evaluation Kit
MAX743CPEKIT	Production Kit (0°C to +70°C)
MAX743EPEKIT	Production Kit (-25°C to +85°C)
MAXL001	100µH Inductor
MAXC001	150µF Capacitor

MAXIM

150µF Low-ESR Aluminum Electrolytic Capacitor

General Description

The MAXC001 is a 150µF capacitor designed for filtering and bypassing in DC-DC converters, low-dropout linear regulators, and other circuits requiring miniaturization in conjunction with low cost and low Equivalent Series Resistance (ESR). The MAXC001 has excellent impedance characteristics, particularly at the 20kHz to 200kHz switching frequencies which are common to low-power switching-regulator circuits. The MAXC001 is ideal for use in distributed power supplies and portable equipment.

Features

- ♦ **0.2Ω Max ESR at 100kHz**
- ♦ **Miniature 10mm x 12.5mm Can Size**
- ♦ **35V Continuous DC Rating**
- ♦ **Radial Printed-Circuit (PC) Board Mounting**
- ♦ **Excellent High-Frequency Performance**

Applications

Switching Regulators

DC-DC Converters

Charge Pumps

Low-Dropout Linear Regulators

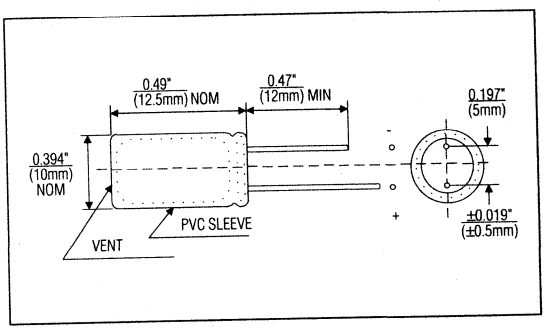
Ordering Information

PART	TEMP. RANGE	VALUE
MAXC001	-25°C to +105°C	150µF ±20%

Physical Characteristics

Diameter	0.394" (10mm) Nominal 0.421" (10.7mm) Max
Length	0.492" (12.5mm) Nominal 0.551" (14mm) Max
Casing	Solvent-Proof Type
Lead Spacing	0.197" (5mm) Nominal
Lead Length	0.472" (12mm) Min 26 AWG
Lead Finish	Tin-Lead Solder

MAXC001 Low-ESR Capacitor



150µF Low-ESR Aluminum Electrolytic Capacitor

ABSOLUTE MAXIMUM RATINGS

Ripple Current (100kHz, +105°C) 625mA
Ripple Current (120Hz, +105°C) 435mA

Operating Temperature Range . . . . . -25°C to +105°C
Storage Temperature Range . . . . . -40°C to +105°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the capacitor. These are stress ratings only, and functional operation at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, Note 1.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance	120Hz	120	150	180	µF
ESR	100kHz		0.10	0.2	Ω
Applied Voltage		35			V
Leakage Current	V = 35V			5	µA

Note 1: Maxim sample tests these parameters to an LTPD = 10.

Applications Information

DC-DC Converter Filtering

While designed specifically for the MAX743 dual-output current-mode +5V to ±15V or ±12V converter (Figure 1), the MAXC001 works well for many low-power DC-DC converter and charge-pump applications. For best filtering action, place a 0.1µF monolithic ceramic capacitor in parallel with the MAXC001.

MAXC001 Compatible Power-Supply ICs

STEP UP	INVERTING	STEP DOWN	LOW VOLTAGE	DUAL OUTPUT
MAX630	MAX634	MAX638	MAX654	MAX742
MAX631	MAX635		MAX655	MAX743
MAX632	MAX636		MAX656	
MAX633	MAX637		MAX657	
MAX4193	MAX4391		MAX658	
MAX641			MAX659	
MAX642				
MAX643				

LOW-DROPOUT LINEAR	CHARGE PUMP
MAX667	ICL7660
	ICL7662
	MAX680

150µF Low-ESR Aluminum Electrolytic Capacitor

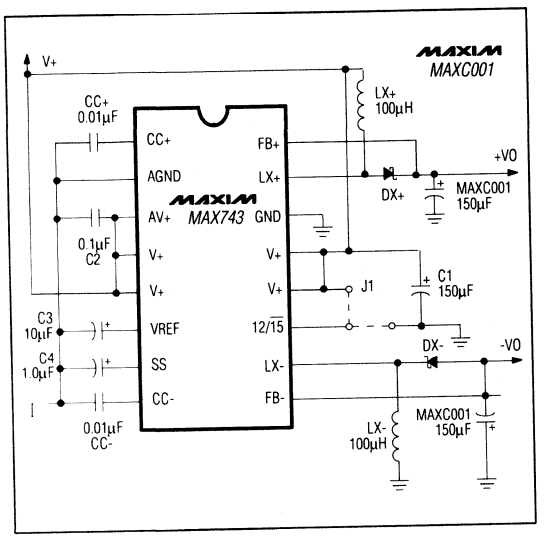


Figure 1. Bypass and Filter Capacitor Application (MAX743 +5V to ±15V Converter)

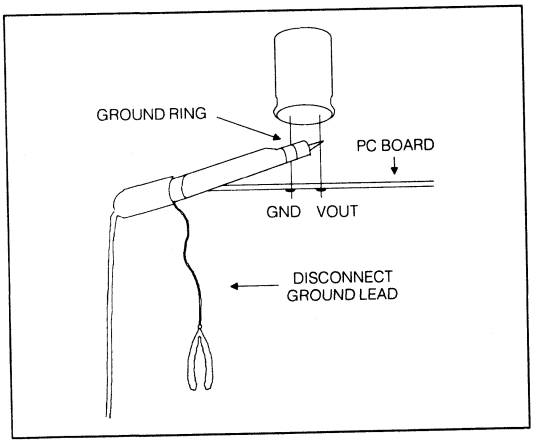


Figure 2. Noise Measurement

Eliminating Noise Spikes

Large noise spikes, hundreds of millivolts or even volts in amplitude, often threaten to upset sensitive circuits. These noise spikes are sometimes eliminated by replacing existing general-purpose capacitors with high-quality, low-ESR capacitors such as the MAXC001. In other cases, the measurement technique may introduce apparent noise.

Long-scope probe ground leads often cause measurement-related noise problems. Electromagnetic Interference (EMI) radiating from PC traces or unshielded inductors can be picked up by the scope ground lead and appear as transient spikes. With many types of probes, this problem can be distinguished from real noise by disconnecting the ground lead, removing the probe tip cover, and touching the ground ring near the tip directly to the filter-cap ground lead (Figure 2).

If induced ground noise is the problem, protect sensitive circuitry by locating it physically distant from the DC-DC converter and placing a 0.1µF to 1µF ceramic capacitor across the supply leads close to the sensitive circuitry. That way, the long PC traces carrying power will exhibit some inductance, and the combination of the main capacitor, local bypass capacitor, and lead inductance act as a pi filter.

MAXIM
100µH Toroid Inductor

General Description

The MAXL001 is a 100µH inductor designed as the main magnetic component for simple flyback DC-DC converters with up to 3W output. Quieter than bobbin inductors and less costly than Molypermalloy Powder (MPP) or pot-core inductors, the MAXL001 is ideal for distributed power supplies and portable equipment. The MAXL001 core material is an iron-powder compound selected for good circuit efficiency at switching frequencies up to 200kHz. The MAXL001 has radial leads for Printed-Circuit (PC) board mounting.

Features

- ♦ **Low Electromagnetic Interference**
- ♦ **Toroid Construction**
- ♦ **Low-Cost, Iron-Powder Core**
- ♦ **200kHz Operation**
- ♦ **1.75A Saturation Current**
- ♦ **0.08Ω DC Resistance**

Applications

Switching Regulators
DC-DC Converters
Power Supplies
DC Filters

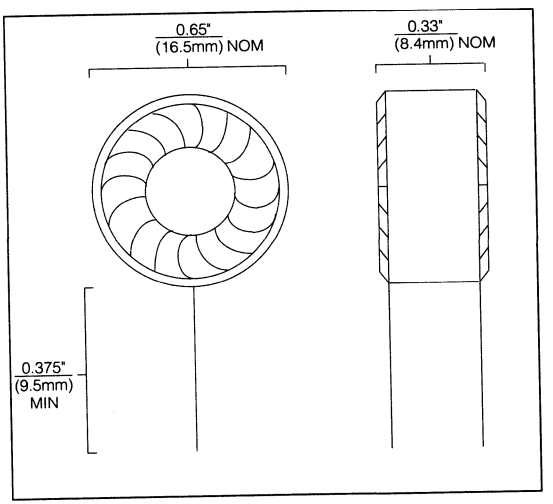
Ordering Information

PART	TEMP. RANGE	VALUE
MAXL001	-55°C to +105°C	100µH ±15%

Physical Characteristics

Diameter	0.65" (16.5mm) Nominal 0.7" (17.8mm) Max
Width	0.33" (8.4mm) Nominal 0.375" (9.5mm) Max
Lead Length	0.375" (9.5mm) Min 26 AWG
Lead Spacing	0.33" (8.4mm) Nominal
Tape	3M #27 or Equivalent
Finish	Saturated with Varnish

MAXL001 PC-Mount Toroid



100µH Toroid Inductor

ABSOLUTE MAXIMUM RATINGS

Peak Current 5A
DC Current 1.5A
Peak Voltage 100V

Operating Temperature Range ..... -55°C to +105°C
Storage Temperature Range ..... -65°C to +105°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the inductor. These are stress ratings only, and functional operation at these conditions is not implied. Expose to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, Note 1.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Inductance	1kHz	85	100	115	µH
Incremental Current	For a 10% change in inductance		1.75		A
DC Resistance			0.08	0.2	Ω
Q	F=100kHz, $V=0.1V_{RMS}$	22	29		

Note 1: Maxim sample tests these parameters to LTPD = 10.

Applications Information

Flyback Inductors for DC-DC Converters

While designed specifically for the MAX743 dual-output current-mode +5V to ±15V or ±12V converter (Figure 1), the MAXL001 works well for many low-power DC-DC converter applications. The 100µH value is fairly low, so caution must be exercised when connecting the MAXL001 to ICs other than the MAX743; calculate the worst-case peak inductor current using equations from the data sheet to be sure the power-transistor ratings are not exceeded. The MAXL001 works well for the following list of products, especially if the supply voltage is 10V or less.

MAXL001 Compatible DC-DC Converter ICs

STEP UP	INVERTING	STEP DOWN	LOW VOLTAGE	DUAL OUTPUT
MAX630	MAX634	MAX638	MAX654	MAX742
MAX631	MAX635		MAX655	MAX743
MAX632	MAX636		MAX656	
MAX633	MAX637		MAX657	
MAX4193	MAX4391		MAX658	
MAX641			MAX659	
MAX642				
MAX643				

100µH Toroid Inductor

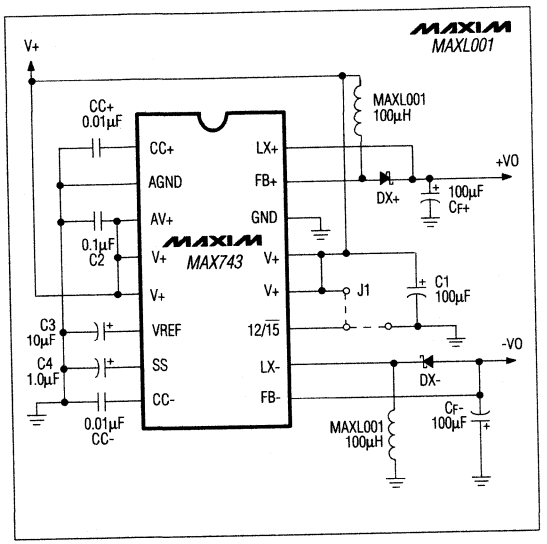


Figure 1. Example Application for MAXL001 (Dual-Output Switching Regulator)

Smaller Inductors: MPP and Pot Core

If cost is not important, consider a MPP toroid inductor such as the 51-559 from Gowanda Electronics, or a miniature surface-mount pot core such as the 41540 from Pico Electronics. Both are much smaller than the MAXL001 and have nearly equal energy storage capabilities.

Gowanda Electronics, Gowanda, NY (716) 532-2234
Pico Electronics, Mt. Vernon, NY (914) 699-5514

MAXIM

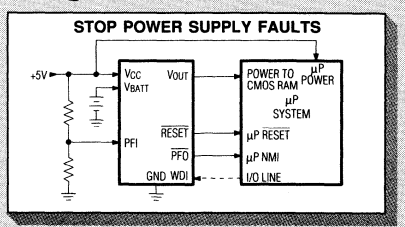
µP Supervisory Circuits

Supervisory ICs Protect μPs Against Power-Supply Failures

Single-Package MAX690 Keeps μPs Running

The MAX690 μP-supervisory IC monitors a microprocessor's environment during power-up, normal operation, and power-down, issuing reset signals as required—particularly when power failures occur. The MAX690 provides four basic housekeeping functions:

- Power-on reset
- Backup-battery switchover
- Power-fail or battery monitoring
- Watchdog timer



The MAX690 guards a μP against supply-voltage failure by providing power-up reset, backup-battery switchover, and power-fail warning. A watchdog timer internal to the MAX690 monitors μP operation.

To provide sufficient reset time for the μPs's internal circuits, the reset output starts out low at power-on and ends 35msec after the supply voltage exceeds 4.65V. If the voltage then falls below a user-selected threshold, the chip issues a power-fail warning that tells the μP to store critical data in a CMOS RAM before the power fails completely. If a further decline brings VCC within 50mV of the backup-battery voltage, the MAX690 connects the battery to power the CMOS RAM.

The MAX690 accommodates systems that employ a 35msec Reset pulse and a ±5% power supply tolerance. If the supply tolerance is ±10%, the MAX692 provides a 4.4V trip threshold. And for newer Intel and Motorola μPs that require a longer Reset pulse, the MAX694 offers a pulse of 140msec.

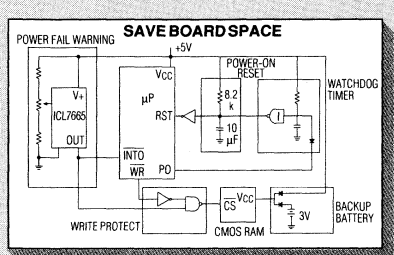
Multi-Function Supervisor Replaces More Than 15 Components

MAX691 Adds Write Protection and Adjustable-Width Resets

The MAX691 saves board space and eliminates time-consuming analog design by replacing at least 15 discrete packages with a single device.

The MAX691 accommodates the reset requirements of different processors by issuing adjustable-width Reset pulses. The default width (35msec) suits fast μPs, but the pulse can be lengthened for other processors by connecting an external capacitor. The MAX691 also issues a Reset when the supply declines to 4.65V for 5V, ±5% tolerance supplies. For a ±10% supply tolerance, the MAX693 issues Resets at 4.4V. The MAX693 has a 35msec default reset pulse width, while the MAX695 defaults to 140msec.

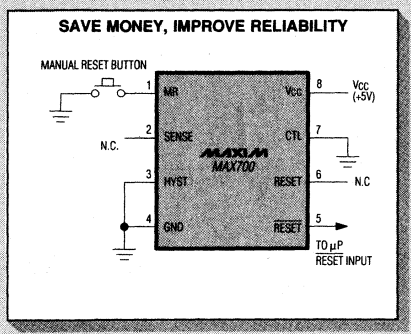
The chip contains an uncommitted 1.3V comparator that warns a system of impending power loss, initiating an orderly μP shutdown. Finally, an on-board write-protect function precludes the μP from storing erroneous data in RAM during power-up, power-down, brownouts, or momentary power interruptions.



The MAX691 replaces a circuit of more than 15 components.

Only 200µA Powers 8-Pin µP Supervisors

Low-Cost MAX700-702s are Ideal for Portable Equipment



The MAX700-702 supervisory ICs lower cost and increase reliability in 5V systems by eliminating external components and adjustments otherwise required for housekeeping functions.

MAX700-702 supervisory circuits offer the simplest and most reliable way to monitor power-supply voltage in a digital or µP system. They are ideal for portable instruments: Supply current is 200µA max, and no external components are required for monitoring 5V systems. All parts are available in space-saving 8-pin DIP and SO packages.

They provide 200ms RESET and $\overline{\text{RESET}}$ pulses on power-up, power-down, and during low-voltage brownout conditions (the MAX702 issues RESET only). Reset pulses can also be triggered by a debounced manual reset input available on each device.

The MAX700 has a preset voltage threshold of 4.65V, but is able to monitor other thresholds as well. Hysteresis can be added with one resistor to minimize switching noise when monitoring slowly-moving voltages.

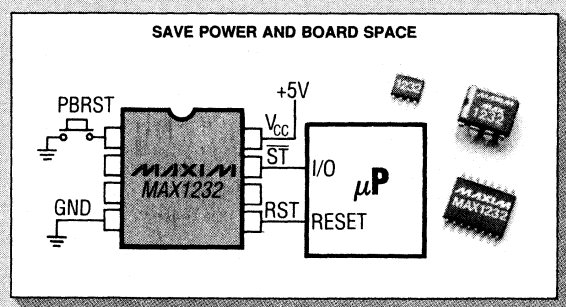
Pin-Compatible DS1232 Upgrade Needs 1/3 the Space and 1/10th the Power

New MAX1232 Available in 8-Pin SO

Maxim's MAX1232 µP supervisor is supplied in an 8-pin surface mount package for space intensive applications and in standard 8-pin DIPs and 16-pin SO packages as a pin-compatible upgrade for the DS1232. What's more, the MAX1232's 50µA supply current is only 1/10th that of the DS1232.

The MAX1232 enhances the reliability of a µP system by monitoring its supply voltage and software execution. The device requires no external components.

The voltage-trip threshold is digitally selected for ±5% or ±10% supply tolerance systems. The chip issues 250msec reset pulses on power-up, power-down, and low-voltage brownout conditions. A debounced manual-reset input initiates reset pulses as well. A watchdog timer, digitally programmed for timeouts of 150msec, 600msec, or 1.2sec, monitors software execution.



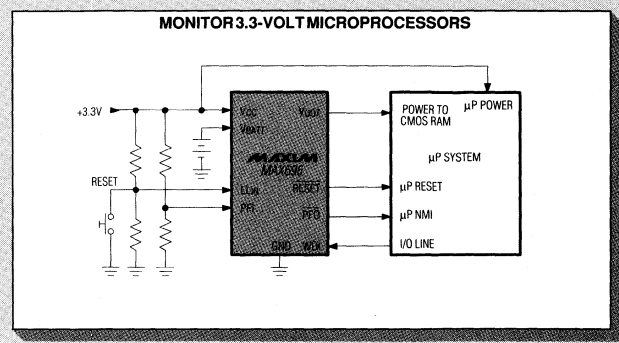
The MAX1232 requires only 1/10th the power of the DS1232 and 1/3 the board space.

+3.3-Volt Microprocessors Are Now Easily Monitored

µP-Supervisor ICs Have Adjustable Threshold

The MAX696/697 offer fully adjustable reset thresholds. Two external resistors, connected to the LL_{IN} (Low Line In) terminal, let you set the threshold as required. Other Maxim ICs are preset to standard 4.4V or 4.65V level. In a 9V battery-powered system, for example, you can reset the µP at a desired battery-discharge level rather than waiting for the regulated 5V to drop out.

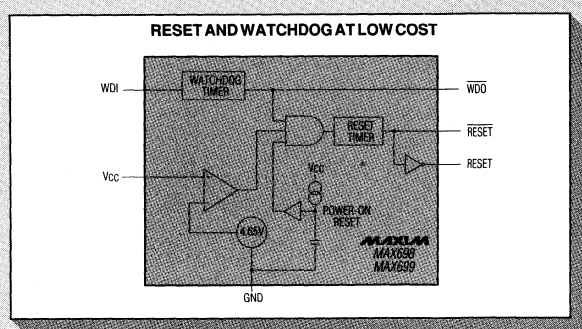
The MAX697 offers both low quiescent current (160µA), useful in low-power applications, and write protection for safeguarding the integrity of non-volatile RAM.



The MAX696 monitors +3.3V microprocessors with four supervisory functions: reset, adjustable reset threshold, watchdog timing, and power fail warning.

Watchdog Monitor and Reset Generator Combined in Single Unit

Economical IC Ideal for Non-Battery Backed Applications



The MAX699 supervisor IC provides reset and watchdog functions for applications that don't use backup batteries.

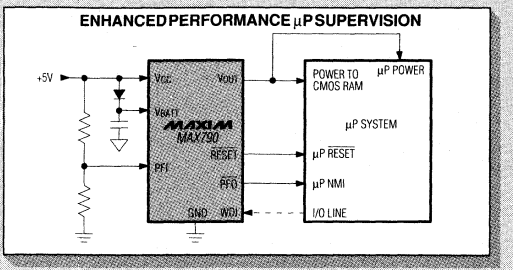
The MAX699 is tailor-made for systems that require only reset and watchdog functions and eliminates all external components and adjustments associated with µP-housekeeping functions. The 8-pin DIP version issues RESET pulses in response to power-up, power-down and brownout conditions; the 16-pin SO version issues positive-going RESETs as well.

The internal watchdog timer monitors software execution on a user-selectable line. A lapse of one second or more triggers a RESET pulse.

µP SUPERVISOR PROVIDES VALID RESETS FOR V_{CC} AS LOW AS 1V

Uses 10x Less Power

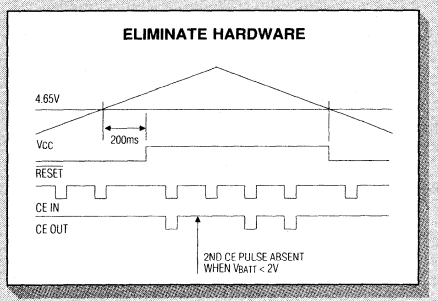
The MAX790 provides all the functions of the pin-compatible MAX690, but with tightened specifications. To prevent a µP from writing to the EEPROM as V_{CC} fails, the chip continues to operate properly and issue valid resets with V_{CC} as low as 1V. Tighter tolerance on the power-fail threshold enables the chip to monitor batteries more closely. And because supply current has been reduced 10 times and the drop from V_{CC} to V_{OUT} has been lowered, the MAX790 provides more output current while dissipating less power.



The MAX790 uses a super-capacitor instead of a backup battery.

STATE-OF-THE-ART µP SUPERVISOR WARNS OF BOTH MAIN AND BACKUP SUPPLY FAILURES

Supports More RAM with 25mA Backup Current



The MAX791 monitors the backup battery without extra hardware or battery connections. When the battery is low, the second CE pulse is suppressed.

The MAX791 offers the most complete µP supervision available in a single IC. Separate on-chip monitors warn both when the main +5V power line starts to fail, and when the backup-battery voltage is low. Though similar to the MAX691, the MAX791 offers more functions, improved specs and draws less than one tenth as much supply current.

Propagation delay for the gated chip-enable switch has been reduced to 10nsec, allowing supervision of faster memories without external gates. Increased output current at V_{BATT} (25mA) allows the device to support more RAM in the backup mode. Maximum output current during normal operation is 250mA.

Separate watchdog and reset outputs let you determine whether a fault was caused by a software glitch or a power failure.

COMPLETE ONE-CHIP BATTERY MANAGEMENT

MAX1259 Consumes 70% Less Power Than the DS1259

The MAX1259 battery-management chip, pin-compatible with the DS1259, supplies more output current, yet consumes 70% less power. The Maxim part monitors the backup battery, warns of impending power failures, and switches the memory to the battery when failures occur.

The MAX1259 eliminates oscillation and increased IBATT during switchover. Clean switchover and low power consumption make the MAX1259 attractive for portable instrument applications and as a safeguard for non-volatile memories.

MAX690-MAX1232 Functions	690	691	692	693	694	695	696	697	698	699	700	701	702	790††	791††	MAX1232	MAX1259
Fixed Power Up/ Down Reset	✔	✔	✔	✔	✔	✔			✔	✔	✔	✔	✔	✔	✔	✔	
Variable Power Up/ Down Reset							✔	✔			✔						
Battery Backup Switching	✔	✔	✔	✔	✔	✔	✔							✔	✔		✔
Watchdog Timer	✔	✔	✔	✔	✔	✔	✔	✔		✔				✔	✔	✔	
Programmable Watchdog Period		✔		✔		✔	✔	✔							✔	✔	
Power Fail Warning	✔	✔	✔	✔	✔	✔	✔	✔						✔	✔		✔
Write Protect		✔		✔		✔		✔							✔		
Reset Threshold (V)	4.65	4.65	4.4	4.4	4.65	4.65	>1.3	>1.3	4.65	4.65	4.65/adj.	4.65	4.65	4.65	4.65/adj.	4.37/4.62	
Reset Pulse Width (ms)	35	35/adj	35	35/adj	140	140/adj	35/adj	35/adj	140	140	200	200	200			250	
Price (1000-up) ($)†	3.33	3.61	3.33	3.61	3.33	3.61	3.55	3.58	1.88	2.13	2.24	1.96	1.71	†	†	1.89	†

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

A Guide For Providing Reliable Microprocessor Supervision

Introduction

Maxim's microprocessor supervisory circuits contain versatile analog and digital functions that save considerable design effort and development time. The parts may seem unglamorous, but they perform most of the "messy" housekeeping functions required by microprocessors. These functions are vital to µP systems because they include safeguards against electrical failure. Some functions are included in the newer µPs, but these µPs cannot always diagnose their own failures. To be effective and reliable, the monitor circuitry must reside in an external supervisory chip.

Microprocessor-supervisory functions include:

- Power-on reset
- Low-voltage reset for glitch and brownout
- Memory write-protection
- Power-fail warning
- Battery backup switchover
- Watchdog timer

These functions are not difficult to implement individually. But integrating them as a coherent whole, fully thought out and debugged, presents a formidable challenge—especially if space is critical. The following review of these supervisory functions shows their relation to the overall microprocessor system.

Power-On Reset

When you apply power to a microprocessor, the internal registers "come up" in arbitrary states that contain random data. Applying a reset command to the µP overcomes this chaos by resetting all internal circuits at a predictable starting point. To insure a proper startup, you must hold the RESET input low for 20 to 120 milliseconds, depending on the µP.

Though relatively simple, the external reset-timer circuit must keep the RESET signal low while the supply voltage (V_{CC}) is below the minimum level allowed for µP operation. During startup, for instance, the circuit initiates a reset-delay interval only when V_{CC} reaches that minimum level. If the timed interval begins early (at too low a voltage) or ends too soon, the reset may be overridden by arbitrary states in the digital circuitry while supply voltage is rising toward the minimum operating level. Reset-timer circuits therefore require a timer, a comparator, an accurate voltage reference, and a suitable means for driving the µP's RESET input.

Low-Voltage (Glitch/Brownout) Reset

Once operating, a µP should continue as long as V_{CC} remains within its specification. But to ensure reliable operation, the system must also monitor V_{CC} for undervoltage—both short term "glitches" and longer-term "brownouts." These undervoltage conditions are seldom destructive, but they can cause unpredictable operation that leads to a "crash." During a crash the computer loses its "mind" in a manner that no programming genius can cure. The µP cannot be trusted to control its own reset, so the most reliable remedy is to reset it with a signal that originates automatically in an external device.

The Low-Voltage and Power-On sections of a Maxim supervisory IC share the same precision voltage-sensing circuit, and they respond when V_{CC} goes low. When V_{CC} returns to normal, the RESET output remains low for a timed delay interval as it does following power-on.

Memory-Write Protection

Crashes are bad, but they can lead to a potentially worse problem—during the crash the µP may write "garbage" into its permanent (non-volatile) memory, causing data and program losses that cannot be restored by a subsequent reset. To prevent these losses, the system must intercept and disable the memory's chip-enable signal (CE) during a supply-voltage glitch or brownout: Simply apply the CE signal and the low-voltage comparator output to a gate whose output drives the memory's CE input. But no ordinary gate will do; this one must operate reliably with V_{CC} as low as 2 volts.

Power-Fail Warning

Reliable protection may require more than low-voltage detection and reset; an orderly shutdown may require other actions prior to the reset. The processor, for instance, may need to store its register contents in a non-volatile memory such as battery-backed CMOS RAM.

It may seem impossible to specify a preventive action before the low-voltage condition occurs, but power-supply regulators operate in a way that makes this possible. Regulators have large input filter capacitors, which, in a typical 5V supply, charge to between 8 and 10 volts. This charge enables the regulator to continue operating for 50 to 100msec after the primary power is lost—until the capacitor discharges to about 6.5V (or less, for low-dropout regulators).

You can generate an early warning by monitoring the filter-capacitor voltage with the Power Fail In (PFI) input of a Maxim supervisor chip. When the unregulated voltage falls below, say, 7.5 volts, the chip's internal comparator issues a Power Fail Out signal (PFO), which allows sufficient time for µP house-cleaning chores before the system initiates a reset.

PFO normally connects to the µP's non-maskable-interrupt input to ensure top-priority treatment. In the super-

A Guide For Providing Reliable Microprocessor Supervision

visory chip, PFI drives one side of an internal CMOS comparator while a 1.3V reference drives the other. Two external resistors, which divide the capacitor voltage down to the 1.3V PFI threshold, let you set the comparator's trip point for any desired filter-capacitor voltage.

Battery-Backup Switchover

CMOS RAM is normally powered by the µP's 5V supply. When connected to a 3V battery in the shutdown or backup mode, the RAM retains its contents while consuming very little power. Backup batteries can be small because the memory's current drain—several milliamperes in normal operation—drops to a few microamperes in the backup mode.

The circuit that switches RAM from main supply to the battery must then "stay awake" to switch it back. Like the RAM, this circuit depends on the battery and therefore must operate on microamperes. Besides low power consumption, the circuit must exhibit reliable operation at low supply voltage as the backup battery discharges. The same is true for reset and write-protect circuits, which remain active in the backup mode.

Watchdog

Software is usually written as a series of modules interconnected in a continuous loop. During execution, an unforeseen sequence of events can sometimes cause the program to stall within one module, endlessly performing some useless (or possibly harmful) function. A "watchdog" is a timer circuit that monitors this program execution and issues a reset command when the stall condition appears.

To use the watchdog, you connect a port of the µP to the timer-reset input of the free-running watchdog circuit, and configure the software to write data to this port several times a second. Because it interprets missing instructions as a software problem, the watchdog issues a system reset whenever it times out before receiving the next write instruction.

The optimum timeout depends on the system's hardware as well as its software. A longer period at powerup, for instance, gives the microprocessor extra time to initialize the system before starting the main software loop. And in some systems, the watchdog is activated only for certain operations.

Most of these supervisory functions can be implemented with little difficulty using standard analog components. The trick is to squeeze them into half a square inch of board space, avoid trims, and not get overrun with discrete external components. Maxim's MAX690 family of supervisory ICs does just that. The family includes a variety of feature combinations that accomodate most µP-system requirements. Table 1 summarizes these features.

Default and Adjustable Features

Most µP-supervisor requirements can be satisfied by the MAX690, which has nearly everything (see Table 1). It offers small size, no external parts, and the most commonly specified, factory-trimmed power-supply thresholds, watchdog times, and reset times. More complex applications, however, may require different default values, adjustable values, or other inputs and outputs.

The MAX690 issues a reset of 35msec minimum on powerup and in response to brownouts and glitches (i.e., whenever V_{CC} falls below the 4.65V limit). Available in an 8-pin DIP, the device provides battery-backup switchover, power-fail warning, and a 1.6sec watchdog timer.

Other devices offer different combinations of functions and parameter values.

Reset

Because a voltage divider external to the MAX696 and MAX697 determines the V_{CC} level at which these devices issue a reset, they can monitor 3V, 5V, or any other unusual supply voltage. All other parts in the MAX690 series (see Table 1) are dedicated to a specific V_{CC} threshold level; for these parts, the level cannot be altered.

Several values of power-on reset delay are available. The MAX690, 691, 692, 693, 696, and 697 have minimum-35msec delays that suit the majority of µPs. The MAX694, 695, 698, and 699 have minimum 140msec delays as required by Motorola and the newer Intel µPs. The MAX700/701/702 offer 200ms delays, and the MAX1232 offers three options: 150msec, 600msec, and 1.2sec. The MAX691, 693, 695, and 697 offer reset periods and watchdog-timer periods that you adjust by varying an external capacitor value or applied clock frequency. Note that supervisor-generated reset delays should always be longer than the µP's required minimum.

In order to distinguish resets caused by undervoltage from those generated by the watchdog timer, the MAX691, 693, 695, 696, 697, and 699 provide separate outputs for the reset and watchdog voltage comparators. A manual-reset input, available on the MAX696, 697, 700, 701, 702 and MAX1232, can sometimes be added to the other devices as well (see below).

Reset

The MAX691, 693, 695, 696, 697, 700, 701 and MAX1232 provide both RESET (active high) and $\overline{\text{RESET}}$ (active low)

Table 1. Microprocessor-Supervisor Features

PART NO.	POWER ON RESET (min)	LOW V_{CC} THRESHOLD	WATCHDOG TIMER	BATTERY BACKUP SWITCHOVER	WRITE PROTECT	POWER FAIL IN/OUT	MANUAL RESET	PINS
MAX690	35 ms.	4.65 V	YES	YES		YES		8
MAX691	35 ms. (1)	4.65 V	YES	YES (2)	YES	YES		16
MAX692	35 ms.	4.4 V	YES	YES		YES		8
MAX693	35 ms. (1)	4.4 V	YES	YES (2)	YES	YES		16
MAX694	140 ms.	4.65 V	YES	YES		YES		8
MAX695	140 ms. (1)	4.65 V	YES	YES (2)	YES	YES		16
MAX696	35 ms.	>1.3V (1)	YES	YES (2)		YES	YES	8
MAX697	35 ms. (1)	>1.3V (1)	YES		YES	YES	YES	16
MAX698	140 ms.	4.65 V						16
MAX699	140 ms. (1)	4.65 V	YES					16
MAX700	200 ms.	4.65 V (1)					YES	8
MAX701	200 ms.	4.65 V					YES	8
MAX702	200 ms.	4.65V					YES	8
MAX1232	250 ms.	4.5 V or 4.75V	YES				YES	8

Notes:
1. Default value shown. These parts are adjustable (see text).
2. Also has BATT ON output pin.

outputs. The Intel 8051 family and similar microprocessors specify an active-high polarity for RESET; the high level also serves as V_{CC} for the internal RAM during battery backup (standby). During battery backup, RESET remains low and RESET remains "high" as long as the battery voltage is above 2.0 volts. "High" in this case is the battery voltage or V_{CC}, whichever is higher. This is a very important specification; it guarantees that the microprocessor will stay reset during the transient (and generally unspecified) conditions that accompany application of power.

Memory-Write Protection

The MAX691, 693, 695, and 697 perform a write-protect function to prevent the system from writing erroneous data into memory during the reset interval.

Power-Fail Warning

The MAX690-697 devices include a power-fail circuit (PFI and PFO) that forewarns the system of an impending power loss and reset.

Battery-Backup Switchover

MAX690-696 devices normally furnish power to the CMOS RAM by connecting V_{CC} to OUT. When V_{CC} drops below the battery voltage, OUT is connected to V_{BATT}, placing the MAX690-696 in standby mode to conserve battery power. RESET, $\overline{\text{RESET}}$, LO LINE, BATT ON, WDO, PFO, and CE OUT remain active (high or low, as specified) and CE IN, PFI, and WDI are disconnected. In battery backup mode the "high" logic state is equal to the backup-battery voltage. Total current through the MAX690-696 is reduced to less than 1µA.

Watchdog

Watchdog circuits in the MAX691, 693, 695, 696 and 697 provide several ways to adjust the time-out intervals that follow reset. You can select between preset intervals of 1.6sec and 100msec. If you select the shorter interval (100msec) it will affect the watchdog intervals only; reset intervals will remain at 1.6sec. To disable the watchdog timer, either connect its input (WDI) to 1/2V_{CC} or leave it floating.

To set a custom timeout interval by altering the internal-oscillator frequency (10.24kHz nominal), connect an external capacitor or an external clock signal to the OSC IN terminal. Watchdog and reset timers in these devices share the internal oscillator, so any adjustment of oscillator frequency affects both functions.

A Guide For Providing Reliable Microprocessor Supervision

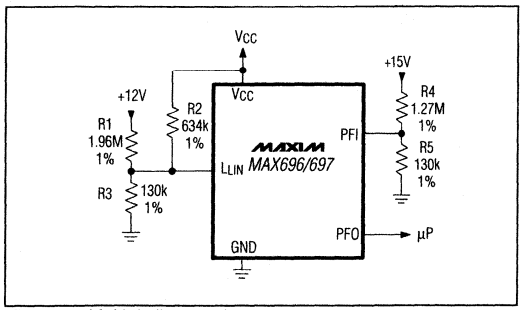


Figure 1. Multiple line monitor.

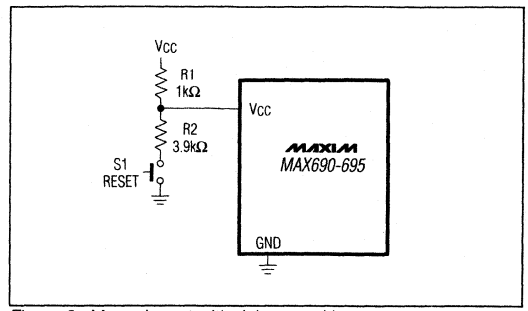


Figure 2. Manual reset with debounced input.

Additional Features

Monitoring Multiple Power Supplies

Both the power-fail circuit and the low-line input (L_{LIN}) of MAX696 and MAX697 devices can monitor multiple power supplies (Figure 1). Low leakage into these CMOS inputs allows use of high-resistance voltage dividers that draw little current from their sources—an advantage when monitoring a backup battery.

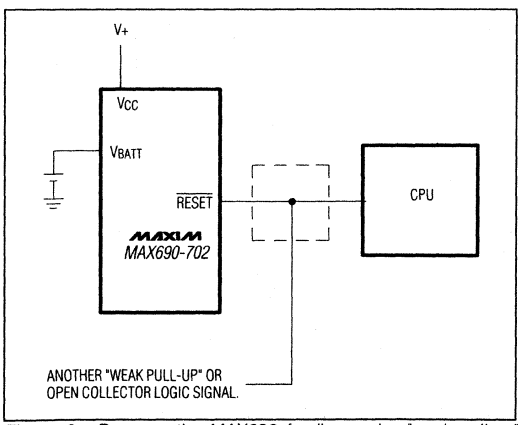


Figure 3. Because the MAX690 family employ "weak pull-up" outputs, they can be connected to form a "wired NOR" gate, thus saving an extra component.

Adding Manual Reset

Adding this circuit to a MAX690-695 device provides all the normal reset delays plus a manual reset with debounced input (Figure 2).

Paralleled NOR Outputs

The MAX691, MAX693, MAX695, MAX696, MAX697, and MAX698 have unusual output structures that allow them to be paralleled with other logic as a "wired-NOR" gate, or used with an external pull-up resistor to V_{OUT}, to drive higher current loads. To perform this, the $\overline{RESET}$ and RESET lines employ a "weak pull-up". When they are high, they source only 1µA (saving power consumption), but they can sink more than a milliamp to ground when low. Thus, if two of these outputs are connected and one is pulled low, the other will be pulled low.

MAXIM
MAX1232 Microprocessor Monitor

General Description

The MAX1232 microprocessor (µP) supervisory circuit provides µP "housekeeping" and power-supply supervision functions while consuming only 1/10th the power of the DS1232. The MAX1232 enhances circuit reliability in µP systems by monitoring the power supply, monitoring software execution, and providing a debounced manual reset input. The MAX1232 is a plug-in upgrade of the Dallas DS1232.

A reset pulse of at least 250ms duration is supplied on power-up, power-down, and low-voltage brown-out conditions (5% or 10% supply tolerances can be selected digitally). Also featured is a debounced manual reset input that forces the reset outputs to their active states for a minimum of 250ms. A digitally-programmable watchdog timer monitors software execution and can be programmed for timeout settings of 150ms, 600ms, or 1.2sec. The MAX1232 requires no external components.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Features

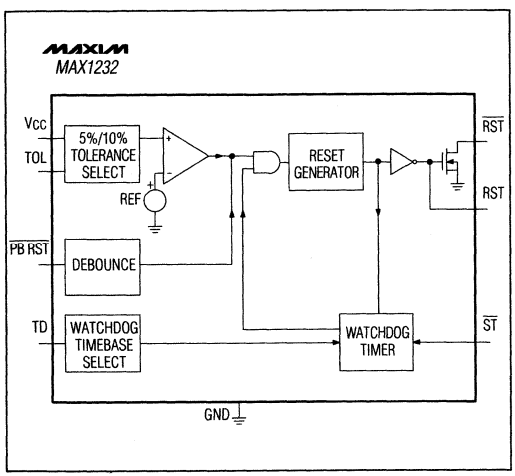
- **Consumes 1/10th the Power of the DS1232**
- **Precision Voltage Monitor - Adjustable +4.5V or +4.75V**
- **Power OK/Reset Pulse Width - 250ms Min**
- **No External Components**
- **Adjustable Watchdog Timer - 150ms, 600ms, or 1.2sec**
- **Debounced Manual Reset Input for External Overide**
- **Available in 8-pin DIP/Small Outline and 16-pin Wide Small Outline Packages**

Ordering Information

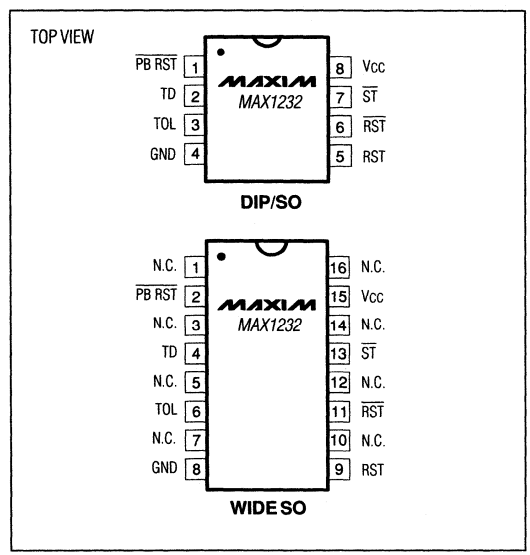
PART	TEMP. RANGE	PIN-PACKAGE
MAX1232CPA	0°C to +70°C	8 Plastic DIP
MAX1232CSA	0°C to +70°C	8 SO
MAX1232CWE	0°C to +70°C	16 Wide SO
MAX1232C/D	0°C to +70°C	Dice*
MAX1232EPA	-40°C to +85°C	8 Plastic DIP
MAX1232ESA	-40°C to +85°C	8 SO
MAX1232EWE	-40°C to +85°C	16 Wide SO
MAX1232MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Block Diagram



Pin Configuration



5

MAX1232 Microprocessor Monitor

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin (with respect to GND) ..... -1V to +7V
Operating Temperature Ranges:
MAX1232C_ _ ..... 0°C to +70°C
MAX1232E_ _ ..... -40°C to +85°C
MAX1232M_ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level (Note 1)	V_{IH}		2.0		V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}		-0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}; V_{CC} = +4.5V to +5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage $\overline{ST}$, TOL	I_{IL}		-1.0		+1.0	µA
Output Current RST	I_{OH}	V_{OH} = 2.4V	-1.0	-12		mA
Output Current RST, $\overline{RST}$	I_{OL}	V_{OL} = 0.4V	2.0	10		mA
Operating Current (Note 2)	I_{CC}			50	200	µA
V_{CC} 5% Trip Point (Note 3)	V_{CCTP}	TOL = GND	4.50	4.62	4.74	V
V_{CC} 10% Trip Point (Note 3)	V_{CCTP}	TOL = V_{CC}	4.25	4.37	4.49	V

CAPACITANCE (Note 4)

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance $\overline{ST}$, TOL	C_{IN}				5	pF
Output Capacitance RST, $\overline{RST}$	C_{OUT}				7	pF

A.C. ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}; V_{CC} = +5V to ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{PB\ RST}$ (Note 5)	t_{PB}	Figure 3	20			ms
$\overline{PB\ RST}$ Delay	t_{PBD}	Figure 3	1	4	20	ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	Figure 4	75			ns
$\overline{ST}$ Timeout Period	t_{TD}	Figure 4 TD pin = 0V	62.5	150	250	ms
		TD pin = open	250	600	1000	
		TD pin = V_{CC}	500	1200	2000	
V_{CC} Fall Time (Note 4)	t_F	Figure 5	10			µs
V_{CC} Rise Time (Note 4)	t_R	Figure 6	0			µs
V_{CC} Detect to RST High and $\overline{RST}$ Low	t_{RPD}	Figure 7, V_{CC} falling			100	ns
V_{CC} Detect to RST Low and $\overline{RST}$ Open (Note 6)	t_{RPU}	Figure 8, V_{CC} rising	250	610	1000	ms

Note 1: $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40kΩ.
Note 2: Measured with outputs open.
Note 3: All voltages referenced to GND.
Note 4: Guaranteed by design.
Note 5: $\overline{PB\ RST}$ must be held low for a minimum of 20ms to guarantee a reset.
Note 6: t_R = 5µs.

MAX1232 Microprocessor Monitor

Pin Description

NAME	FUNCTION
$\overline{\text{PB RST}}$	Pushbutton Reset Input. A debounced active-low input that ignores pulses less than 1ms in duration and is guaranteed to recognize inputs of 20ms or greater.
TD	Time Delay Set. The watchdog timebase select input (t_{TD} = 150ms for TD = 0V, t_{TD} = 600ms for TD = open, t_{TD} = 1.2sec for TD = V_{CC}).
TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
GND	Ground
RST	Reset Output (Active High) - goes active: 1. If V_{CC} falls below the selected reset voltage threshold 2. If $\overline{\text{PB RST}}$ is forced low 3. If $\overline{\text{ST}}$ is not strobed within the minimum timeout period 4. During power-up
$\overline{\text{RST}}$	Reset Output (Active Low, Open Drain) - see RST.
$\overline{\text{ST}}$	Strobe Input. Input for watchdog timer.
V_{CC}	The +5V Power-Supply Input
N.C.	No Connect

Detailed Description

Power Monitor

A voltage detector monitors V_{CC} and holds the reset outputs (RST and $\overline{\text{RST}}$) in their active states whenever V_{CC} is below the selected 5% or 10% tolerance (4.62V or 4.37V typically). To select the 5% level, connect TOL to ground. To select the 10% level, connect TOL to V_{CC}. The reset outputs will remain in their active states until V_{CC} has been continuously in-tolerance for a minimum of 250ms (the reset active time) to allow the power supply and µP to stabilize.

The RST output both sinks and sources current, while the $\overline{\text{RST}}$ output, an open-drain MOSFET, sinks current only and must be pulled high.

Pushbutton Reset Input

The MAX1232's debounced manual reset input ($\overline{\text{PB RST}}$) manually forces the reset outputs into their active states. The reset outputs go active after $\overline{\text{PB RST}}$ has been held low for a time t_{PBD}, the pushbutton reset delay time. The reset outputs remain in their active states for a minimum of 250ms after $\overline{\text{PB RST}}$ rises above V_{IH} (Figure 3).

A mechanical pushbutton or an active logic signal can drive the $\overline{\text{PB RST}}$ input. The debounced input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater. The $\overline{\text{PB RST}}$ input has an internal pull-up to V_{CC} of about 100µA; therefore, an external pull-up resistor is not necessary.

Watchdog Timer

The µP drives the $\overline{\text{ST}}$ input with an Input/Output (I/O) line. The µP must toggle the $\overline{\text{ST}}$ input within a set period (as determined by TD) to verify proper software execution. If a hardware or software failure keeps $\overline{\text{ST}}$ from toggling within the minimum timeout period – $\overline{\text{ST}}$ is activated only by falling edges (a high-to-low transition) – the MAX1232 reset outputs are forced to their active states for 250ms (Figure 2). This typically initiates the µP's power-up routine. If the interruption continues, new reset pulses are generated each timeout period until $\overline{\text{ST}}$ is strobed. The timeout period is determined by the TD input connection. This timeout period is typically 150ms with TD connected to GND, 600ms with TD floating, or 1200ms with TD connected to V_{CC}.

The software routine that strobes $\overline{\text{ST}}$ is critical. The code must be in a section of software that executes frequently enough so the time between toggles is less than the watchdog timeout period. One common technique controls the µP I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

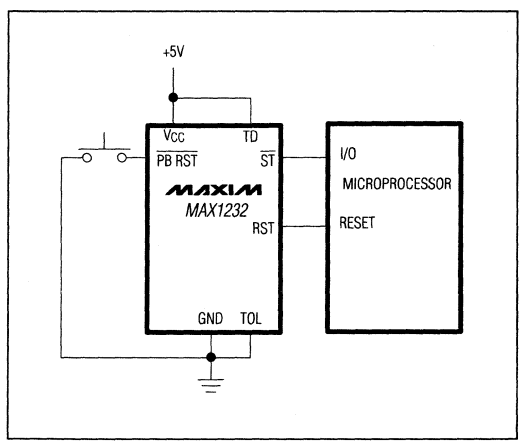


Figure 1. Pushbutton Reset

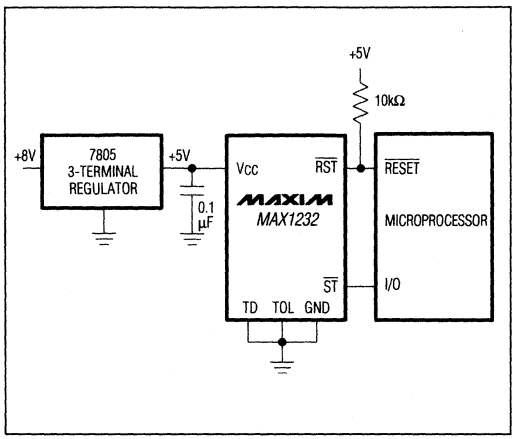
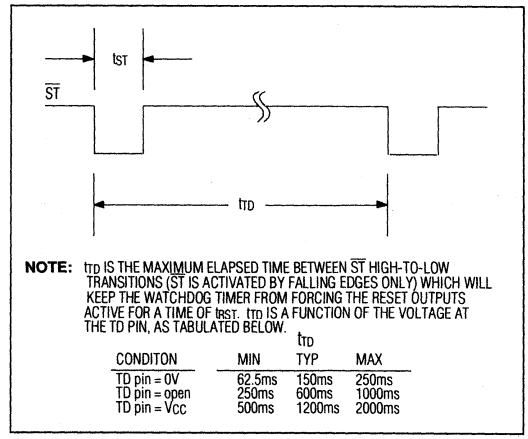


Figure 2. Watchdog Timer



NOTE: tTD IS THE MAXIMUM ELAPSED TIME BETWEEN ST HIGH-TO-LOW TRANSITIONS (ST IS ACTIVATED BY FALLING EDGES ONLY) WHICH WILL KEEP THE WATCHDOG TIMER FROM FORCING THE RESET OUTPUTS ACTIVE FOR A TIME OF tRST. tTD IS A FUNCTION OF THE VOLTAGE AT THE TD PIN, AS TABULATED BELOW.

CONDITON	MIN	tTD TYP	MAX
TD pin = 0V	62.5ms	150ms	250ms
TD pin = open	250ms	600ms	1000ms
TD pin = Vcc	500ms	1200ms	2000ms

Figure 4. Watchdog Strobe Input

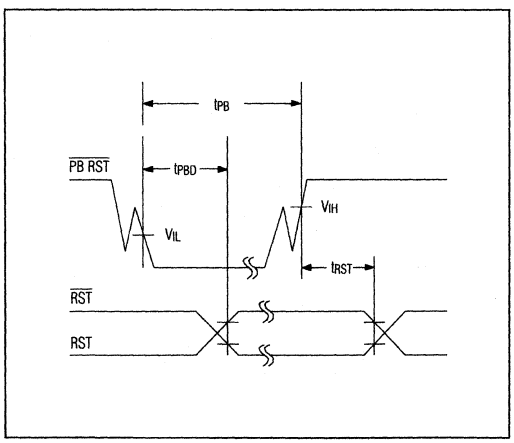


Figure 3. Pushbutton Reset. The debounced PB RST input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater.

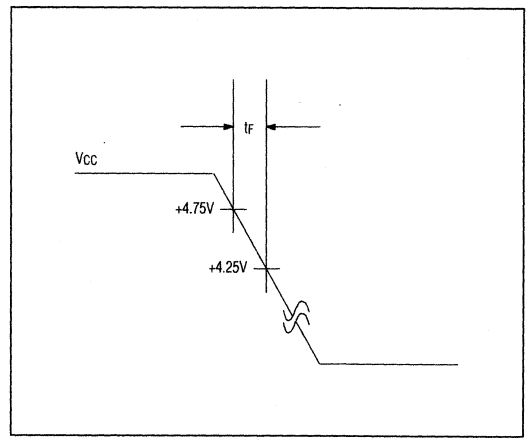


Figure 5. Power-Down Slew Rate

MAX1232 Microprocessor Monitor

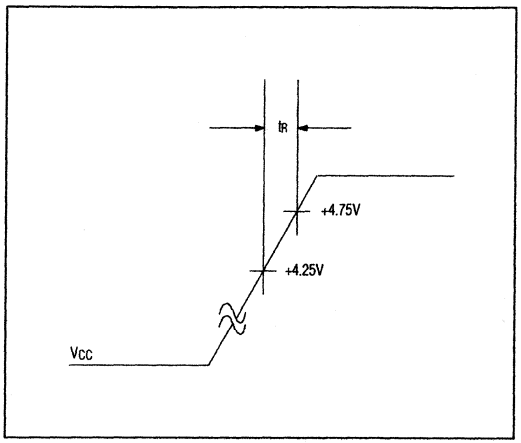


Figure 6. Power-Up Slew Rate

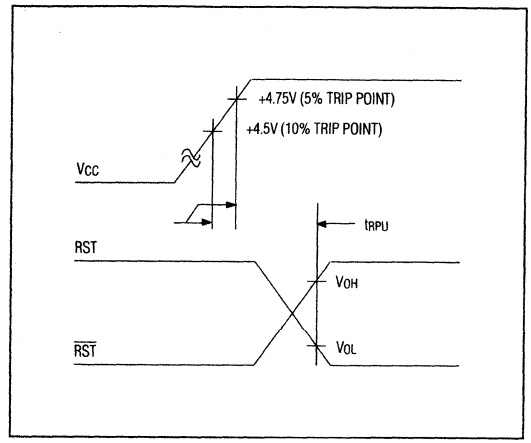


Figure 8. V_{CC} Detect Reset Output Delay (Power-Up)

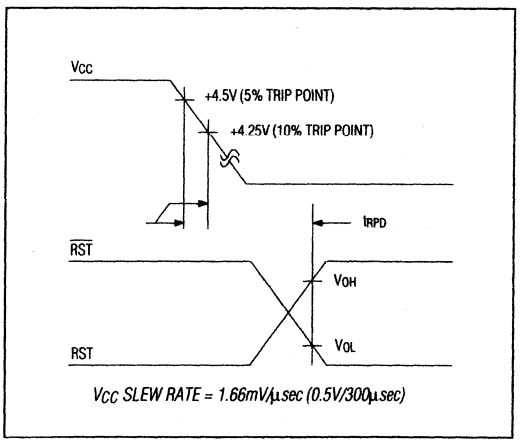
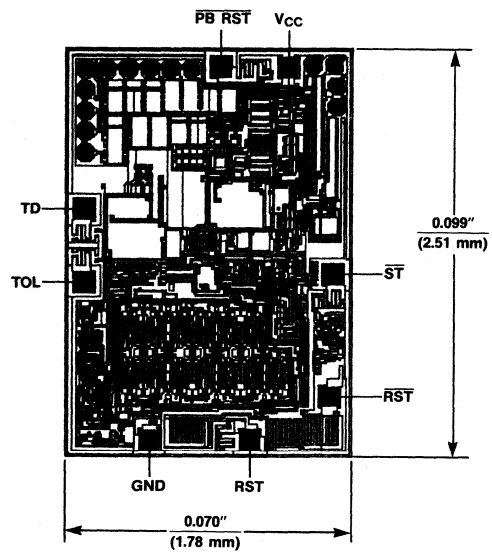


Figure 7. V_{CC} Detect Reset Output Delay (Power-Down)

Chip Topography



ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

MAX1259 Battery Manager

General Description

The MAX1259 battery manager provides backup-battery switching for CMOS RAM, microprocessors, or other low-power logic ICs. It automatically switches to the backup battery when the primary power supply is interrupted. Low-loss switches guarantee an input-to-output differential of only 200mV while supplying 250mA from the primary power supply or 15mA from the battery.

Battery discharge during shipping does not occur in the MAX1259, since the backup battery can be disconnected by strobing the RST input.

A battery-failure output signal indicates when the backup battery is below +2V, and a power-fail output signal indicates when the primary power supply is low. The MAX1259 monitors the backup battery, warns of impending power failures, and switches the memory to the battery when failures occur. The MAX1259 is pin-compatible with the DS1259, but consumes three times less supply current. Commercial, extended and military temperature range devices are available.

Applications

Battery Backup for CMOS RAM
Uninterruptable Power Supplies
Computers
Controllers
Automotive Systems

Features

- ♦ **Switches to Backup Battery if Power Fails**
- ♦ **Consumes Less than 100nA of Battery Current**
- ♦ **Power-Fail Output Signals Primary Power-Supply Loss**
- ♦ **Battery Monitor Indicates Low Battery**
- ♦ **Battery Can Be Disconnected to Prevent Discharge During Shipping**
- ♦ **Battery Automatically Reconnected when V_{CC} is Applied**
- ♦ **Pin-Compatible with the DS1259**
- ♦ **Supply Current Three Times Lower than DS1259**
- ♦ **Available in Industrial and Military Temperature Ranges**

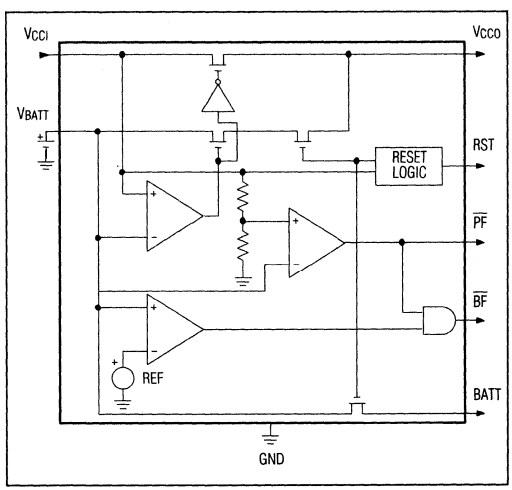
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1259CPE	0°C to +70°C	16 Plastic DIP
MAX1259CWE	0°C to +70°C	16 Wide SO
MAX1259C/W	0°C to +70°C	Dice*
MAX1259EPE	-40°C to +85°C	16 Plastic DIP
MAX1259EWE	-40°C to +85°C	16 Wide SO
MAX1259MJE	-55°C to +125°C	16 CERDIP

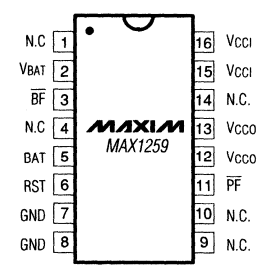
**Contact factory for dice specifications.*

5

Functional Diagram



Pin Configuration



DIP/SO

MAXIM
Microprocessor Supervisory Circuits

General Description

The MAX690 Family of supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 Family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

The MAX690, MAX692 and MAX694 are supplied in 8-pin packages and provide four functions:
1) A Reset output during power-up, power-down and brownout conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MAX691, MAX693 and MAX695 are supplied in 16-pin packages and perform all MAX690/692/694 functions, plus:
1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC}.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

Features

- **Precision Voltage Monitor**
  4.65V in MAX690, MAX691, MAX694 and MAX695
  4.40V in MAX692 and MAX693
- **Power OK/Reset Time Delay – 50, 200ms, or adjustable**
- **Watchdog Timer – 100ms, 1.6 sec, or adjustable**
- **Minimum Component Count**
- **1μA Standby Current**
- **Battery Backup Power Switching**
- **Onboard Gating of Chip Enable Signals**
- **Voltage Monitor for Power Fail or Low Battery Warning**

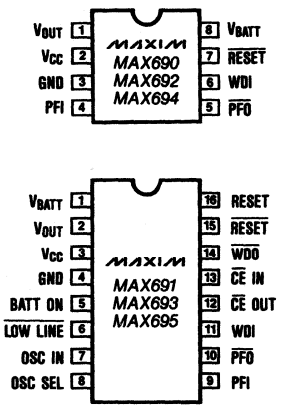
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX690CPA	0°C to +70°C	8 Lead Plastic DIP
MAX690EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX690EJA	−40°C to +85°C	8 Lead CERDIP
MAX690MJA	−55°C to +125°C	8 Lead CERDIP
MAX691C/D	0°C to +70°C	Dice
MAX691CPE	0°C to +70°C	16 Lead Plastic DIP
MAX691CWE	0°C to +70°C	16 Lead Wide SO
MAX691EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX691EJE	−40°C to +85°C	16 Lead CERDIP
MAX691EWE	−40°C to +85°C	16 Lead Wide SO
MAX691MJE	−55°C to +125°C	16 Lead CERDIP

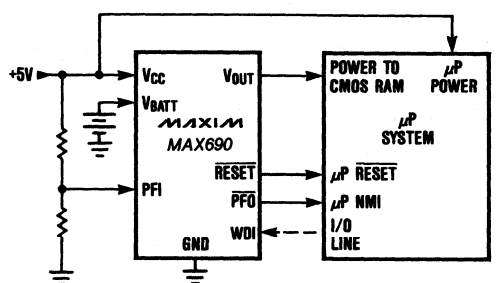
(Ordering information is continued on last page.)

Pin Configuration

Top View



Typical Operating Circuit



MAX690 Typical Application

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... −0.3V to 6.0V
- V_{BATT} ..... −0.3V to 6.0V
- All Other Inputs (Note 1) .. −0.3V to (V_{OUT} +0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/μs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... −40°C to +85°C
- M suffix ..... −55°C to +125°C

Power Dissipation
- 8 Pin Plastic DIP (Derate 5mW/°C above +70°C) 400mW
- 8 Pin CERDIP (Derate 8mW/°C above +85°C) 500mW
- 16 Pin Plastic DIP (Derate 7mW/°C above +70°C) 600mW
- 16 Pin Small Outline (Derate 7mW/°C above +70°C) 600mW
- 16 Pin CERDIP (Derate 10mW/°C above +85°C) 600mW

Storage Temperature Range ..... −65°C to +160°C

Lead Temperature (Soldering, 10 seconds) .... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATTERY BACKUP SWITCHING					
Operating Voltage Range MAX690, MAX691, MAX694, MAX695 V_{CC} MAX690, MAX691, MAX694, MAX695 V_{BATT} MAX692, MAX693 V_{CC} MAX692, MAX693 V_{BATT}		 4.75 2.0 4.5 2.0		 5.5 4.25 5.5 4.0	 V
V_{OUT} Output Voltage	I_{OUT} = 1mA I_{OUT} = 50mA	V_{CC}−0.3 V_{CC}−0.5	V_{CC}−0.1 V_{CC}−0.25		V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250μA, V_{CC} < V_{BATT}−0.2V	V_{BATT}−0.1	V_{BATT}−0.02		V
Supply Current (excludes I_{OUT})	I_{OUT} = 1mA I_{OUT} = 50mA		2 3.5	5 10	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V		0.6	1	μA
Battery Standby Current (+ = Discharge, − = Charge)	5.5V > V_{CC} > V_{BATT}+1V T_A = 25°C T_A = Full Operating Range	 −0.1 −1.0		 +0.02 +0.02	 μA
Battery Switchover Threshold V_{CC} − V_{BATT}	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	I_{SINK} = 3.2mA			0.4	V
BATT ON Output Short Circuit Current	BATT ON = V_{OUT} = 4.5V Sink Current BATT ON = 0V Source Current	 0.5	25 1	 25	mA μA
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	T_A = Full Operating Range MAX690, MAX691, MAX694, MAX695 MAX692, MAX693	 4.5 4.25	 4.65 4.4	 4.75 4.5	 V V

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Threshold Hysteresis			40		mV
Reset Timeout Delay (MAX690/91/92/93)	Figure 6. OSC SEL HIGH, V_{CC} = 5V	35	50	70	ms
Reset Timeout Delay (MAX694/95)	Figure 6. OSC SEL HIGH, V_{CC} = 5V	140	200	280	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V Short Period, V_{CC} = 5V	1.0 70	1.6 100	2.25 140	sec ms
Watchdog Timeout Period, External Clock	Long Period Short Period	3840 768		4097 1025	Clock Cycles
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 0.8V_{CC}	200			ns
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1μA, V_{CC} = 5V	 3.5		0.4	V
RESET and $\overline{WDO}$ Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 1μA, V_{CC} = 5V	 3.5		0.4	V
Output Short Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$	1	3	25	μA
WDI Input Threshold Logic Low Logic High	V_{CC} = 5V (Note 2)	 3.5		0.8	V
WDI Input current	WDI = V_{OUT} WDI = 0V	 −50	20 −15	50	μA
POWER FAIL DETECTOR					
PFI Input Threshold	V_{CC} = +5V, T_A = Full	1.2	1.3	1.4	V
PFI Input Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 1μA	 3.5		0.4	V V
$\overline{PFO}$ Short Circuit Source Current	PFI = 0V, $\overline{PFO}$ = 0V	1	3	25	μA
CHIP ENABLE GATING					
$\overline{CE}$ IN Thresholds	V_{IL} V_{IH}	 3.0		0.8	V
$\overline{CE}$ IN Pullup Current			3		μA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1μA, V_{CC} = 0V	 V_{OUT}−1.5 V_{OUT}−0.05		0.4	V
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		50	200	ns
OSCILLATOR					
OSC IN Input Current			±2		μA
OSC SEL Input Pullup Current			5		μA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX690/ 692/694	MAX691/ 693/695	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	3	4	0V Ground reference for all signals.
$\overline{RESET}$	7	15	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/ 691/694/695, and 4.4V for the MAX692 and MAX693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V, (except 200ms in MAX694/695). $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	5	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
BATT ON	—	5	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	—	6	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET	—	16	RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL	—	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	—	7	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	—	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MAX691, MAX693 and MAX695

A typical connection for the MAX691/693/695 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 25mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT}-700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MAX693). An internal monostable holds $\overline{RESET}$ low for 50ms* after V_{CC} rises above 4.65V (4.4V for MAX693). This prevents repeated toggling of $\overline{RESET}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{RESET}$ must be held low until the microprocessor clock oscillator has started. The MAX690 Family power-up $\overline{RESET}$ pulse lasts 50ms* to allow for this oscillator start-up time. The manual reset switch and the 0.1μF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MAX691/93/95 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output ($\overline{PFO}$) drives the processor's NMI input low. If a Power Fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} fails from 4.8V to 4.65V to save data into RAM. An earlier power fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MAX691/93/95 $\overline{CE}$ OUT line drives the Chip Select inputs of the CMOS RAM. $\overline{CE}$ OUT follows $\overline{CE}$ IN as long as V_{CC} is above the 4.65V (4.4V for MAX693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{CE}$ OUT goes high, independent of the logic level at $\overline{CE}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The LOW LINE output goes low when V_{CC} falls below 4.65V (4.4V for MAX693).

*200ms for MAX695

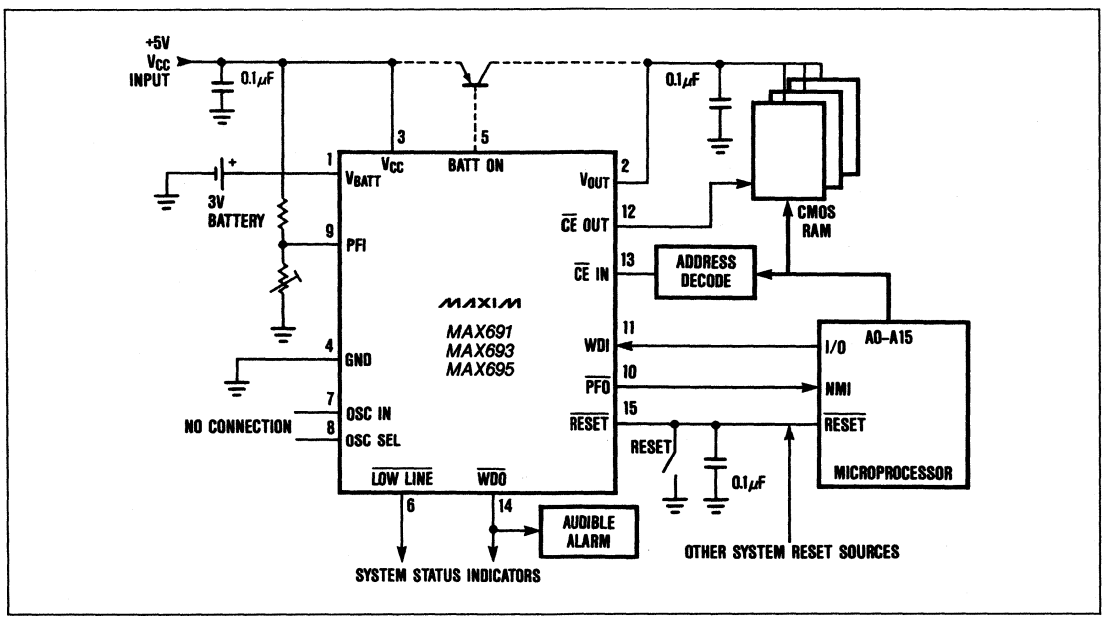


Figure 1. MAX691/693/695 Typical Application

Microprocessor Supervisory Circuits

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled, the MAX691/93 will issue a 50ms* RESET pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new RESET pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once WDO goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MAX690, MAX692 and MAX694

The 8 pin MAX690, MAX692 and MAX694 have most of the features of the MAX691, MAX693 and MAX695.

*200ms for MAX695

Figure 2 shows the MAX690/692/694 in a typical application. Operation is much the same as with the MAX691/693/695 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MAX690/694 RESET output goes low when V_{CC} falls below 4.65V. The RESET output of the MAX692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 50mA. The MAX690/692/694 does not have a BATT ON output to drive an external transistor. The MAX690/92/94 also does not include chip enable gating circuitry that is available on the MAX691/93/95. In many systems though, CE gating is not needed since a low input to the microprocessor RESET line prevents the processor from writing to RAM during power-up and power-down transients.

The MAX690/92/94 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds, a RESET pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left floating.

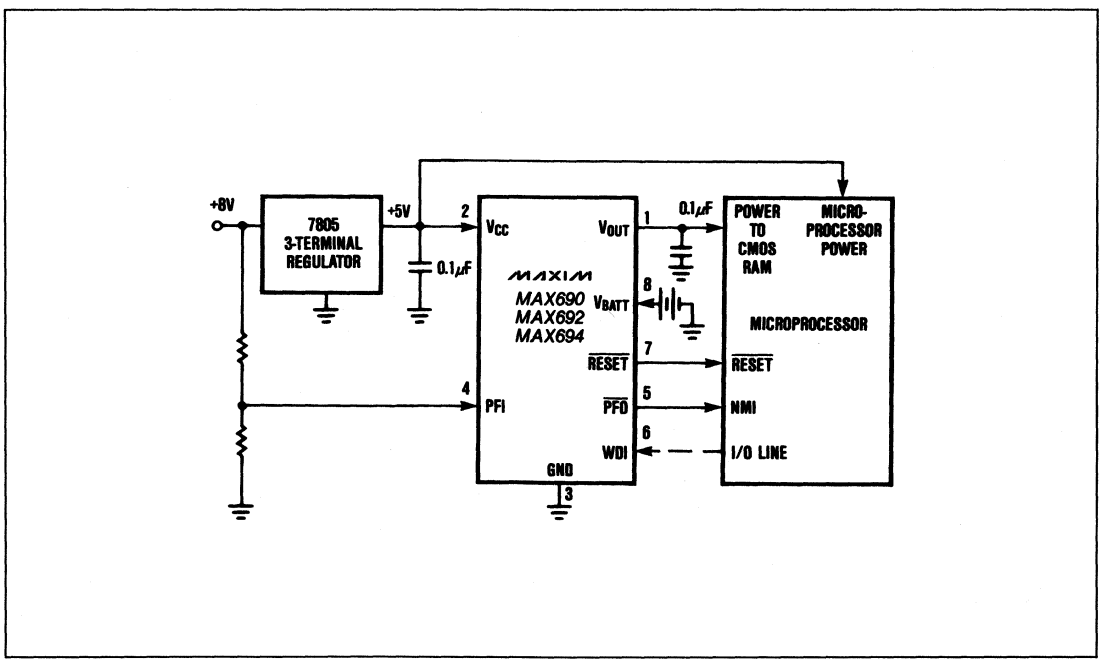


Figure 2. MAX690/692/694 Typical Application

Detailed Description

Battery-Switchover and VOUT

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MAX691/693/695 only) can directly drive the base of the external transistor.

It should be noted that the MAX690/91/92/93/94/95 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} – 700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX690/691/694/695 operates with battery voltages from 2.0V to 4.25V while the MAX692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small charging current of typically 10nA (0.1µA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

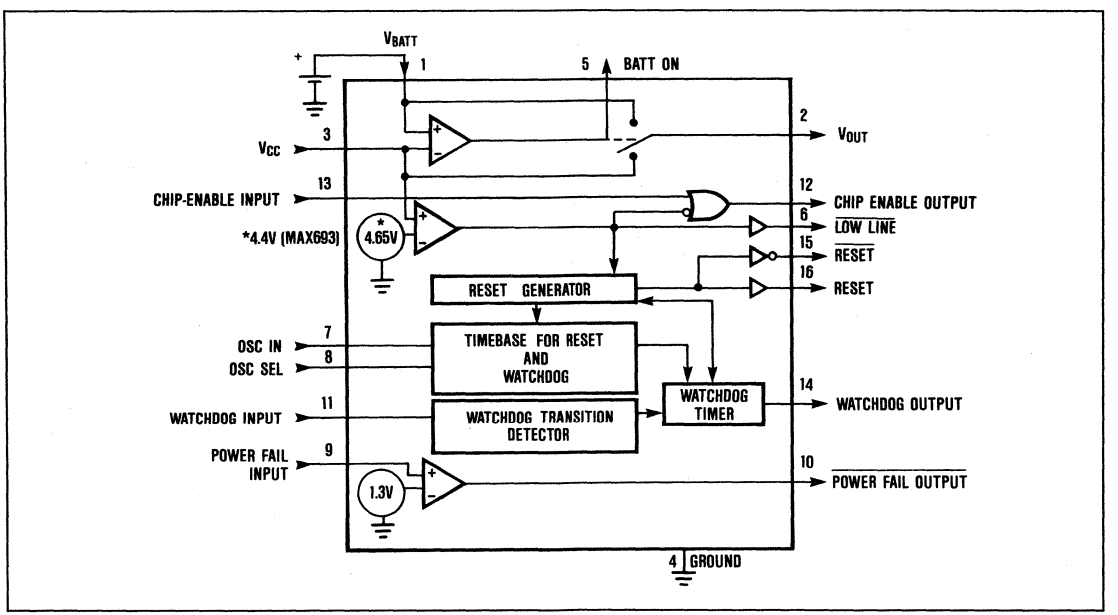


Figure 3. MAX691/693/695 Block Diagram

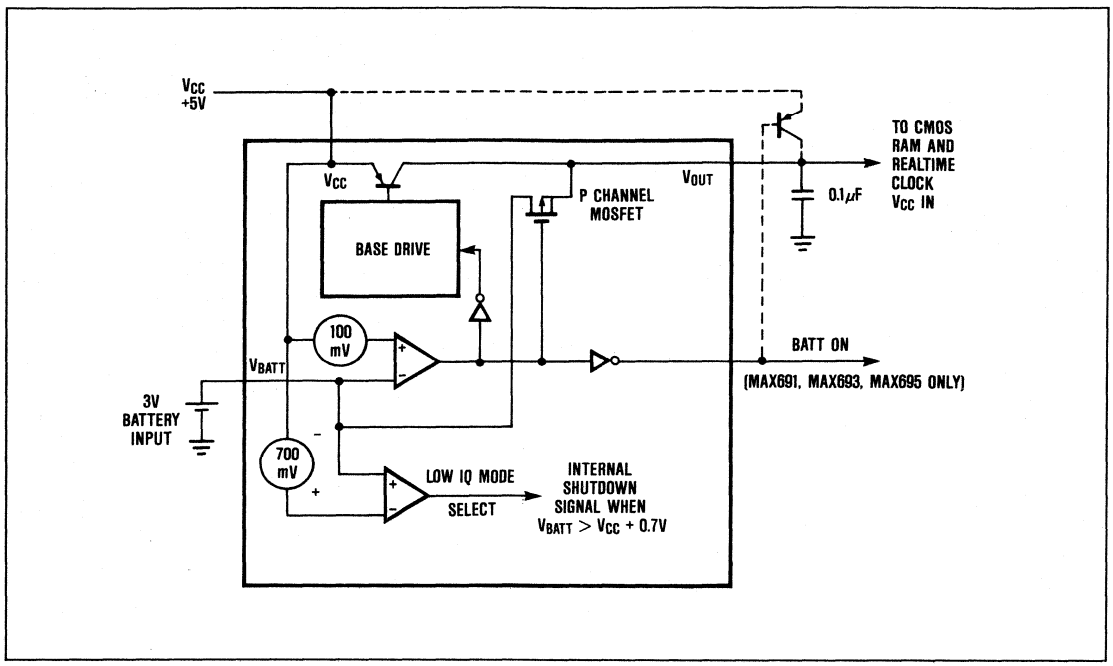


Figure 4. Battery-Switchover Block Diagram

Reset Output

$\overline{\text{RESET}}$ is an active low output which goes low whenever V_{CC} falls below 4.5V (MAX690/691/694/695) or 4.25V (MAX692/693). It will remain low until V_{CC} rises above 4.75V (MAX690/691/694/695) or 4.5V (MAX692/693) for 50 milliseconds*. See Figures 5 and 6.

The guaranteed minimum and maximum thresholds of the MAX690/691/694/695 are 4.5V and 4.75V, while the guaranteed thresholds of the MAX692/693 are 4.25V and 4.5V. The MAX690/691/694/695 is compatible with 5V supplies with a +10%, −5% tolerance while the MAX692/693 is compatible with 5V±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MAX690/691/694/695, and 4.4V in the MAX692/693.

The response time of the reset voltage comparator is about 100μs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{\text{RESET}}$ output.

$\overline{\text{RESET}}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ has an internal 3μA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

**200ms for MAX694 and MAX695*

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MAX691, MAX693 and MAX695 use two pins to control the Chip Enable or Write inputs of CMOS RAMs. When V_{CC} is +5V, CE OUT is a buffered replica of CE IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The MAX693 $\overline{\text{CE}}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{\text{CE}}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{\text{CE}}$ OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect CE IN to GND and use the resulting CE OUT to control a high speed external logic gate. A second alternative is to AND the LOW LINE output with the $\overline{\text{CE}}$ or WR signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MAX690/692/694 can also be used for CMOS RAM write protection.

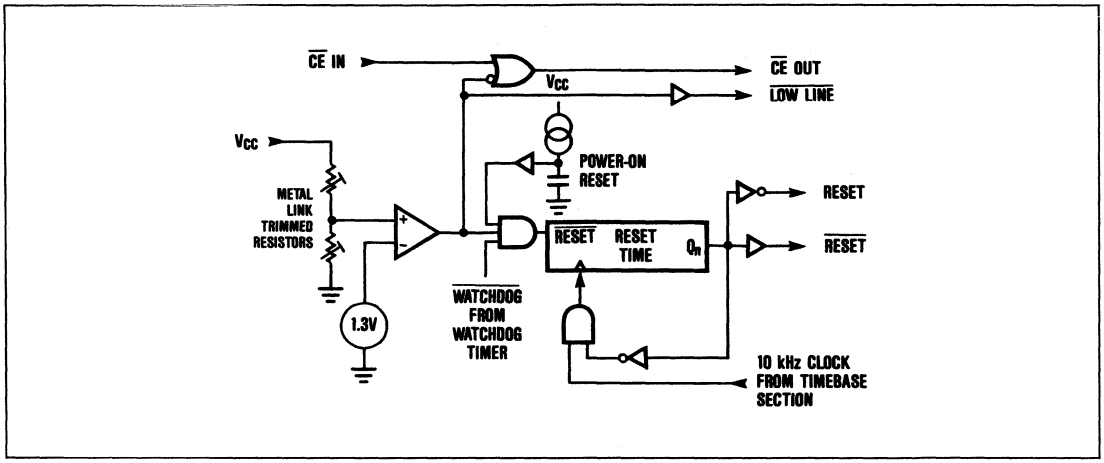


Figure 5. Reset Block Diagram

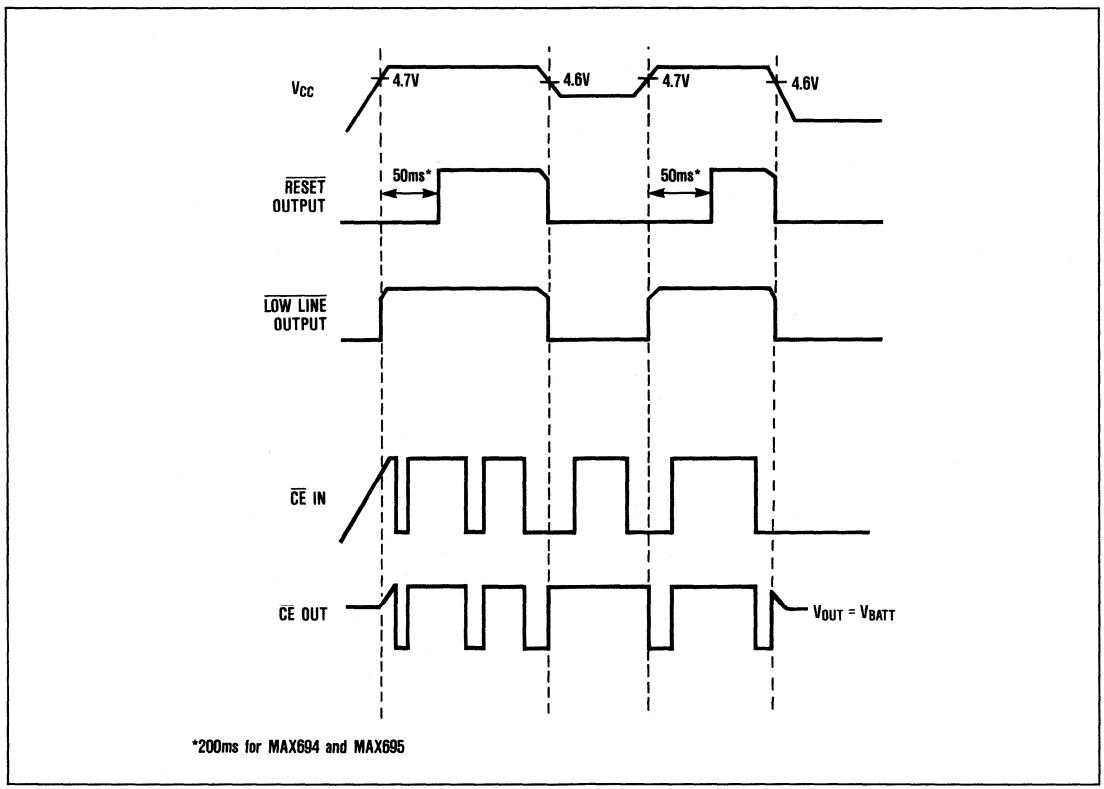


Figure 6. Reset Timing

Microprocessor Supervisory Circuits

1.3V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output (PFO) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. PFO is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the RESET output goes low (4.5V for MAX692/93).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and PFO is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond* RESET pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX691/693/695 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after RESET has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{WDO}$, MAX691/693/695 only) goes low if the watchdog timer "times out" and remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the reset pulse width is fixed at 50ms* on the 8-pin MAX690, MAX692 and MAX694. The MAX691, MAX693 and MAX695 allow these times to be adjusted per Table 1. Figure 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to re-initialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

*200ms for MAX694

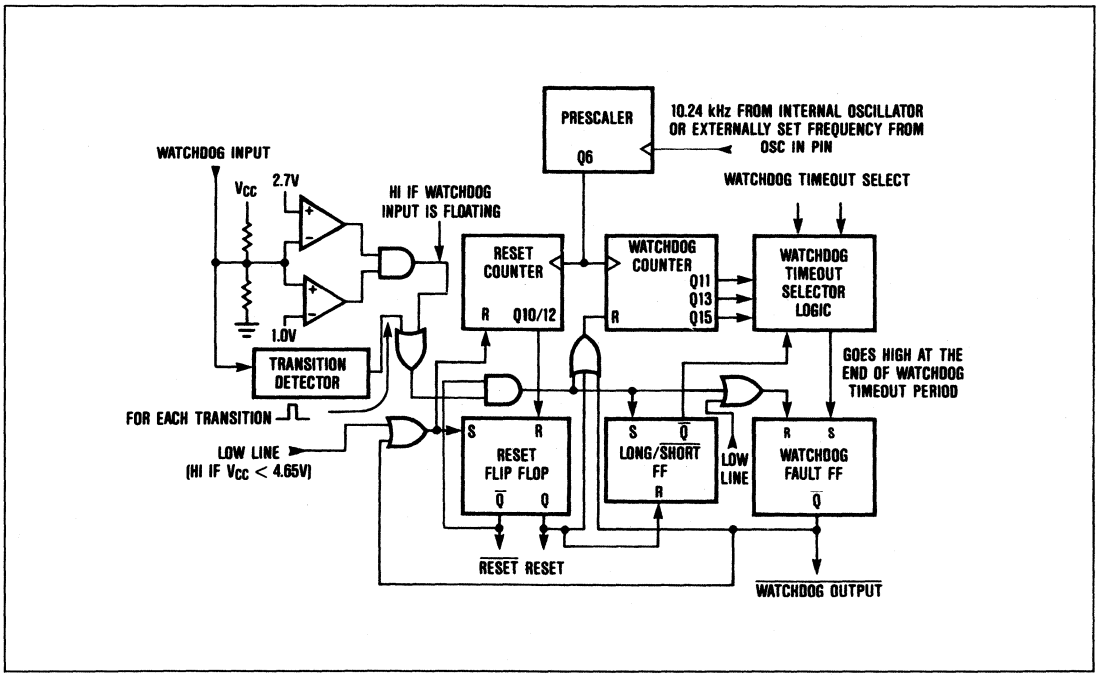


Figure 7. Watchdog Timer Block Diagram

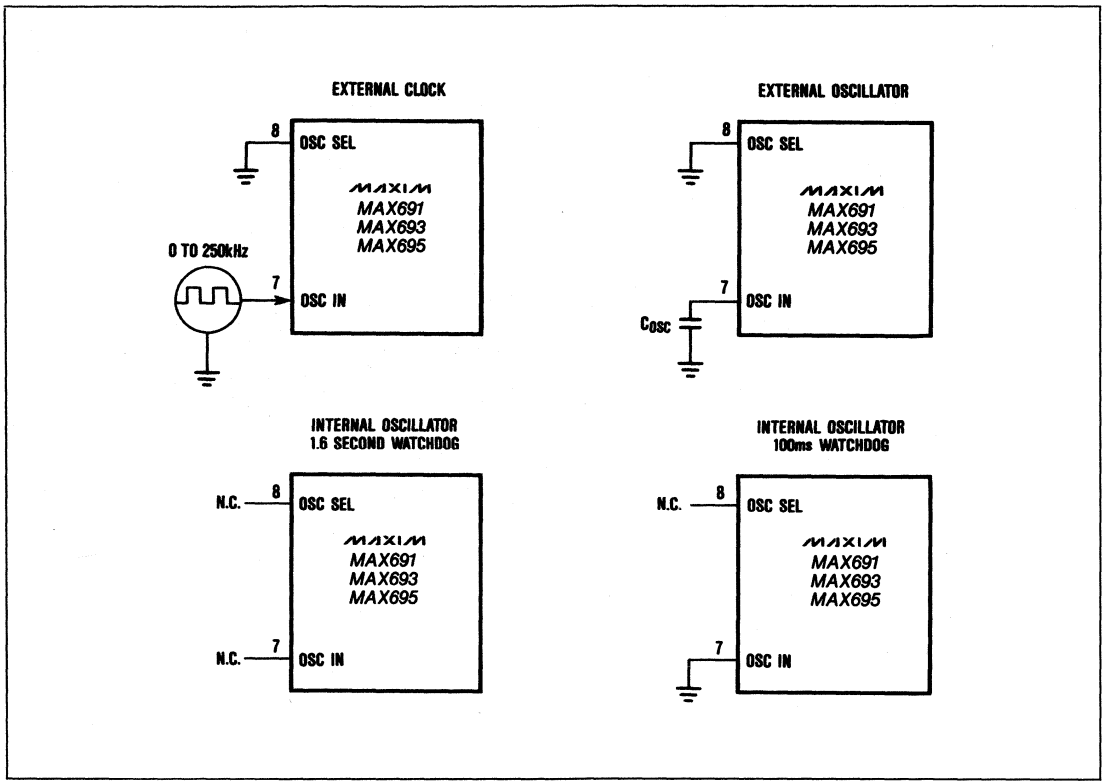


Figure 8. Oscillator Circuits

Table 1. MAX691, MAX693 and MAX695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period	
		Normal	Immediately After Reset	MAX691/93	MAX695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$	$\frac{800ms}{47pF} \times C$
Floating	Low	100ms	1.6 sec	50ms	200ms
Floating	Floating	1.6 sec	1.6 sec	50ms	200ms

Note 1: The MAX690/692/694 watchdog timeout period is fixed at 1.6 seconds nominal, the MAX690/692 Reset pulse width is fixed at 50ms nominal and the MAX694 is 200ms nominal.

Note 2: When the MAX691 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is

$$F_{OSC}(Hz) = \frac{184{,}000}{C(pF)}$$

Note 3: See Electrical Characteristics Table for minimum and maximum timing values.

Microprocessor Supervisory Circuits

Application Hints

Other Uses of the Power Fail Detector

In Figure 9 the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the $\overline{PFO}$ and $\overline{RESET}$ outputs have high sink current capability and only 10μA of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the CE OUT can be used to apply a test load to the battery. Since CE OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 12. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01μF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

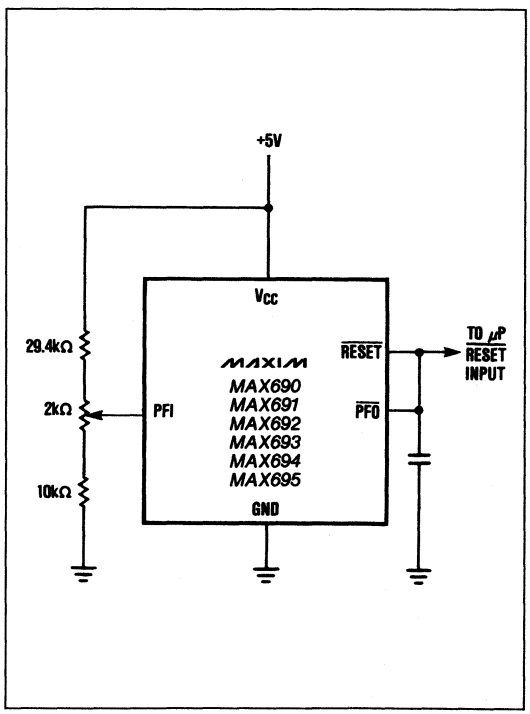


Figure 9. Externally Adjustable V_{CC} Reset Threshold

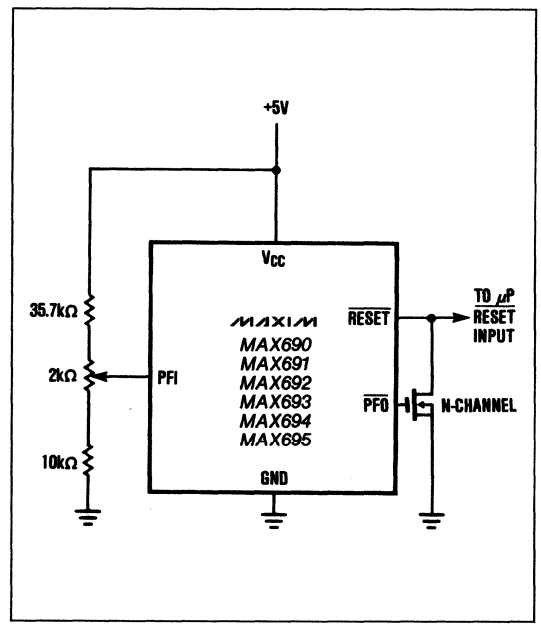


Figure 10. Reset on Overvoltage or Undervoltage

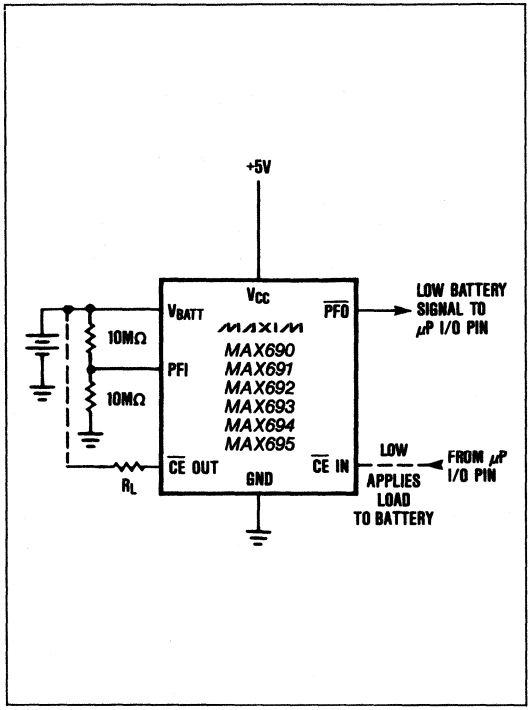


Figure 11. Backup Battery Monitor with Optional Test Load

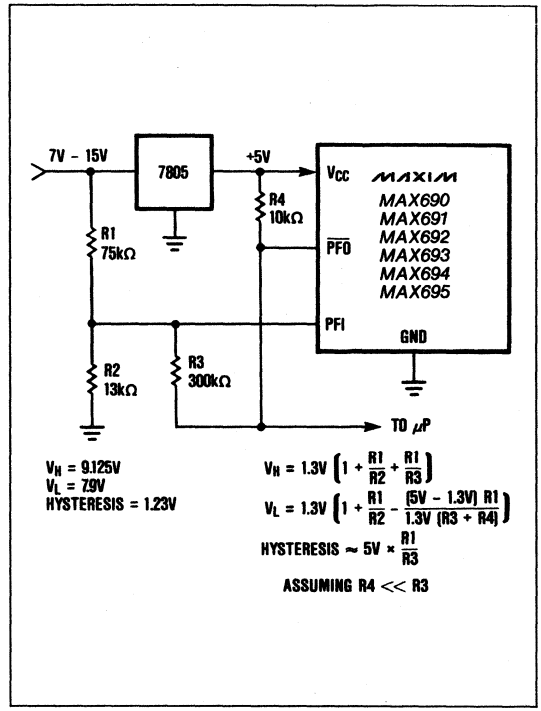


Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

5

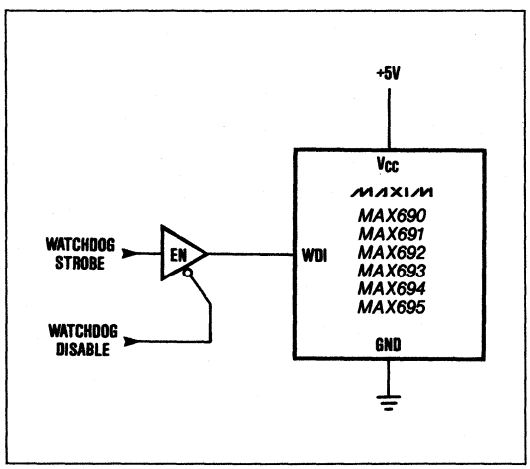


Figure 13. Disabling the Watchdog Under Program Control

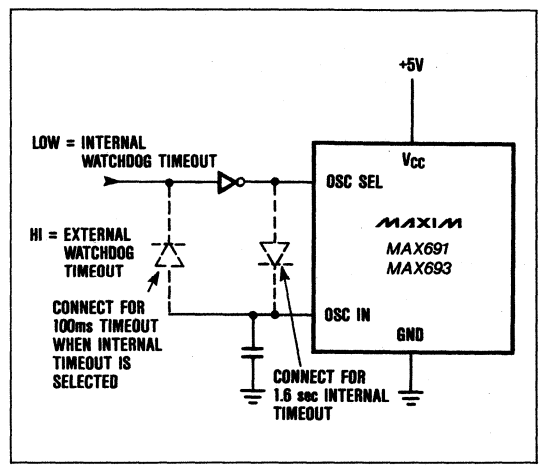


Figure 14. Selecting Internal or External Watchdog Timeout

Microprocessor Supervisory Circuits

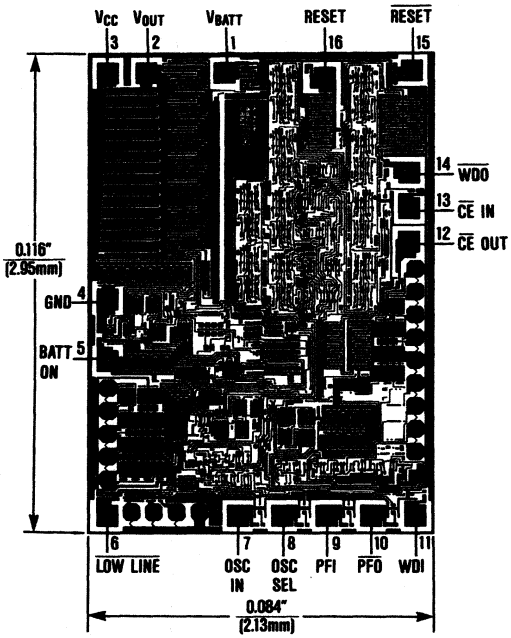
Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
BATT ON	Logic high
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}$ OUT	Logic high
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12μA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} +100mV and V_{BATT} −700mV. The supply current is 1μA maximum when V_{CC} is less than V_{BATT} −700mV.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX692CPA	0°C to +70°C	8 Lead Plastic DIP
MAX692EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX692EJA	−40°C to +85°C	8 Lead CERDIP
MAX692MJA	−55°C to +125°C	8 Lead CERDIP
MAX693C/D	0°C to +70°C	Dice
MAX693CPE	0°C to +70°C	16 Lead Plastic DIP
MAX693CWE	0°C to +70°C	16 Lead Small Outline
MAX693EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX693EJE	−40°C to +85°C	16 Lead CERDIP
MAX693EWE	−40°C to +85°C	16 Lead Small Outline
MAX693MJE	−55°C to +125°C	16 Lead CERDIP
MAX694CPA	0°C to +70°C	8 Lead Plastic DIP
MAX694EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX694EJA	−40°C to +85°C	8 Lead CERDIP
MAX694MJA	−55°C to +125°C	8 Lead CERDIP
MAX695C/D	0°C to +70°C	Dice
MAX695CPE	0°C to +70°C	16 Lead Plastic DIP
MAX695CWE	0°C to +70°C	16 Lead Small Outline
MAX695EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX695EJE	−40°C to +85°C	16 Lead CERDIP
MAX695EWE	−40°C to +85°C	16 Lead Small Outline
MAX695MJE	−55°C to +125°C	16 Lead CERDIP

Chip Topography



MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX696/697 supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX696/697 significantly improves system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MAX696 and MAX697 are supplied in 16 pin packages and perform six functions:

1. A Reset output during power-up, power-down and brownout conditions. The threshold for this "low line" reset is adjustable by an external voltage divider.
2. A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
3. Individual outputs for low line and watchdog fault conditions.
4. The Reset time may be left at its default value of 50 ms. or may be varied with an external capacitor or clock pulses.
5. A separate 1.3 volt threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.

The MAX696 also has battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.

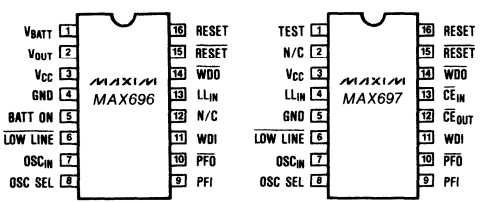
The MAX697 lacks battery backup switching, but has write protection pins ($\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$) for CMOS RAM or EPROM. In addition, it consumes less than 250 microamperes.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

Pin Configurations

Top View



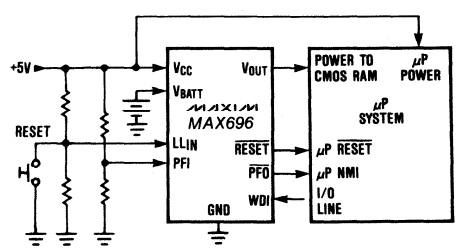
Features

- ◆ **Adjustable Low Line monitor and Power Down Reset**
- ◆ **Power OK/Reset Time Delay**
- ◆ **Watchdog Timer—100ms, 1.6 sec, or adjustable**
- ◆ **Minimum Component Count**
- ◆ **1μA Standby Current**
- ◆ **Battery Backup Power Switching (MAX696)**
- ◆ **Onboard Gating of Chip Enable Signals (MAX697)**
- ◆ **Separate Monitor for Power Fail or Low Battery Warning**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX696C/D	0°C to +70°C	Dice
MAX696CPE	0°C to +70°C	16 Lead Plastic DIP
MAX696CWE	0°C to +70°C	16 Lead Wide SO
MAX696EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX696EJE	-40°C to +85°C	16 Lead CERDIP
MAX696EWE	-40°C to +85°C	16 Lead Wide SO
MAX696MJE	-55°C to +125°C	16 Lead CERDIP
MAX697C/D	0°C to +70°C	Dice
MAX697CPE	0°C to +70°C	16 Lead Plastic DIP
MAX697CWE	0°C to +70°C	16 Lead Wide SO
MAX697EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX697EJE	-40°C to +85°C	16 Lead CERDIP
MAX697EWE	-40°C to +85°C	16 Lead Wide SO
MAX697MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



MAX696 Typical Application

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{OUT} +0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/μs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... -40°C to +85°C
- M suffix ..... -55°C to +125°C

Power Dissipation
- 16 Pin Plastic DIP (Derate 7mW/°C above +70°C) 600mW
- 16 Pin Small Outline (Derate 7mW/°C above +70°C) 600mW
- 16 Pin CERDIP (Derate 10mW/°C above +85°C) 600mW

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range MAX696 V_{CC} MAX696 V_{BATT} MAX697 V_{CC}	T_A = Full	 3.0 2.0 3.0		 5.5 V_{CC} -0.3V 5.5	 V
Supply Current (MAX697)	T_A = Full		160	300	μA
BATTERY BACKUP SWITCHING (MAX696)					
V_{OUT} Output Voltage	I_{OUT} = 1mA, T_A = Full I_{OUT} = 50mA, T_A = Full	V_{CC} -0.3 V_{CC} -0.5		V_{CC} -0.1 V_{CC} -0.25	V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250μA, V_{CC} < V_{BATT} -0.2V, T_A = Full	V_{BATT} -0.1		V_{BATT} -0.02	V
Supply Current (excludes I_{OUT})	I_{OUT} = 1mA I_{OUT} = 50mA		1.5 2.5	4 7	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V, T_A = 25°C V_{CC} = 0V, V_{BATT} = 2.8V, T_A = Full		0.6	1 10	μA
Battery Standby Leakage Current	5.5V > V_{CC} > V_{BATT}+0.3V T_A = 25°C T_A = Full	 -100 -1		 +20 +0.02	 nA μA
Battery Switchover Threshold V_{CC}-V_{BATT}	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	I_{SINK} = 1.6mA			0.4	V
BATT ON Output Short Circuit Current	BATT ON = V_{OUT} = 2.4V Sink Current BATT ON = V_{OUT}, V_{CC} = 0V	 0.5	7 2.5	 25	mA μA
RESET AND WATCHDOG TIMER					
Low Line Voltage Threshold (LL_{IN})	V_{CC} = +5V, +3V, T_A = Full	1.25	1.30	1.35	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Timeout Delay	Figure 6. OSC SEL HIGH, V_{CC} = 5V	35	50	70	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V Short Period, V_{CC} = 5V	1.0 70	1.6 100	2.25 140	sec ms
Watchdog Timeout Period, External Clock	Long Period Short Period	4032 960		4097 1025	Clock Cycles
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 3.5V, V_{CC} = 5V	200			ns
$\overline{RESET}$ and RESET Output Voltage (Note 3)	I_{SINK} = 400μA, V_{CC} = 2V, V_{BATT} = 0 I_{SINK} = 1.6mA, 3V < V_{CC} < 5.5V I_{SOURCE} = 1μA, V_{CC} = 5V	 3.5		0.4 0.4 	V
$\overline{LOW\ LINE}$ and $\overline{WDO}$ Output Voltage	I_{SINK} = 800μA, T_A = Full I_{SOURCE} = 1μA, V_{CC} = 5V, T_A = Full	 3.5		0.4 	V
Output Short Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$	1	3	25	μA
WDI Input Threshold Logic Low Logic High (MAX696) Logic High (MAX697)	V_{CC} = 5V (Note 2)	 3.5 3.8		0.8 	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	 -50	20 -15	50 	μA
POWER FAIL DETECTOR					
PFI Input Threshold	V_{CC} = 3V, 5V	1.2	1.3	1.4	V
PFI-LL_{IN} Threshold Difference	V_{CC} = 3V, 5V		±15	±50	mV
PFI Input Current			±0.01	±25	nA
LL_{IN} Input Current	MAX697	-25	±0.01	+25	nA
	MAX696	-500	±0.01	+25	
$\overline{PFO}$ Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 1μA, V_{CC} = 5V	 3.5		0.4 	V V
$\overline{PFO}$ Short Circuit Source Current	PFI = 0V, $\overline{PFO}$ = 0V	1	3	25	μA
CHIP ENABLE GATING (MAX697)					
$\overline{CE}$ IN Thresholds	V_{IL} V_{IH}, V_{CC} = 5V	 3.0		0.8 	V
$\overline{CE}$ IN Pullup Current			3		μA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 800μA I_{SOURCE} = 1μA, V_{CC} = 0V	 V_{CC} -0.5V V_{CC} -0.05		0.4 	V
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		80	150	ns
OSCILLATOR					
OSC IN Input Current			±2		μA
OSC SEL Input Pullup Current			5		μA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded providing the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Note 3: T_A = Full Operating Range.

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX696	MAX697	
V_{CC}	3	3	The +5V input.
V_{BATT}	1	—	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	2	—	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	4	5	0V ground reference for all signals.
$\overline{RESET}$	15	15	$\overline{RESET}$ goes low whenever LL_{IN} falls below 1.3 volts or V_{CC} falls below the V_{BATT} input voltage. $\overline{RESET}$ remains low for 50ms after LL_{IN} goes above 1.3 volts. $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	11	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	9	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	10	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and LL_{IN} is above 1.3V. See Figure 5.
BATT ON	5	—	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	6	6	$\overline{LOW\ LINE}$ goes low when LL_{IN} falls below 1.3 volts. It returns high as soon as LL_{IN} rises above 1.3 volts. See Figure 5, Reset Timing.
RESET	16	16	RESET is an active high output. It is the inverse $\overline{RESET}$.
OSC SEL	8	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	7	7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven low. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 7. When OSC SEL is high, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	14	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.
NC	12	2	NO CONNECT. Leave this pin open.
LL_{IN}	13	4	LOW LINE INPUT. LL_{IN} is the CMOS input to a comparator whose other input is a precision 1.3 volt reference. The output is $\overline{LOW\ LINE}$ and is also connected to the reset pulse generator. See Figure 2.
TEST	—	1	Used during Maxim manufacture only. Always ground this pin.

Typical Applications

MAX696

A typical connection for the MAX696 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT} -700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's $\overline{\text{RESET}}$ line low when LL_{IN} is below 1.3V. An internal monostable holds $\overline{\text{RESET}}$ low for 50ms after LL_{IN} rises above 1.3V. This prevents repeated toggling of $\overline{\text{RESET}}$ even if the V_{CC} power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{\text{RESET}}$ pulse lasts 50ms to allow for this oscillator start-up time. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MAX696 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output ($\overline{\text{PFO}}$) drives the processor's NMI input low. An earlier power fail warning can be generated if the unregulated DC input of the regulator is available for monitoring.

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MAX696 will issue a 50ms $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low it remains low until a transition occurs at WDI while $\overline{\text{RESET}}$ is high. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 7.

MAX697

The MAX697 is nearly identical to the MAX696. The MAX697 lacks the battery backup feature, so it does not have the V_{BATT}, V_{OUT}, or BATT ON pins. This allows the MAX697 to consume less than 250 microamperes, and it allows the inclusion of RAM write protection pins. See Figure 2.

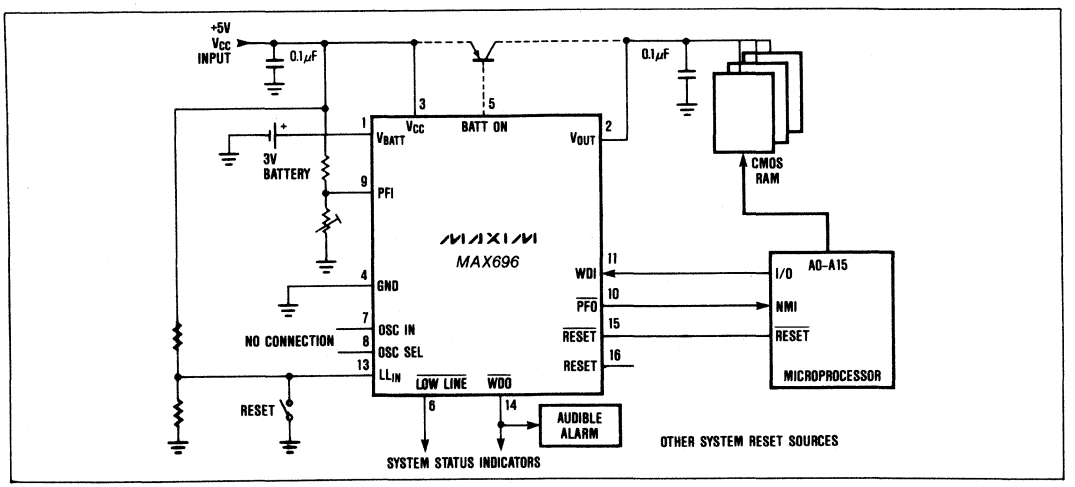
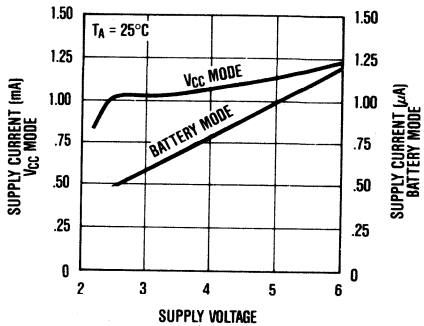
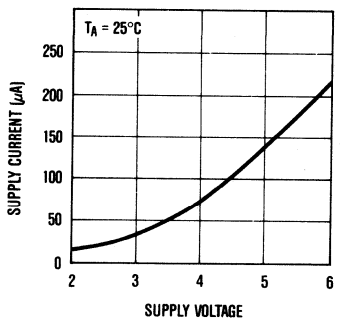


Figure 1. MAX696 Typical Application

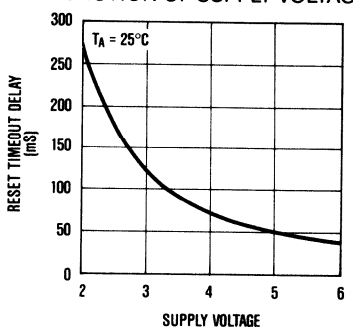
MAX696
SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE



MAX697
SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE



RESET TIMEOUT DELAY AS A
FUNCTION OF SUPPLY VOLTAGE



Detailed Description

Battery-Switchover and V_{OUT} (MAX696)

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (See Figure 3). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output can directly drive the base of the external transistor.

It should be noted that the MAX696 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX696 operates with battery voltages from 2.0V to 4.25V. The battery voltage should not be within 0.5V of V_{CC} or switchover may occur. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The capacitor charging voltage should include a diode to limit the fully charged voltage to approximately 0.5V less than V_{CC}. The charging resistor for rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small leakage current of typically 10nA (20nA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum current (20nA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

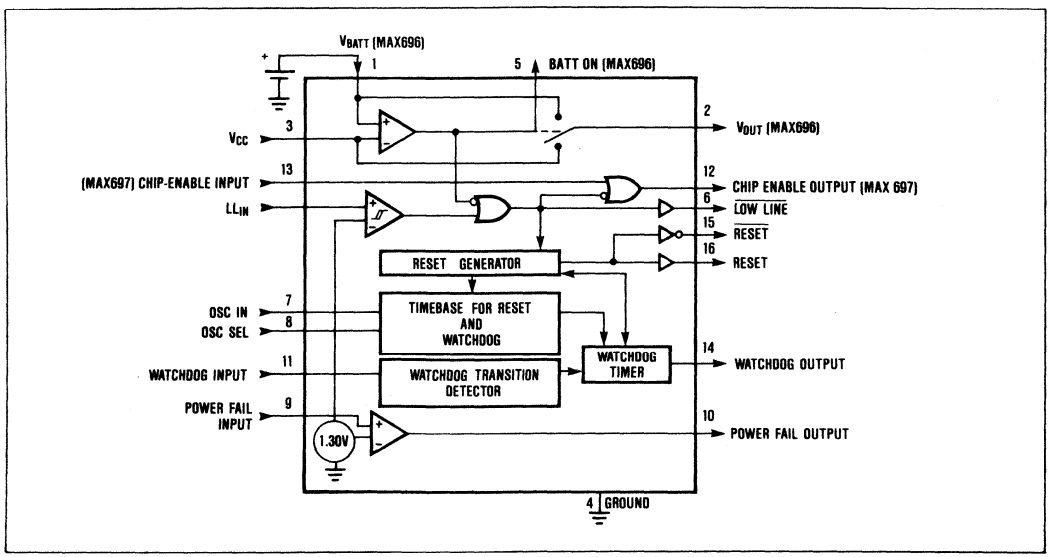


Figure 2. MAX696/697 Block Diagram

Microprocessor Supervisory Circuits

Reset Output

$\overline{RESET}$ is an active low output which goes low whenever LL_{IN} falls below 1.3 volts. It will remain low until LL_{IN} rises above 1.312 volts for 50 milliseconds. (See Figures 4 and 5.)

The guaranteed minimum and maximum low line thresholds of the MAX696/697 are 1.2 and 1.4 volts. The LL_{IN} comparator has approximately 12mV of hysteresis.

The response time of the reset voltage comparator is about 100 microseconds. LL_{IN} should be bypassed to ensure that glitches do not activate $\overline{RESET}$ output.

$\overline{RESET}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{RESET}$ has an internal 3μA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{CE}$ Gating and RAM Write Protection

The MAX697 uses two pins to control the Chip Enable or Write inputs of CMOS RAMs. When LL_{IN} is > 1.3V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50ns propagation delay. If LL_{IN} input falls below 1.3V (1.2 min., 1.4 max.) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The $\overline{CE}$ output is also forced high when V_{CC} is less than V_{BATT}. (See Figure 4.)

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$ or $\overline{Write}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting $\overline{CE}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{LOW\ LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the $\overline{RESET}$ output of the MAX696/697 can also be used for CMOS RAM write protection.

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's V_{CC} regulator or the regulated output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the LL_{IN} falls below 1.3V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before LL_{IN} falls below 1.3V and the $\overline{RESET}$ output goes low.

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{PFO}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

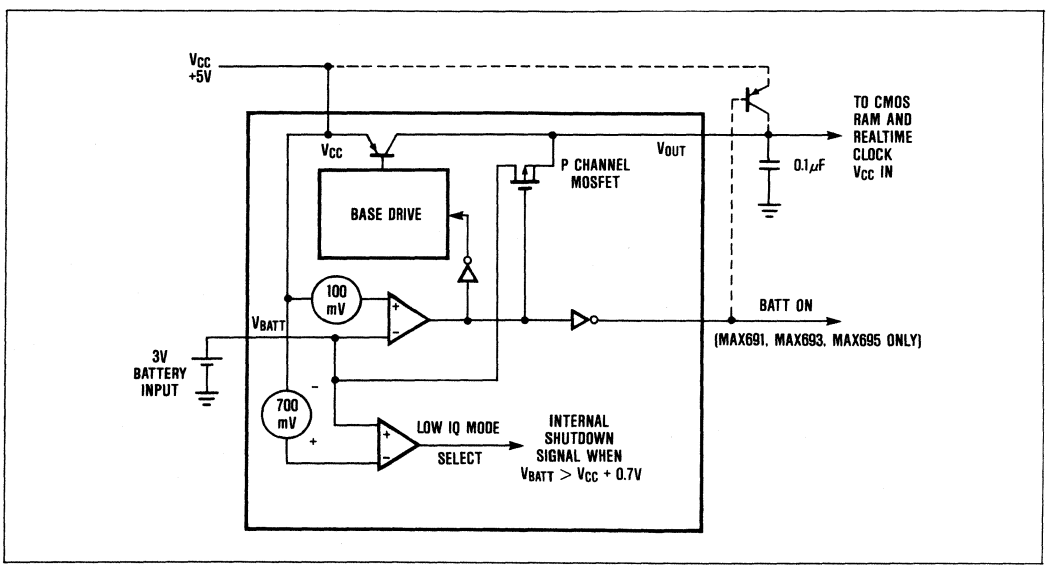


Figure 3. MAX696 Battery-Switchover Block Diagram

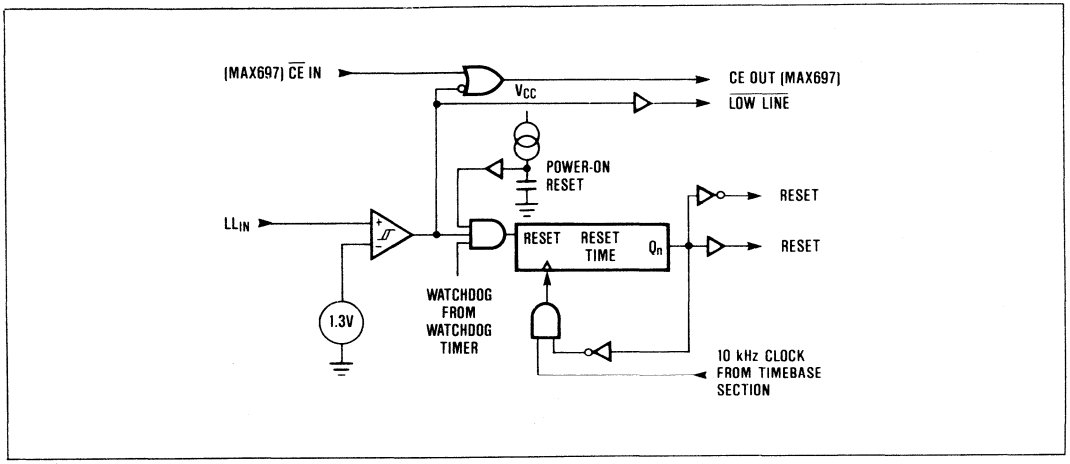


Figure 4. Reset Block Diagram

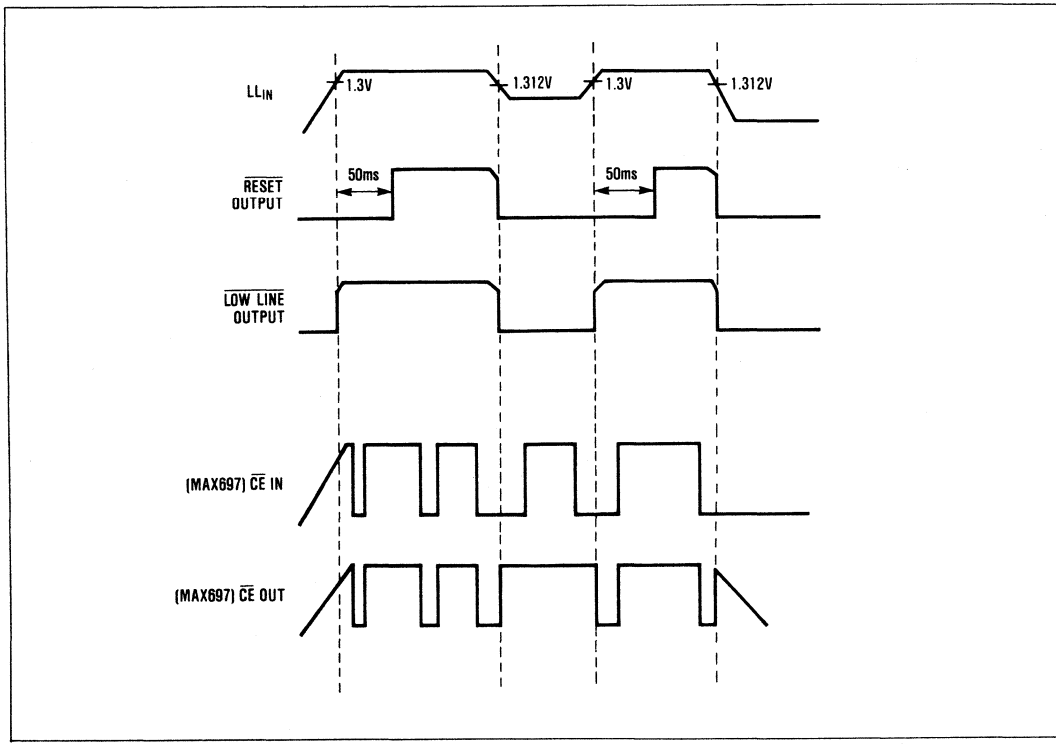


Figure 5. MAX697 Reset Timing

Microprocessor Supervisory Circuits

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 milliseconds $\overline{\text{RESET}}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX696/697 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by LL_{IN} falling below 1.3V. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output $\overline{\text{WDO}}$ goes low if the watchdog timer "times out," and it remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when LL_{IN} goes below 1.3V.

The watchdog timeout period defaults to 1.6 seconds and the reset pulse width defaults to 50ms. The MAX696 and MAX697 allow these times to be adjusted per Table 1.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. WD transmissions while $\overline{\text{RESET}}$ is low are ignored. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

Application Hints

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 7. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 8). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 9. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01μF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 9 is used.

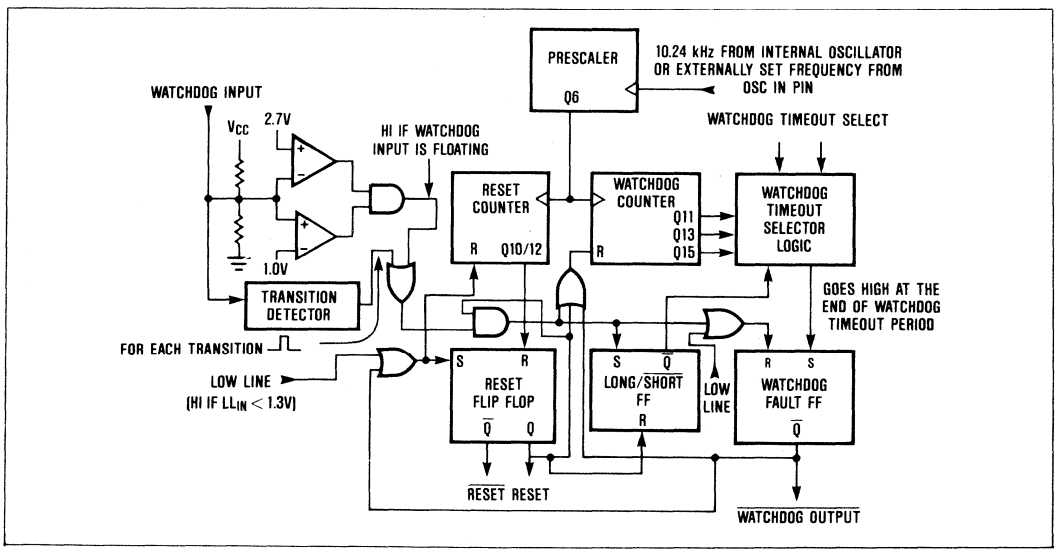


Figure 6. Watchdog Timer Block Diagram

Table 1. MAX696 and MAX697 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL (Note 3)	OSC IN	WATCHDOG TIMEOUT PERIOD NORMAL	WATCHDOG TIMEOUT PERIOD IMMEDIATELY AFTER RESET	RESET TIMEOUT PERIOD
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pf} \times C$	$\frac{1.6\ sec}{47pf} \times C$	$\frac{200ms}{47pf} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	Floating	1.6 sec	1.6 sec	50ms

Note 1: When the MAX696/697 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $F_{OSC}(Hz) = \frac{184,000}{C_{OSC}(pF)}$

Note 2: See Electrical Characteristics Table for minumum and maximum timing values.

Note 3: "HIGH" for the OSC SEL pin should be connected to V_{OUT}, not V_{CC} (on MAX696).

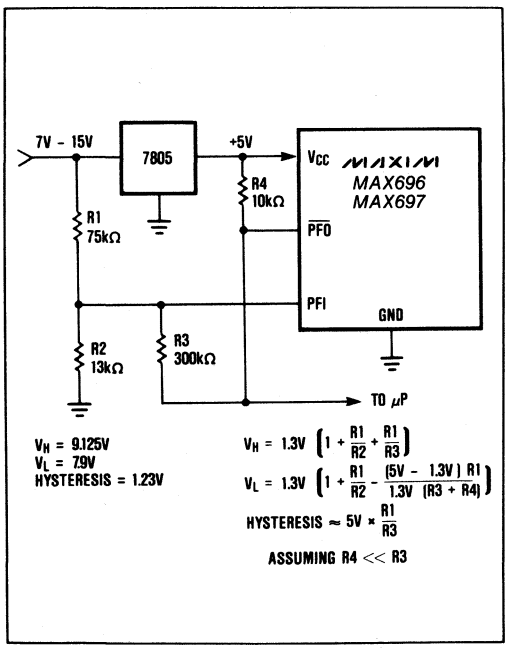


Figure 7. Adding Hysteresis to the Power Fail Voltage Comparator

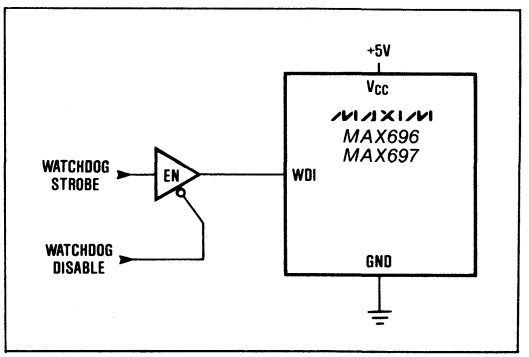


Figure 8. Disabling the Watchdog Under Program Control

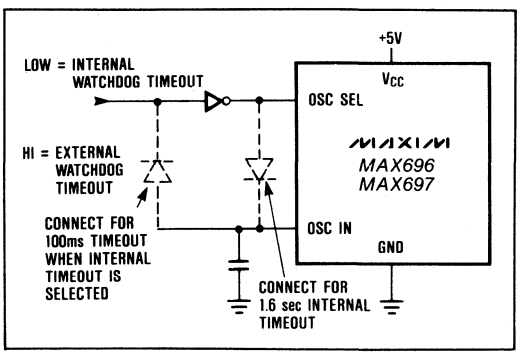


Figure 9. Selecting Internal or External Watchdog Timeout

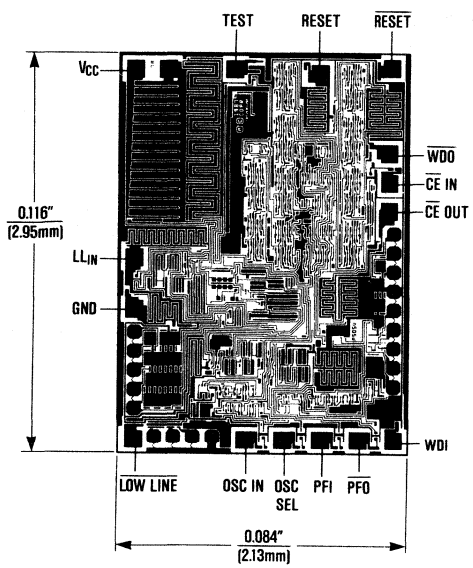
Microprocessor Supervisory Circuits

Table 2. Input and Output Status in Battery Backup Mode

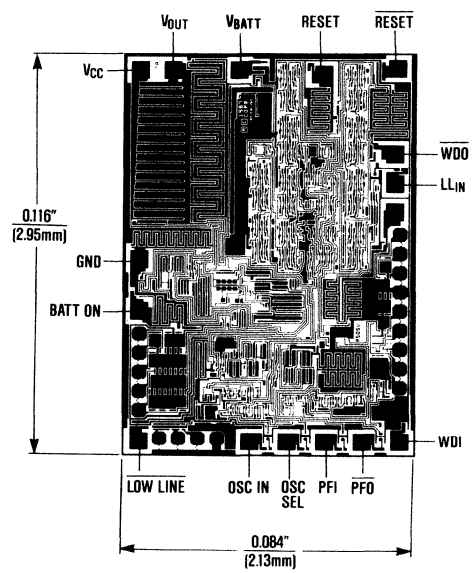
V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET. (MAX696 only)
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
BATT ON	Logic high (MAX696 only)
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current. (MAX697 only)
$\overline{CE}$ OUT	Logic high (MAX697 only)
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12μA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1μA maximum when V_{CC} is less than V_{BATT} - 700mV.

Chip Topography

MAX697



MAX696



MAXIM

Low Cost Power-On Reset and Watchdog Controllers

General Description

The MAX698 and MAX699 monitor the +5V supply in microprocessor and digital systems. They supply a RESET pulse of at least 140ms duration on power-up, power-down, and during low voltage "brown out" conditions. Circuit reliability is increased at reduced cost by eliminating all external components and adjustments.

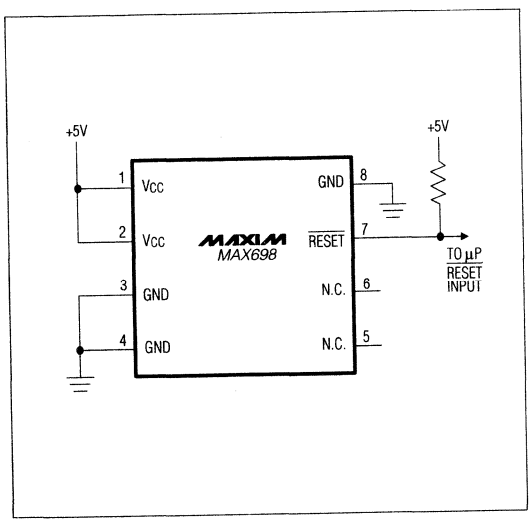
The MAX699 includes all features of the MAX698 but also provides a "watchdog" input to monitor microprocessor activity. The RESET output goes low if the watchdog input (WDI) is not toggled within 1 second. The watchdog feature can be disabled by leaving WDI open.

Both parts are supplied in 8 lead DIP and 16 lead 0.3" wide Small Outline (SO) packages and are specified from 0°C to +70°C for "C" grade devices and -40°C to +85°C for "E" devices. The Small Outline versions, with more pins than the 8 lead DIP, have additional outputs not available in DIP packages. These are RESET (without inversion) and Watchdog Output (WDO).

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



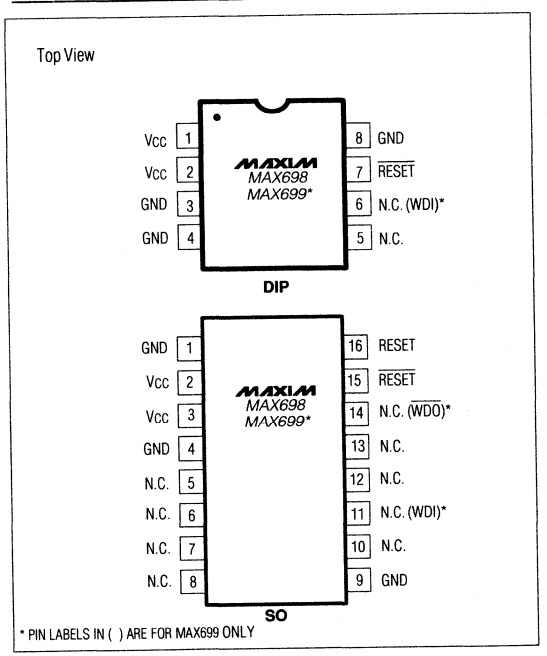
Features

- ♦ Precision Voltage Monitor
- ♦ Power OK/Reset Time Delay
- ♦ Watchdog Timer
- ♦ Minimum Component Count

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX698CPA	0°C to +70°C	8 Lead Plastic DIP
MAX698CWE	0°C to +70°C	16 Lead Wide SO
MAX698EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX698EWE	-40°C to +85°C	16 Lead Wide SO
MAX699CPA	0°C to +70°C	8 Lead Plastic DIP
MAX699CWE	0°C to +70°C	16 Lead Wide SO
MAX699EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX699EWE	-40°C to +85°C	16 Lead Wide SO

Pin Configurations



5

Low Cost Power-On Reset and Watchdog Controllers

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to 6.0V
Input Voltage (with respect to GND)
WDI, $\overline{WDO}$, RESET, $\overline{RESET}$ ..... -0.3V to V_{CC}
Operating Temperature Range
MAX69XC ..... 0°C to +70°C
MAX69XE ..... -40°C to +85°C

Rate of Rise, V_{CC} 100V/µs
Power Dissipation
Plastic DIP (Derate 5mW/°C above 70°C) 400mW
Small Outline (Derate 7mW/°C above 70°C) 600mW
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operations sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = +5V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	T_A = Full	3.0		5.5	V
Supply Current				5	mA
Power Up Reset De-Assertion	T_A = Full	4.5	4.65	4.75	V
Power Down Reset Assertion	T_A = Full	4.4			V
Hysteresis			40		mV
Reset Output Pulse Width		140		500	ms
$\overline{RESET}$ Output Output Low Output High	(Open Drain) I_{SINK} = 1.6mA, V_{CC} = 4.4V I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4	V
RESET Output - SO Pkg. Only Output Low Output High	 I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1µA, V_{CC} = 4.4V	 3.5		0.4	V
$\overline{WDO}$ Output - SO MAX699 Only Output Low Output High	 I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1µA, V_{CC} = 4.4V	 3.5		0.4	V
MAX699 Watchdog Timeout Period		1.0	1.6	2.25	sec
MAX699 Minimum WDI Input Pulse Width		200			ns
MAX699 WDI Input Threshold Logic Low Logic High	V_{CC} = +5V	 3.8		0.8	V
MAX699 WDI Input Current	WDI = V_{CC} WDI = 0V	 -50	20 -15	50	µA

Pin Description

NAME	FUNCTION
V_{CC}	+5V sense input and MAX698/699 chip power.
GND	Chip power GND.
$\overline{RESET}$	Goes low when V_{CC} falls below internally set threshold (See Electrical Characteristics).
RESET	(Small Outline devices only) Goes high when V_{CC} falls below internally set threshold.
WDI	(MAX699 only) A three level input. If WDI remains high or low for more than the watchdog timeout period, $\overline{RESET}$ pulses low ($\overline{WDO}$ also goes low on Small Outline MAX699). If WDI is unconnected or at mid supply, the watchdog circuit is disabled.
$\overline{WDO}$	(Small Outline MAX699 only) Goes low when WDI remains high or low for more than the watchdog timeout period. $\overline{WDO}$ is set high at the next WDI transition. If WDI is unconnected or at mid supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also remains high when V_{CC} falls below 4.4V.

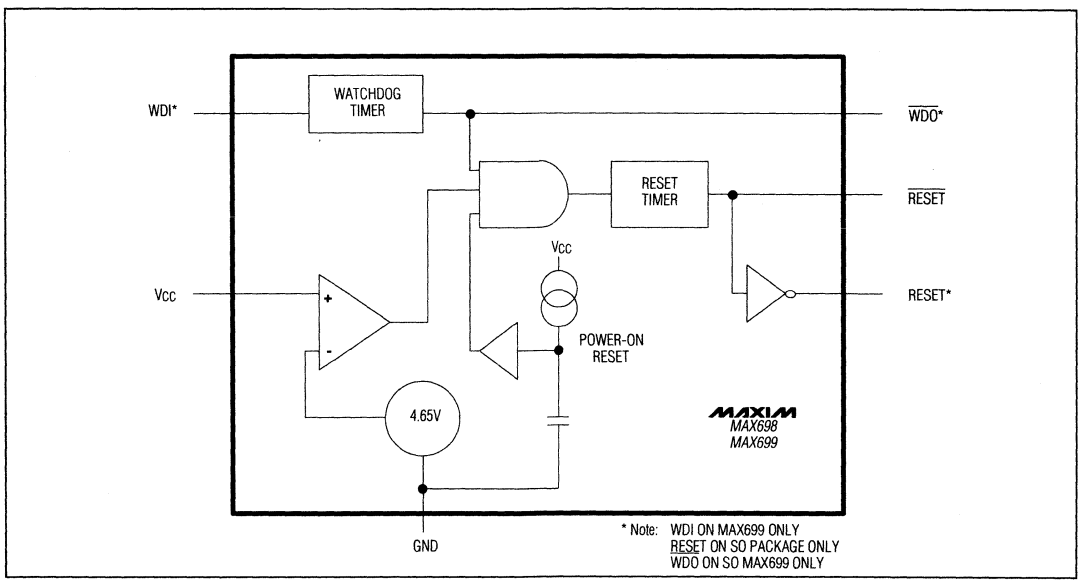
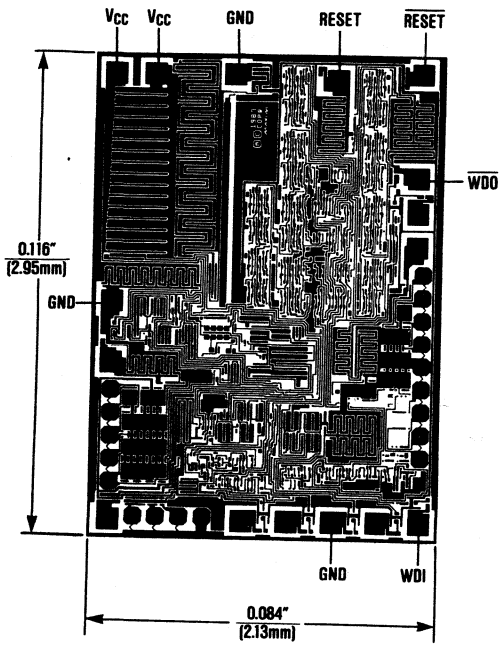


Figure 1. MAX698/699 Block Diagram

Low Cost Power-On Reset and Watchdog Controllers

Chip Topography



Power-Supply Monitor with Reset

General Description

The MAX700/701/702 are supervisory circuits used to monitor the power supplies in µP and digital systems. The $\overline{RESET}$/RESET outputs of the MAX700/701/702 are guaranteed to be in the correct state for V_{CC} voltages down to +1V (Figure 4). They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V powered circuits.

The MAX702 is the simplest part in the family. When V_{CC} falls to 4.65V, $\overline{RESET}$ goes low. The MAX702 also provides a debounced manual reset input. The MAX701 performs the same functions but has both $\overline{RESET}$ and RESET outputs. Their primary function is to provide a system reset. Accordingly, an active reset signal is supplied for low supply voltages and for at least 200ms after the supply voltage reaches its operating value.

In addition to the features of the MAX701 and MAX702, the MAX700 provides preset or adjustable voltage detection so thresholds other than 4.65V can be selected, and adjustable hysteresis. All parts are supplied in 8-pin Plastic DIP and Narrow SO packages in commercial and extended temperature ranges.

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

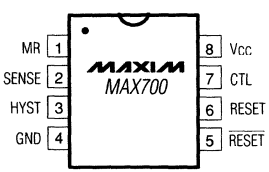
- **Min 200ms $\overline{RESET}$ Pulse on Power-Up, Power-Down, and During Low-Voltage Conditions**
- **Reset Threshold Factory Trimmed for +5V Systems**
- **No External Components or Adjustments With +5V Powered Circuits**
- **Debounced Manual Reset Input**
- **Preset or Adjustable Voltage Detection (MAX700)**
- **Adjustable Hysteresis (MAX700)**
- **8-Pin Plastic DIP and Narrow SO Packages**

Ordering Information

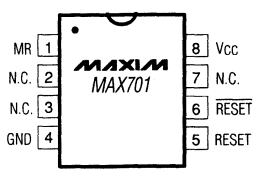
PART	TEMP. RANGE	PIN-PACKAGE
MAX700CPA	0°C to +70°C	8 Plastic DIP
MAX700CSA	0°C to +70°C	8 Narrow SO
MAX700C/D	0°C to +70°C	Dice
MAX700EPA	-40°C to +85°C	8 Plastic DIP
MAX700ESA	-40°C to +85°C	8 Narrow SO
MAX701CPA	0°C to +70°C	8 Plastic DIP
MAX701CSA	0°C to +70°C	8 Narrow SO
MAX701C/D	0°C to +70°C	Dice
MAX701EPA	-40°C to +85°C	8 Plastic DIP
MAX701ESA	-40°C to +85°C	8 Narrow SO
MAX702CPA	0°C to +70°C	8 Plastic DIP
MAX702CSA	0°C to +70°C	8 Narrow SO
MAX702C/D	0°C to +70°C	Dice
MAX702EPA	-40°C to +85°C	8 Plastic DIP
MAX702ESA	-40°C to +85°C	8 Narrow SO

Pin Configurations

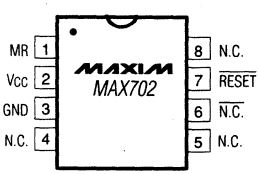
TOP VIEW



DIP/SO



DIP/SO



DIP/SO

Power-Supply Monitor with Reset

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +15.5V
Voltage (with respect to GND) at RESET, $\overline{RESET}$, HYST,
CTL, SENSE ..... -0.3V to Vcc
Operating Temperature Range
MAX70_C ..... 0°C to +70°C
MAX70_E ..... -40°C to +85°C

Rate of Rise, V_{CC} 100V/µs
Power Dissipation, any package 380mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = +5V, CTL = GND on MAX700, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Monitor Voltage Range MAX700 Only	$T_A = T_{MIN}$ to T_{MAX} CTL = V_{CC}	3		15	V
Min V_{CC} For Valid Reset Output, Declining Supply	$T_A = T_{MIN}$ to T_{MAX} $\overline{RESET}$ ≤ 0.4V when sinking 1mA	1.5	1		V
Supply Current			100	200	µA
Reset Threshold Power-up Power-down	$T_A = T_{MIN}$ to T_{MAX}	 4.5 4.5	 4.65 4.62	 4.75 4.75	V
Internal Hysteresis	HYST not connected		30		mV
Reset Output Pulse Width		200	350	500	ms
RESET Fall Time	MAX700/701 Only, C_{LOAD} = 100pF		200		ns
V_{CC} Pulse Duration Guaranteeing No Reset Reset	5V to 4V V_{CC} Pulse	 100	 10 10	 1	µs
MR Input Threshold			0.7		V
MR Pullup Current			-5	-30	µA
MAX700					
RESET Output Low RESET Output High	I_{SINK} = 3.2mA, V_{CC} = 5V I_{SINK} = 1.6mA, V_{CC} = 3V I_{SOURCE} = 3.2mA, V_{CC} = 4.25V I_{SOURCE} = 1.6mA, V_{CC} = 3V I_{SOURCE} = 0.5mA, V_{CC} = 1.5V	 V_{CC}-0.4 V_{CC}-0.4 V_{CC}-0.4		0.4 0.4	V
$\overline{RESET}$ Output Low $\overline{RESET}$ Output High	I_{SINK} = 16mA, V_{CC} = 4.25V I_{SINK} = 1.6mA, V_{CC} = 3V I_{SINK} = 0.4mA, V_{CC} = 1.5V I_{SOURCE} = 3.2mA, V_{CC} = 5V I_{SOURCE} = 1.6mA, V_{CC} = 3V	 V_{CC}-0.4 V_{CC}-0.4		0.4 0.4 0.4	V
MAX701					
RESET Output Low RESET Output High	I_{SINK} = 16mA, V_{CC} = 5V I_{SOURCE} = 3.2mA, V_{CC} = 4.25V I_{SOURCE} = 1.6mA, V_{CC} = 3V I_{SOURCE} = 0.5mA, V_{CC} = 1.5V	 V_{CC}-0.4 V_{CC}-0.4 V_{CC}-0.4		0.4	V
$\overline{RESET}$ Output Low $\overline{RESET}$ Output High	I_{SINK} = 3.2mA, V_{CC} = 4.25V I_{SINK} = 1.6mA, V_{CC} = 3V I_{SINK} = 0.4mA, V_{CC} = 1.5V I_{SOURCE} = 3.2mA, V_{CC} = 5V	 V_{CC}-0.4		0.4 0.4 0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(T_A = 25°C, V_{CC} = +5V, CTL = GND on MAX700, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAX702					
$\overline{RESET}$ Output Low	I_{SINK} = 3.2mA, V_{CC} = 4.25V I_{SINK} = 1.6mA, V_{CC} = 3V I_{SINK} = 0.4mA, V_{CC} = 1.5V			0.4 0.4 0.4	V
$\overline{RESET}$ Output High	I_{SOURCE} = 3.2mA, V_{CC} = 5V	V_{CC}-0.4			
MAX700 ONLY (CTL = V_{CC}, unless otherwise noted.)					
SENSE Input Threshold	T_A = T_{MIN} to T_{MAX}	1.25	1.29	1.35	V
SENSE Input Current			0.1		nA
HYST Input On Resistance			0.5		kΩ
CTL Input Threshold			2		V
CTL Pulldown Current			30	100	µA

Pin Description

NAME	FUNCTION
V_{CC}	Chip power and +5V sensing input (when CTL = GND on MAX700).
GND	Ground
$\overline{RESET}$	Goes low when V_{CC} falls below 4.65V, or when CTL = V_{CC} on the MAX700 goes low when SENSE falls below 1.9V.
RESET	MAX700, 701 only – Inverted Version of $\overline{RESET}$.
MR	Input for manual push button reset. Has internal 5µA pull up. Low input activates the RESET/$\overline{RESET}$ outputs.
CTL	MAX700 only – When CTL = GND, V_{CC} is monitored by the reset circuit. When CTL = V_{CC}, V_{CC} is ignored and SENSE is monitored, allowing the threshold to be set with external resistors.
HYST	MAX700 only – Normally NOT used when voltage is monitored through V_{CC} (CTL = GND). When monitoring through SENSE (CTL = V_{CC}), HYST allows hysteresis to be added, reducing noise and spurious reset activity (Figure 3). HYST turns on 5µs before the RESET/$\overline{RESET}$ outputs are activated, and its on resistance to GND is typically 1kΩ.
SENSE	MAX700 only – The voltage sense input when CTL = V_{CC}. Its threshold is 1.29V. Sense always remains connected to the internal comparator. So, when V_{CC} is being monitored internally (CTL = GND), SENSE should be left open circuit.

5

Power-Supply Monitor with Reset

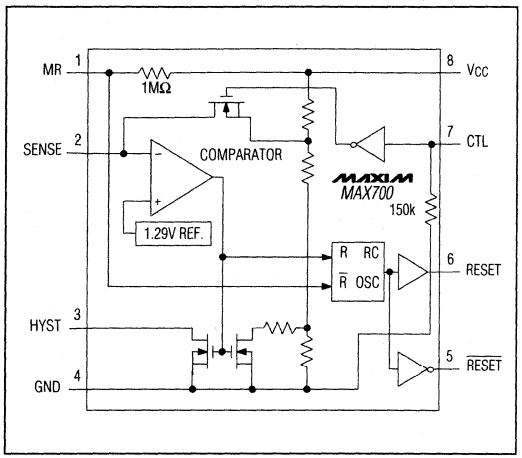


Figure 1. MAX700 Block Diagram

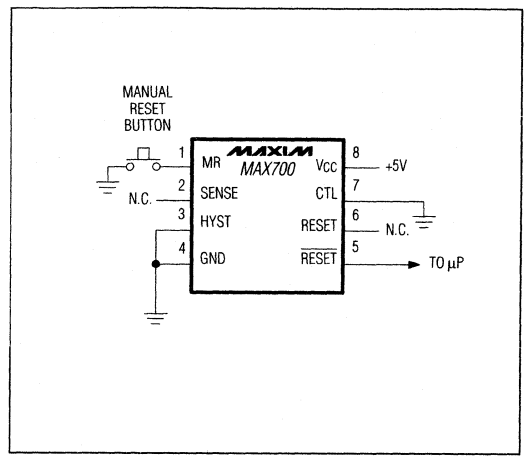


Figure 2. MAX700 Typical Connection Diagram

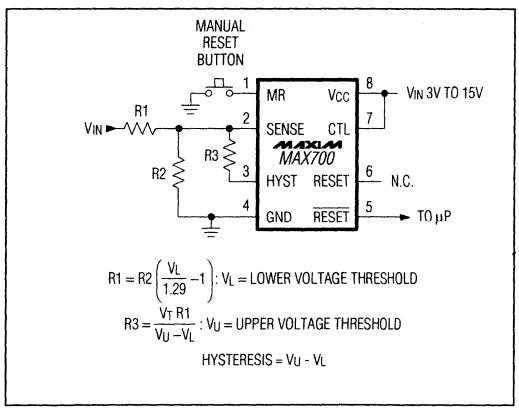


Figure 3. MAX700 Connected for External Sense and Hysteresis

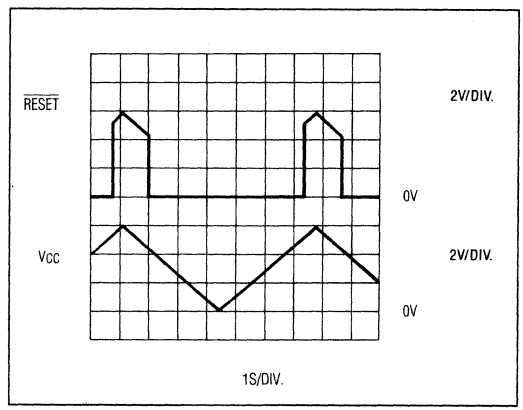


Figure 4. Typical MAX700/701/702 $\overline{RESET}$ Output vs. V_{CC}

Figure 4 shows the $\overline{RESET}$ output of the MAX700/701/702 in the correct state for V_{CC} voltages down to 0V. Note the effect of the built-in hysteresis on the trigger level of $\overline{RESET}$.

ADVANCE INFORMATION

FIRST PAGE OF DATA SHEET IN PREPARATION

MAXIM

High-Performance Supervisory Circuits

General Description

The MAX790/MAX791 supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. These include µP reset, backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The $\overline{\text{RESET}}$ output of the ICs is guaranteed to be in the correct state for V_{CC} voltages down to 1V.

The MAX790/MAX791 offer several improvements over Maxim's MAX690 Series of supervisory circuits, including 70µA supply current, 10ns CE propagation delay, 250mA output current (V_{CC} mode), and 25mA output current (VBATT mode). The MAX790 is pin compatible with the MAX690.

Applications

Computers

Controllers

Intelligent Systems

Automotive Systems

Critical µP Power Monitoring

Features

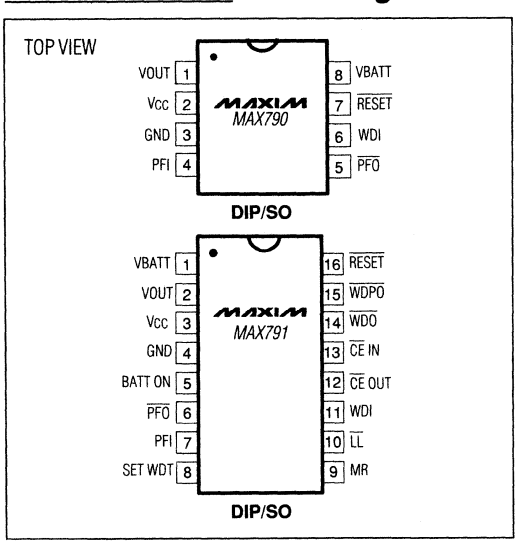
- ♦ **Precision 4.72V Monitor**
- ♦ **250ms $\overline{\text{RESET}}$ V_{CC} Assertion Time**
- ♦ **1.6sec or Adjustable Watchdog Timeout Period**
- ♦ **Min Component Count**
- ♦ **1µA Standby Current**
- ♦ **Monitors Backup Battery**
- ♦ **Battery-Backup Power Switching**
- ♦ **On-board Gating of Chip-Enable Signals**

Ordering Information

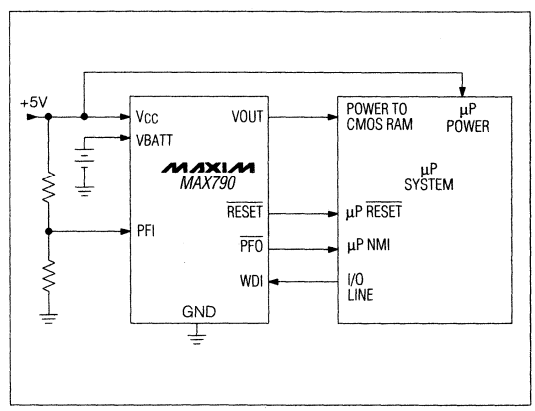
PART	TEMP. RANGE	PIN-PACKAGE
MAX790CPA	0°C to +70°C	8 Plastic DIP
MAX790C/D	0°C to +70°C	Dice*
MAX790EPA	-40°C to +85°C	8 Plastic DIP
MAX790MJA	-55°C to +125°C	8 CERDIP
MAX791CPE	0°C to +70°C	16 Plastic DIP
MAX791CWE	-0°C to +70°C	16 Wide SO
MAX791C/D	0°C to +70°C	Dice*
MAX791EPE	-40°C to +85°C	16 Plastic DIP
MAX791EWE	-40°C to +85°C	16 Wide SO
MAX791MJE	-55°C to +125°C	16 CERDIP

Consult factory for dice specifications.

Pin Configurations



Typical Operating Circuit



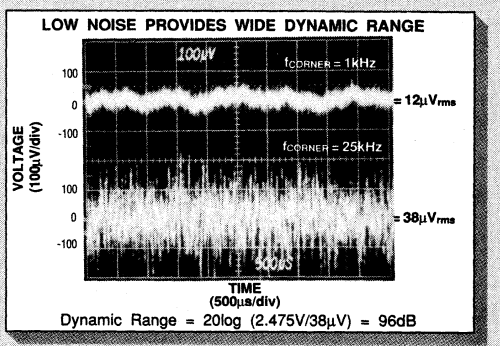
MAXIM

Analog Filters

Un-Clocked Lowpass Filters Have 96dB Dynamic Range

No Design, No External Components Needed

Do you have lowpass filtering applications, such as anti-aliasing or output smoothing, requiring a wide 96dB dynamic range? Maxim's new MAX270 and MAX271 dual, 2nd-order Chebyshev filters achieve an impressive noise level of less than 38μVrms by combining a proprietary low-noise circuit design, with all noise-sensitive nodes inside the package, and a continuous-time architecture. Unlike switched-capacitor filters, continuous-time filters require NO clocking. This removes the need for clock signals in analog input and output circuitry, where clock-noise coupling often degrades circuit performance.



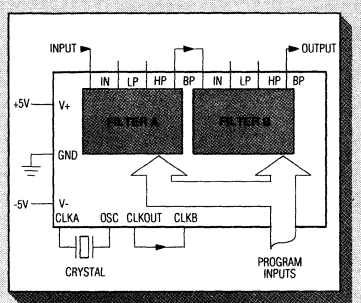
With a maximum full-scale output swing of 2.475Vrms, MAX270/271 wideband noise at 1kHz to 25kHz corner frequencies is good enough for 12- to 14-bit systems.

The MAX270/271 are completely self-contained, making them easy-to-use. No calculations are required because the programmable corner frequency is set without any external components. Simply pick one of the 127 codes between 1kHz and 25kHz by pin-strapping for fixed corner-frequency applications, or by writing a data word to the MAX270/271's μP interface for variable corner-frequency applications.

The MAX270 and MAX271 are identical, except the MAX271 adds a track-and-hold that can upgrade non-sampling, analog-to-digital converter designs to fast 500kHz sampling systems.

Universal-Filter Designs Offer μP or Pin-Strap Programmability

Frequency Range: 0.01Hz to 140kHz



MAX260/261/262 4th-order bandpass filter.

Maxim's MAX260 family of switched-capacitor filters realizes five filter functions with no precision external components required. Lowpass, bandpass, highpass, and allpass responses are obtained by selecting the appropriate output pin. Notch, a fifth response, is realized by summing the highpass and lowpass outputs. Center frequency (0.01Hz to 140kHz), Q, and operating mode are selected by microprocessor programming or pin-strapped logic inputs, requiring no hardware changes.

Typically, wideband noise is less than 100μVrms, and total harmonic distortion is better than 0.1%. This performance combined with the MAX260 family's flexibility satisfies diverse filter requirements.

6

ANALOG DESIGN GUIDE

1	Multiplexers, Switches, Military
2	Interface Products
3	Op Amps
4	DC-DC Converters, Power Supplies
5	μP Supervisory
6	Analog Filters
7	A/D Converters
8	High Speed: Video, Comparators
9	D/A Converters

MAXIM

Small 5th-Order Lowpass Filters With No DC Offset

Design High-Order Filters in Two Easy Steps

For circuit designs demanding accurate filtering with no DC offset, Maxim's new MAX280 and MAX281 offer compact solutions in miniDIP and small outline packages. The MAX280's Butterworth response has a flat frequency for audio, telecom, and dynamic signal analysis. The MAX281's Bessel response provides low overshoot and rapid settling, which is ideal for pulse and step input signals for weigh scale and multiplexed input source applications.

Both filters isolate the DC signal path and create a 5th pole (in addition to the four generated by the MAX280/281) with a single resistor and capacitor. The combination of a single resistor in the DC signal path and the 50pA of MAX280/281 bias current results in input-to-output offset voltages below a few microvolts.

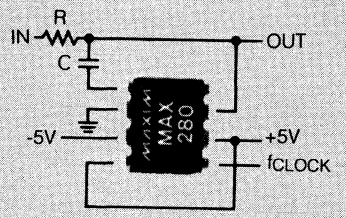
The MAX280/281 filter cutoff frequency (0.01Hz to 20kHz) is set in two easy steps: Select the corner frequency, then choose either the capacitor or resistor value. The 100:1 clock-to-cutoff frequency ratio results in clock ripple equal to 100 times the cutoff frequency, where it has either a negligible effect on circuit performance or can be easily removed. An external clock can be used for synchronous applications, while a capacitor generates an internal clock for asynchronous designs.

EASY 5TH-ORDER FILTER DESIGN IN TWO STEPS:

Step 1: Choose corner frequency and C.
Step 2: Calculate f_{CLOCK} and R.

DONE!

And DC offset is only a few microvolts!



★ FUTURE PRODUCTS ★

MAX274/MAX275 8th-/4th-Order, Continuous-Time Filters

Features:

- ♦ Quad/Dual 2nd-Order Sections
- ♦ Design Any All-Pole Response
- ♦ Bandpass or Lowpass Filtering
- ♦ Frequencies to: 150kHz (MAX274)
  300kHz (MAX275)
- ♦ Programmed with Only Four External Resistors
- ♦ Frequency Stable Over Temperature
- ♦ NO Clocking

MAX291/MAX292/MAX293 8th-Order Ladder Filters

Features:

- ♦ Butterworth Lowpass Filter (MAX291)
- ♦ Bessel Lowpass Filter (MAX292)
- ♦ Elliptic Lowpass Filter (MAX293)
- ♦ Corner Frequency Programmed by 100:1 Clock
- ♦ No External Resistors or Capacitors
- ♦ Cascadable for 16th-Order Rolloff

MAXIM

Analog Filters

Part Number	Description		Type*	Orders**	Class	Cutoff Frequency Range	Program Method	Price† 1000-up ($)
MAX270	Dual	Lowpass	CH	4	Continuous	1.0kHz to 25kHz	µP bus/pin strap	
MAX271	Dual + T/H	Lowpass	CH	4	Continuous	1.0kHz to 25kHz	µP bus/pin strap	
MAX274	Quad	Band/lowpass	BT, BL, CH	8	Continuous	100Hz to 150kHz	Resistor	††
MAX275	Dual	Band/lowpass	BT, BL, CH	4	Continuous	100Hz to 300kHz	Resistor	††
MAX260	Dual	Biquad	Universal	4	Switched capacitor	0.01Hz to 7.5kHz	µP bus	6.49
MAX261	Dual	Biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	µP bus	6.50
MAX262	Dual	Biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	µP bus	7.49
MAX263	Dual	Biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin strap	6.89
MAX264	Dual	Biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin strap	7.50
MAX265	Dual	Biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin/resistor	6.49
MAX266	Dual	Biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin/resistor	7.50
MAX267	Dual	Biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin strap	6.50
MAX268	Dual	Biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin strap	7.00
MAX280	Single	Lowpass	BT	5	Switched capacitor	0.01Hz to 20kHz	Clock, resistor, capacitor	4.87
MAX281	Single	Lowpass	BL	5	Switched capacitor	0.01Hz to 20kHz	Clock, resistor, capacitor	3.99
MAX291	Single	Lowpass	BT	8	Switched capacitor	1Hz to 25kHz	Clock	††
MAX292	Single	Lowpass	BL	8	Switched capacitor	1Hz to 25kHz	Clock	††
MAX293	Single	Lowpass	ET	8	Switched capacitor	1Hz to 25kHz	Clock	††

* BT = Butterworth, BL = Bessel, CH = Chebyshev, EL = Elliptic, Universal = All Filter Types
** Order level achieved by cascading all filters in package.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

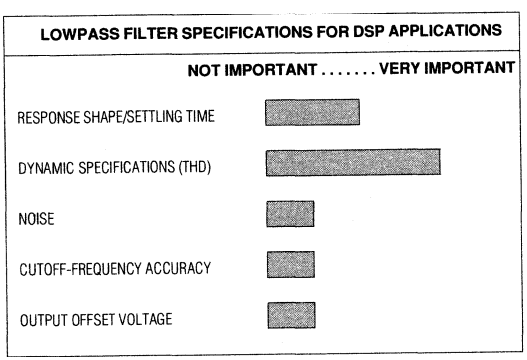
CHOOSE THE RIGHT LOWPASS FILTER

Filter design proceeds in two stages. First you express the desired filter response in terms of Q, order, corner frequency, and stop-band attenuation, then you "realize" the filter by converting the resulting specs into hardware. Most designers prefer the first task, which relates closely to their immediate application, rather than the second, which requires specialized expertise.

The realization expertise (and silicon) required for a given filter structure comes prepackaged in a monolithic lowpass filter. Such commercially available ICs—primarily switched-capacitor and non-switched programmable types—not only shrink the delay between filter definition and working prototype; they offer specifications guaranteed by the manufacturer. Many designers prefer this prepackaged approach over discrete-component design as a way to avoid restrictions such as pc-board layout sensitivity, component tolerances, and parameter drift vs. time and temperature.

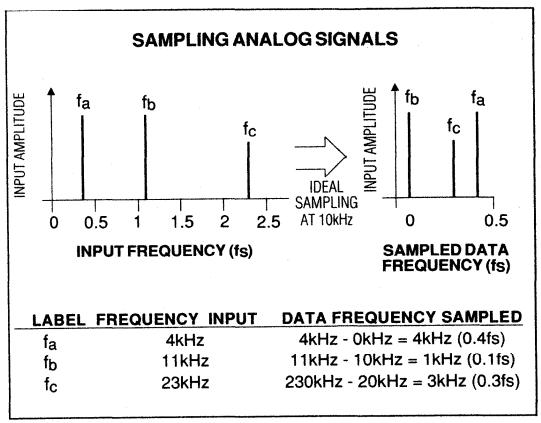
Monolithic filters greatly simplify system design, but you need to pay close attention to specifications when selecting them . Dynamic performance is critical in digital signal processing (DSP) systems, for example, but low offset voltage is more critical in DC measurements. No single filter satisfies all applications. The following discussion presents three typical lowpass-filter circuits, each stressing different specs for the monolithic filter.

DSP Applications



Examples of DSP Applications: speech processing, ultrasound, distortion analysis and other spectral measurements.

In a DSP system, incoming frequencies higher than the Nyquist limit (one-half the sampling rate) must be removed by lowpass filtering before admission to the A/D converter. If left in place, these frequencies fold back into the passband once they are digitized. As represented in the sampled data, such "alias" frequencies are indistinguishable from valid passband signals (Figure 1).



LABEL	FREQUENCY INPUT	DATA FREQUENCY SAMPLED
f_a	4kHz	4kHz - 0kHz = 4kHz (0.4fs)
f_b	11kHz	11kHz - 10kHz = 1kHz (0.1fs)
f_c	23kHz	230kHz - 20kHz = 3kHz (0.3fs)

Figure 1. Aliasing of Digitized Signals

A second lowpass filter should be included if the DSP system generates an analog output with a D/A converter. The converter's analog output is a staircase of quantized voltage steps occurring at the clock rate. To reproduce the desired output, a lowpass filter must "smooth" the analog signal by removing these clock-frequency components.

Any 10-bit sampling system exhibits quantization noise that limits the achievable signal-to-noise-and-distortion (SINAD) ratio to approximately 62dB. To maintain 10-bit accuracy, the anti-aliasing filter, A/D converter, D/A converter, and smoothing filter must provide a minimum net SINAD of 62dB.

In the 10-bit sampling system of Figure 3, the 12-bit sampling A/D converter (MAX167) provides two bits of "overhead." The D/A converter (MAX501B) contributes 12-bit resolution and 11-bit linearity, and the dual lowpass filter (MAX270) performs anti-aliasing and smoothing functions.

The system collects data at a 10kHz sampling rate for input frequencies to 1kHz. The anti-aliasing filter, with a 4th-order rolloff beginning at 2kHz (Figure 4), provides attenuation of input frequencies above the Nyquist frequency before they enter the A/D converter. The attenuation must insure that these alias frequencies (which contribute to distortion) do not degrade the system's overall SINAD. In this case, the anti-aliasing filter attenuates signals above the 5kHz Nyquist frequency by at least 35dB. When combined with natural rolloff in the input transducer and signal-conditioning circuitry (-30dB at

CHOOSE THE RIGHT LOWPASS FILTER

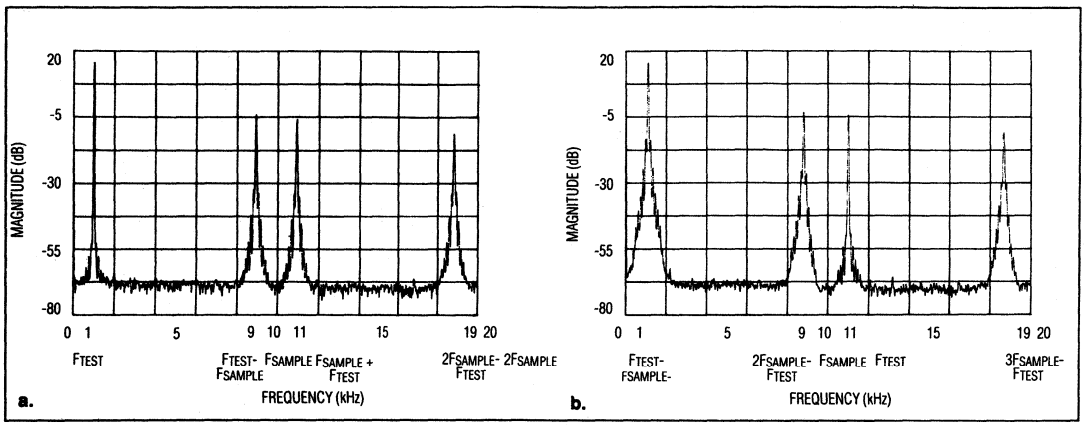


Figure 2. Without an anti-aliasing filter, the sampled 1kHz signal (a) is indistinguishable from the sampled 11kHz signal (b). Without a smoothing filter for the D/A converter output, the sampling creates spectral copies of the input spectrum that are mirrored around multiples of the sampling frequency. The signals shown are digitized at a sampling rate of 10kHz, then applied to a D/A converter with no output filtering.

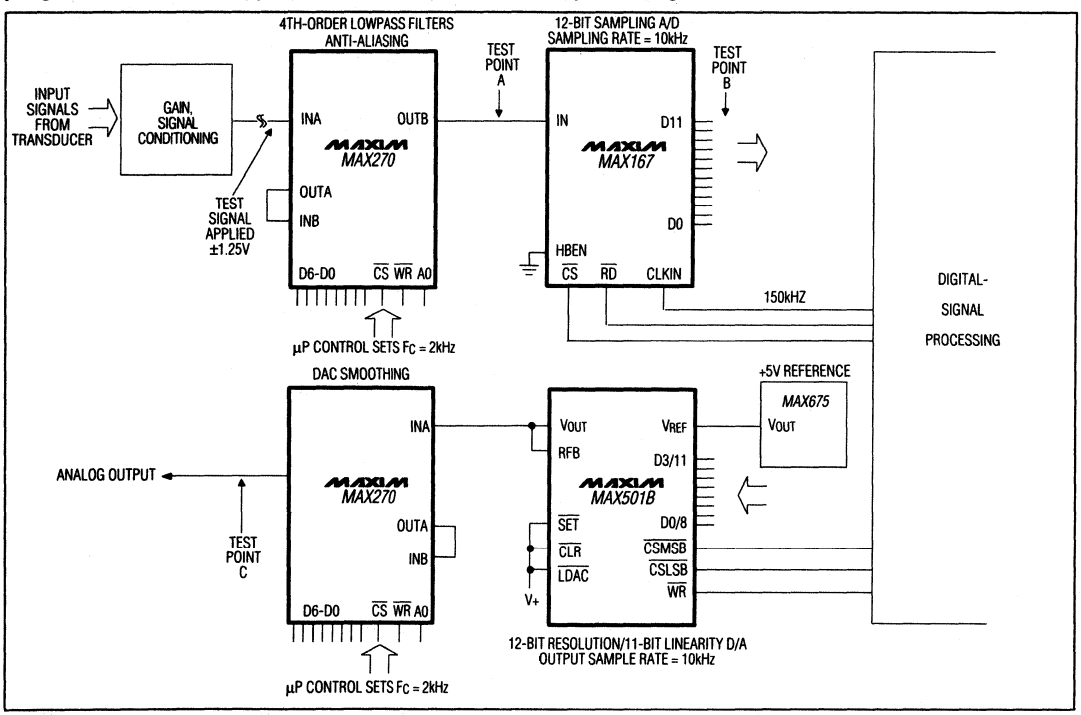


Figure 3. 10-Bit, 10kHz DSP System

CHOOSE THE RIGHT LOWPASS FILTER

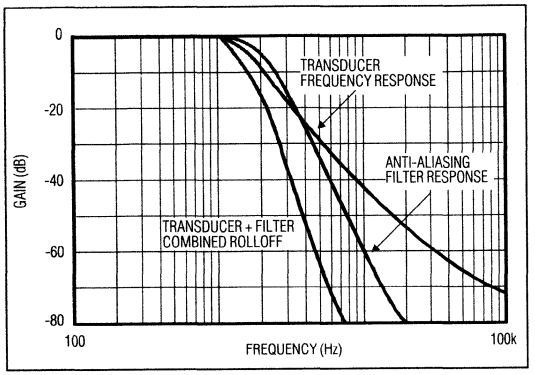


Figure 4. System Anti-Aliasing

5kHz), the resulting attenuation (-65dB) suppresses all alias components below the 10-bit accuracy level (-62dB).

Because digital filtering in the DSP hardware steeply attenuates frequencies above 1kHz, the D/A converter's smoothing filter is generally less critical than the anti-aliasing filter. The smoothing filter simply removes unwanted signals that are "mirrored" around the sampling frequency. The first of these (9kHz) must be attenuated below 62dB to maintain performance without affecting the frequencies below 1kHz; attenuation is greater for the higher-mirrored frequencies. This operation corresponds to the removal of "clocking steps" in the output waveform.

A fourth-order rolloff from 2kHz, identical to that of the anti-aliasing filter, provides an attenuation of -55dB at 9kHz, 7dB short of the 62dB required. But a glance at

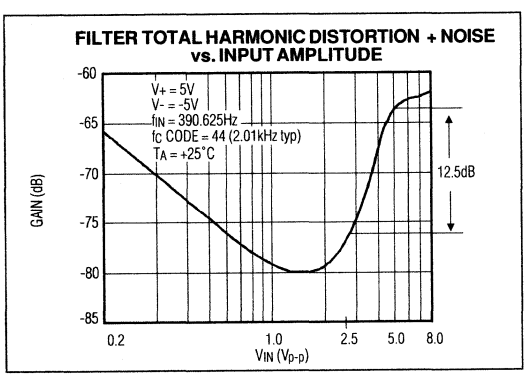


Figure 5. SNR of the noise floor dominates the MAX270's SINAD for low-amplitude signals. Higher signal levels introduce greater distortion, which limits the filter's SINAD.

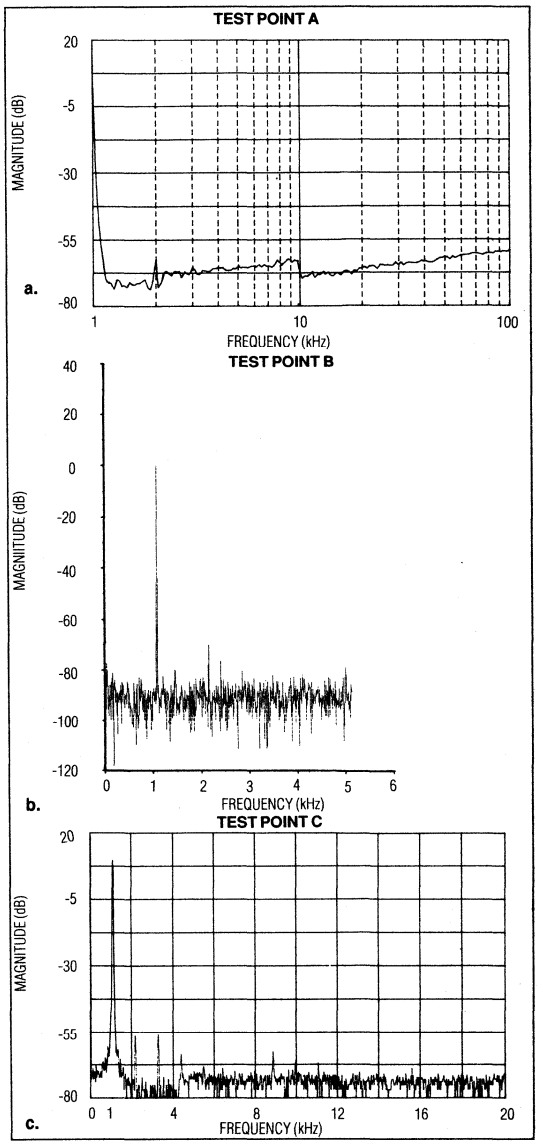


Figure 6. A pure 1kHz, ±1.25V test signal is applied to the system in Figure 3. These THD plots show distortion in the anti-aliasing filter (a), in the FFT performed on digital data from the A/D converter (b), and in the complete system, with the output looped back to the input of the anti-aliasing filter (c). All test points show true 10-bit performance, i.e. greater than 62dB SINAD.

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Figure 2 shows that signal frequencies mirrored around 10kHz are already 18dB lower than the fundamental test frequency. Their amplitudes are reduced by "sinc weighting" in accordance with the sinx/x function associated with step waveforms in the D/A converter's output signal. Because the extra attenuation adds to that of the smoothing filter, you can specify less rolloff in that filter.

For maximum dynamic range, the anti-aliasing and smoothing filters' output voltage swings should approach those of the data converters' input and output voltage ranges (±2.5V in this case). Reducing this system's voltage swing by a factor of two (to ±1.25V) yields an SNR loss of 6dB (corresponding to the unused MSB). With the 6dB loss, however, comes a gain of 12.5dB in terms of lower Total Harmonic Distortion (THD) in the filter (Figure 5).

Filter distortion increases sharply with output voltage swing. This effect is typical of all amplifiers, and the unity-gain voltage followers included in Sallen-Key filters (such as the MAX270) are somewhat prone to common-mode distortion at higher voltage swings. By lowering the swing from ±2.5V to ±1.25V, you reduce distortion by 12.5dB and increase the system's overall SINAD (limited by THD in the filter) by 6.5dB.

Spectral measurements taken at various points in the signal path of Figure 3 provide a true test of the circuit's dynamic performance (Figure 6).

Designed for critical dynamic applications, the MAX270 guarantees better than -70dB THD. Switched-capacitor filters have higher distortion, and to maintain SINAD they must filter clock noise with an external RC network. The MAX270, therefore, is the right filter in this case.

Dynamic Measurement Terms:

Total Harmonic Distortion (THD): the ratio of the rms sum of all input-signal harmonics (frequencies between DC and half the sample rate) to the rms amplitude of the fundamental frequency (the input test signal).

$$THD = 20\log \frac{\sqrt{\Sigma(V_1^2...V_n^2)}}{V_0}$$

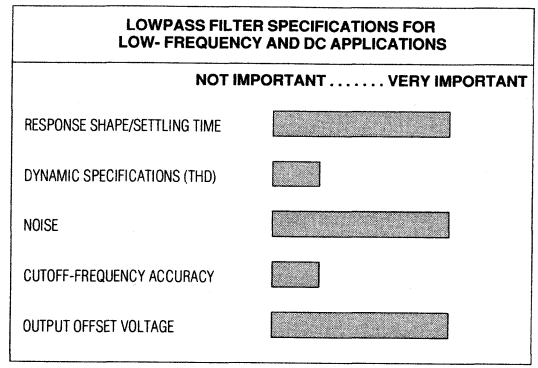
where V_0 is the rms amplitude of the fundamental and $V_1...V_n$ are amplitudes of the first through n^{th} harmonics.

Signal-to-Noise-and-Distortion (SINAD) ratio: the ratio between the rms amplitude of the fundamental input frequency (test signal) and the rms amplitude of all other signals (noise). SINAD is usually dominated by THD stemming from aberrations such as amplifier nonlinearity in the filters, or Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) errors in the A/D and D/A converters. But in systems with a high noise floor or exceptional linearity, noise itself can have a significant effect on SINAD.

Dynamic Range: the ratio of the largest allowable input signal to the smallest signal discernable above the system noise floor. Hence, dynamic range is usually a measure of noise.

The MAX274/MAX275, programmed with external resistors, offer lower distortion than the MAX270—typically better than -86dB THD—for higher resolution DSP applications.

Low-Frequency and DC Measurements



Examples of low-frequency and DC measurement applications: weigh scales, strain-gauge signals, bridge voltages.

Lowpass filters in DC measurements remove line noise (60Hz and harmonics), transducer noise, noise from switching power supplies, and noise from chopper op amps and other switching circuits.

The commercial weigh scale of Figure 7 features a ±20,000-count integrating A/D converter (MAX7129) capable of resolving 10µV on a 200mV scale. The converter drives a 4½-digit LCD and updates the reading at approximately 3Hz.

The MAX7129's built-in LCD drive eliminates the need for external LCD drivers, logic, and a microprocessor, but the device cannot pre-process digital data before it is displayed. Offset voltages cannot be subtracted in the digital domain, so you must minimize analog offset voltages before conversion. Full-scale gain and offsets from the weighing load cell are trimmed at the factory, so the scale is expected to operate without further calibration over all ambient temperature conditions.

Another concern is the two independent sources of noise in this system: the 60Hz line noise, and the 400Hz chopper noise emanating from op amps that amplify the transducer signals. Chopper noise is typically 200µV, with an assumed 10mV maximum of line noise at the output of the bridge amplifier. If fed directly into the A/D converter, this noise level would render the lower display digits useless.

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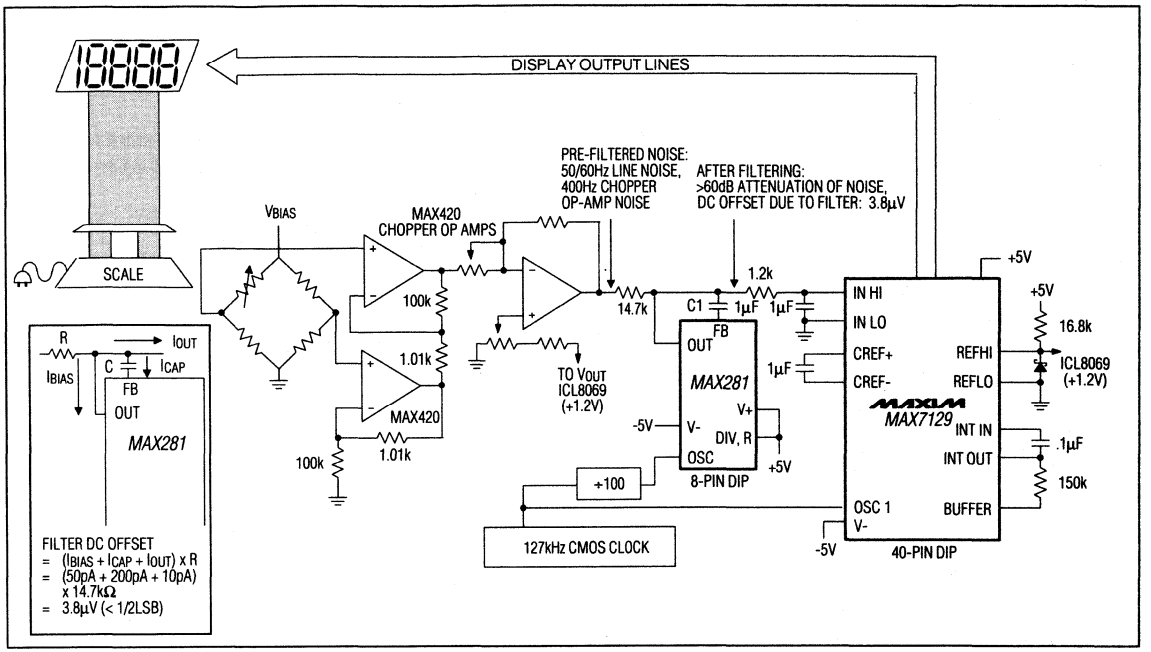


Figure 7. 4½-Digit Weigh Scale

Some of the noise is attenuated by the converter's integrating action (Figure 8). Unlike successive-approximation converters, the MAX7129 converts analog signals by integrating them for a fixed time period (1000 or 10,000 clock cycles, depending on the range setting). The voltage ramp resulting from integration is then deintegrated and compared to the reference voltage before the result is displayed on the LCD readout.

The noise rejection inherent in any integrating A/D converter follows a sinx/x (sinc) function. Nulls in the plot represent virtually 100% rejection functions and correspond to those frequencies that fit an integral number of cycles into the MAX7129's integrating period. Such frequencies are "integrated out."

A common practice is to clock the MAX7129 so its conversion period includes a whole number of 60Hz line cycles, thereby nulling the line noise. But if multiple noise frequencies are present (as in the weigh-scale system), choosing a clock frequency to null all of them becomes much trickier. The problem would be compounded if the manufacturer wished to market the scale in Europe, where the line frequency is 50Hz. Integration alone cannot remove 50Hz, 60Hz, and 400Hz noise from this system simultaneously.

The MAX281—a 5th-order, DC-accurate, Bessel lowpass filter—provides an ideal way to remove noise in the weigh-scale system while contributing virtually no DC

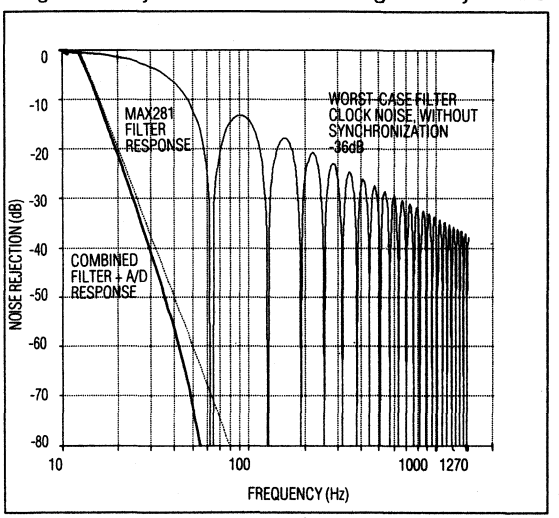


Figure 8. MAX129 Noise Rejection

CHOOSE THE RIGHT LOWPASS FILTER

offset (Figure 7). The filter's high order and low (12.6Hz) corner frequency (fc) guarantee at least 60dB of rejection for all relevant noise frequencies: -60dB at 50Hz, -68dB at 60Hz, and 80dB at 400Hz. The rejection combines with the sinc-filtering effect to provide more than 70dB attenuation at these freqencies.

Filtering thus reduces the 10mV line noise to about 3µV, or less than ½LSB. The filter's unique architecture virtually eliminates DC offset. R_1 and C_1 isolate the chip from the DC signal path, so only the AC portion of the signal is affected. R_1 and C_1 also form one of the filter poles and provide anti-aliasing for the filter.

Because the MAX281 is a switched-capacitor filter, its output exhibits about 10mV of noise at the clock frequency. This relatively high frequency (1.26kHz), unsynchronized with the A/D converter, is reduced approximately -36dB by the converter's integrating action (Figure 8). Further measures, however, must be added to reduce this noise below ½LSB.

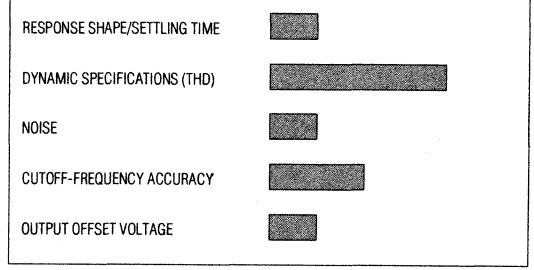
Placing an RC network at the filter output is a common way to reduce clock noise. The pole of this network should be at least a decade above the filter's cutoff frequency to avoid affecting the filter's response. With an internal clock-to-corner-frequency ratio of 101:1, a one-pole RC filter at 130Hz (10 times the cutoff frequency) guarantees 20dB of clock rejection at the clock frequency.

To remove any remaining clock noise from the measurement, synchronize the MAX7129 and MAX281 clock oscillators as shown in Figure 7. This scheme integrates out the clock noise by setting a null at 1.27kHz in the integrator's frequency response. The converter now integrates over exactly twenty cycles of the 1.27kHz waveform (or 200 cycles on the 200mV range).

The MAX281 is a maximally flat delay (Bessel) filter that settles faster than other types. Butterworth and Chebyshev filters, for example, tend to overshoot in response to an input step. When you place an item on the scale in Figure 7, the MAX281 filter settles to within ±0.0025% of final value (corresponding to ½LSB) in 150ms. Because the MAX7129 conversion time exceeds 250ms, this settling time assures a correct reading following the second conversion.

Analog Signal-Processing Applications

LOWPASS FILTER SPECIFICATIONS FOR ANALOG SIGNAL PROCESSING EXAMPLE: HIGH-PURITY SINEWAVE GENERATOR



Example: High-purity sine wave generator. Lowpass filter removes harmonics from generated sine waves.

A TTL counter, 8-channel multiplexer, and 4th-order lowpass filter generate 1kHz to 25kHz sinewaves with THD better than -80dB (Figure 9).

The sinewave frequency is a direct function of the external clocking frequency: $f_{SINE} = f_{CLK}/8$. Set the lowpass filter to the desired sine wave frequency, and apply a clock frequency eight times higher to the CLK input (Figure 9). Two resistive dividers provide input voltages to the multiplexer (mux). When the mux is switched through channels 0-7, the output yields an 8 times oversampled staircase approximation of a sine wave. Compared with a square wave, the 8 times oversampled waveform greatly simplifies smoothing-filter requirements by pushing the first significant harmonic out to seven times the fundamental. All higher-order harmonics are filtered to below -80dB by the MAX270, and the MAX270's uncommitted op amp sets the output level.

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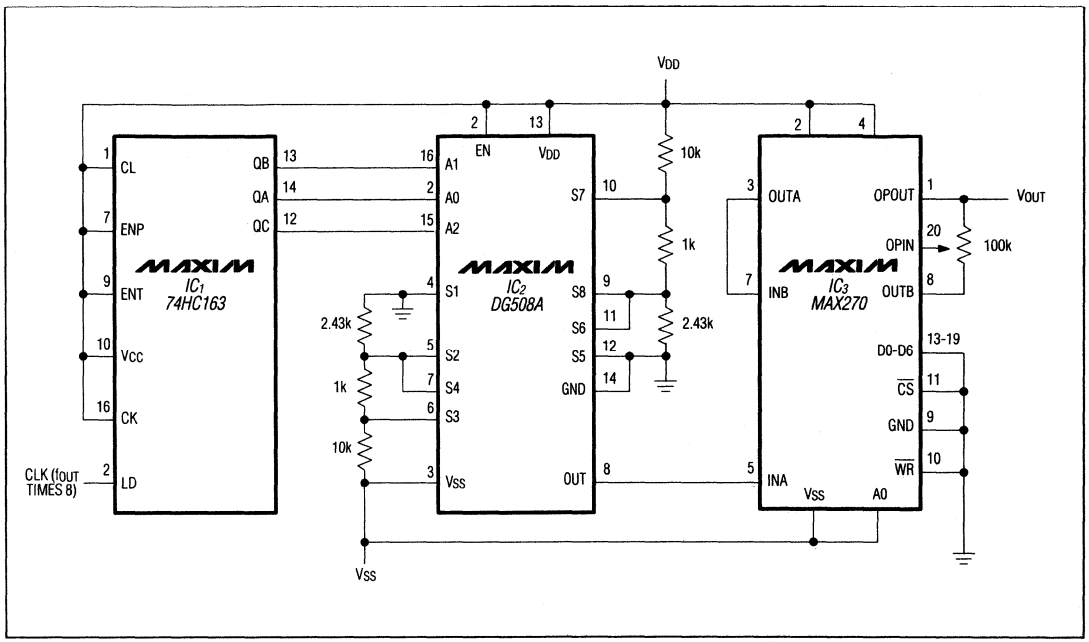


Figure 9. A TTL counter, 8-channel analog multiplexer, and 4th-order lowpass filter generate 1kHz to 25kHz sine waves with THD better than -80dB.

The circuit's gain accuracy is a function of the gain spec at the corner frequency, which is guaranteed between -2.4dB and -3.6dB at 1kHz. For tighter gain control, add the 100kΩ trimming potentiometer. The MAX270 specifies -70dB THD, but in this application the filter attenuates harmonics contributed by itself and the mux to below -80dB. For a worst-case calculation, consider the first harmonic (at 2kHz):

1) 1st harmonic distortion contribution from multiplexer: -64dB
2) 1st harmonic distortion contribution from 2 cascaded MAX270 sections:
   -70dB x 2 = -64dB
3) Sum of 1st harmonic distortion contributions:
   -64dB + -64dB = -58dB
4) Subtract 4th-order filter rolloff at 2kHz:
   6dB x 4 = 24dB (Approx.)
5) Resulting 1st harmonic after filtering:
   -82dB

CHOOSE THE RIGHT LOWPASS FILTER

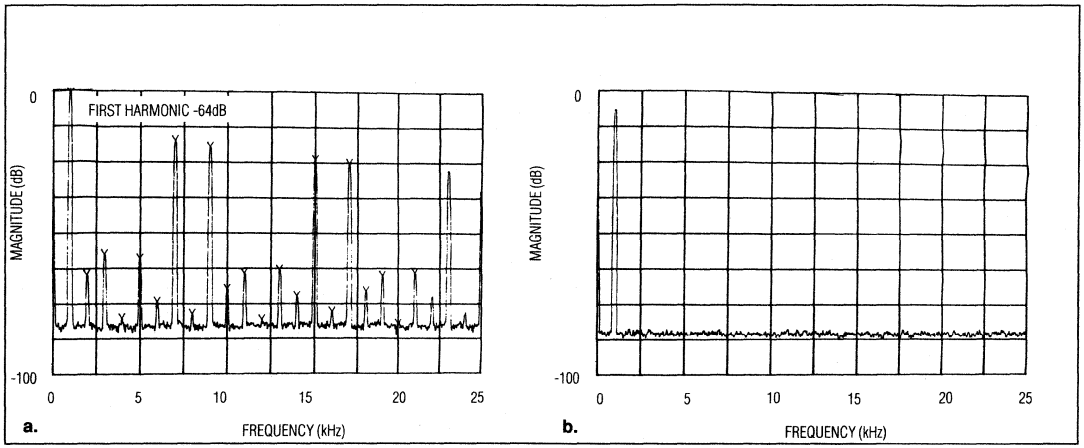


Figure 10. In the multiplexer output spectrum for a 1kHz signal (a), the approximation process generates large harmonics, while resistor divider errors cause small harmonics. The MAX270 attenuates all harmonics below the spectrum analyzer noise floor (b).

Table 1. Maxim Lowpass Filter Comparison

MAXIM LOWPASS FILTER COMPARISON					
Filter	**MAX270/271**	**MAX280**	**MAX281**	**MAX274**	**MAX275**
Response Shape	0.1dB Chebyshev	Butterworth	Bessel	Resistor Programmed	Resistor Programmed
Corner-Frequency Range	1kHz to 25kHz	0.1Hz to 25kHz	0.1Hz to 25kHz		
Order per IC	4	5	5	8	4
Dynamic Specifications	-70dB THD @ 390Hz	Not specified	Not specified	-86dB THD @ 1kHz typ	-86dB THD @ 1kHz typ
Noise	$38\mu V_{rms}$	Dom. by clock	Dom. by clock		
Cutoff-Frequency Accuracy	±10% @ 25kHz	Better, function of clock frequency, ext., R,C	Better, function of clock frequency, ext., R,C	±0.9%	±0.9%
Output Offset Voltage	±2mV	0V	0V	±125mV	±125mV

MAXIM

Microprocessor Programmable Universal Active Filters

General Description

The MAX260/261/262 CMOS dual second-order universal switched-capacitor active filters allow microprocessor control of precise filter functions. No external components are required for a variety of bandpass, lowpass, highpass, notch and allpass configurations. Each device contains two second-order filter sections which place center frequency, Q, and filter operating mode under programmed control.

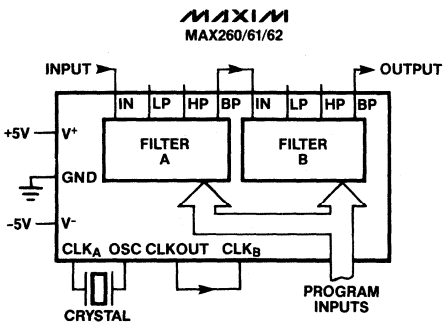
An input clock, along with a 6-bit f_0 program input, determine the filter's center or corner frequency without affecting other filter parameters. The filter Q is also programmed independently. Separate clock inputs for each filter section operate with either a crystal, RC network, or external clock generator.

The MAX260 has superior offset and DC specifications than the MAX261 and MAX262 and a center frequency (f_0) range of 7.5kHz. The MAX261 handles center frequencies to 57kHz while the MAX262 extends the center frequency range to 140kHz by employing lower clock-to-f_0 ratios. All devices are available in 24-pin DIP and small outline packages in commercial, extended, and military temperature ranges.

Applications

- μP Tuned Filters
- Anti-Aliasing Filters
- Digital Signal Processing
- Adaptive Filters
- Signal Analysis
- Phase-Locked Loops

Functional Diagram



Fourth-Order Bandpass Filter

Features

- ◆ **Filter Design Software Available**
- ◆ **Microprocessor Interface**
- ◆ **64-Step Center Frequency Control**
- ◆ **128-Step Q Control**
- ◆ **Independent Q and f_0 Programming**
- ◆ **Guaranteed Clock to f_0 Ratio—1% (A grade)**
- ◆ **75kHz f_0 Range (MAX262)**
- ◆ **Single +5V and ±5V Operation**

Ordering Information

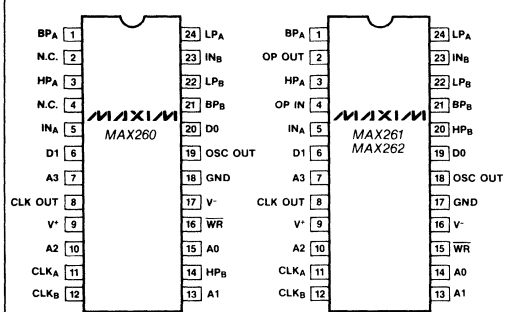
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX260ACNG	0°C to +70°C	Plastic DIP	1%
MAX260BCNG	0°C to +70°C	Plastic DIP	2%
MAX260AENG	-40°C to +85°C	Plastic DIP	1%
MAX260BENG	-40°C to +85°C	Plastic DIP	2%
MAX260ACWG	0°C to +70°C	Wide SO	1%
MAX260BCWG	0°C to +70°C	Wide SO	2%
MAX260AMRG	-55°C to +125°C	CERDIP	1%
MAX260BMRG	-55°C to +125°C	CERDIP	2%
MAX261ACNG	0°C to +70°C	Plastic DIP	1%

** All devices—24-pin packages 0.3" wide packages*

Ordering Information Continued on Last Page

Pin Configuration

Top View



Microprocessor Programmable Universal Active Filters

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^--0.3V to V^++0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
CERDIP (derate 12.5mW/°C above 70°C) 1000mW
Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
MAX260/261/262XCXG ..... 0°C to +70°C
MAX260/261/262XEXG ..... -40°C to +85°C
MAX260/261/262XMXG ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	$T_A = T_{MIN}$ to T_{MAX}	MAX260A		±0.2	±1.0	%
		MAX260B		±0.2	±2.0	
		MAX261/62A		±0.2	±1.0	
		MAX261/62B		±0.2	±2.0	
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	$T_A = T_{MIN}$ to T_{MAX}					%
	Q = 0.5 to 16	MAX260A		±1	±5	
	Q = 0.5 to 16	MAX260B		±1	±10	
	Q = 32	MAX260A		±2	±10	
	Q = 32	MAX260B		±2	±15	
	Q = 64	MAX260A		±4	±15	
	Q = 64	MAX260B		±4	±22	
	Q = 0.5 to 16	MAX261/62A		±1	±5	
	Q = 0.5 to 16	MAX261/62B		±1	±10	
	Q = 32	MAX261/62A		±2	±10	
	Q = 32	MAX261/62B		±2	±15	
	Q = 64	MAX261/62A		±4	±15	
	Q = 64	MAX261/62B		±4	±22	
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX260A		±0.1	±0.2	dB
		MAX260B		±0.1	±0.3	
		MAX261/62A		±0.1	±0.25	
		MAX261/62B		±0.1	±0.5	
Gain Temperature Coefficient	Lowpass (at D.C.)	MAX260		-5		ppm/°C
		MAX261/62		-5		
	Bandpass (at f_0)	MAX260/61/62		+20		
Offset Voltage At Filter Outputs—LP, BP, HP (Note 3)	$T_A = T_{MIN}$ to T_{MAX}, Q = 4 Mode 1					V
		MAX260A		±0.05	±0.25	
		MAX260B		±0.15	±0.45	
		MAX261A		±0.40	±0.90	
		MAX261B		±0.80	±1.60	
		MAX262A		±0.40	±0.90	
		MAX262B		±0.80	±1.60	
	Mode 3	MAX260A		±0.075	±0.30	
		MAX260B		±0.075	±0.50	
		MAX261A		±0.50	±1.00	
		MAX261B		±0.90	±1.60	
		MAX262A		±0.50	±1.00	
		MAX262B		±0.90	±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 $T_A = T_{MIN}$ to T_{MAX}			±0.75		mV/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP 4th-Order LP (Fig. 26) 4th-Order BP (Fig. 24)			See Typ. Oper. Char. 90 100		μV_{RMS}
Harmonic Distortion at f_0	Q = 4, V_{IN} = 1.5V_{PP}			-57		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX} CMOS Level Logic Inputs	MAX260 MAX261 MAX262		15 16 16	20 20 20	mA
Shutdown Supply Current	$Q0_A$-$Q6_A$ = all 0, CMOS Level Logic Inputs (Note 5)			1.5		mA
INTERNAL AMPLIFIERS						
Output Signal Swing (Note 6)	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source Sink			50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/μs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 250kHz for the MAX260 and 1MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 7)		
Maximum Clock Frequency				(Note 7)		
f_{CLK}/f_0 Ratio Error (Notes 1, 8)	Q = 8	MAX26XA MAX26XB		±0.1 ±0.1	1 2	%
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 8)	Q = 8 f_{CLK}/f_0 = 199.49 f_{CLK}/f_0 = 199.49 f_{CLK}/f_0 = 139.80	MAX260A MAX260B MAX261A MAX261B MAX262A MAX262B		±2 ±2 ±2 ±2 ±2 ±2	±5 ±10 ±5 ±10 ±5 ±10	%
Output Signal Swing	All Outputs (Note 6)			±2		V
Power Supply Current	CMOS Level Logic Inputs (Note 5)			7		mA
Shutdown Current	CMOS Level Logic Inputs (Note 5)			0.35		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 199.49 on the MAX260/61, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 139.8 on the MAX262.

Note 2: Q accuracy tested at Q = 0.5, 1, 2, 4, 8, 16, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.

Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 175kHz for the MAX260 and 750kHz for the MAX261/262.

Note 4: Output noise is measured with an RC output smoothing filter at 4 × f_0 to remove clock feedthrough.

Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. CMOS logic levels are: HIGH = 5V, LOW = 0V. Power supply current is typically 4mA higher with TTL logic and clock input levels.

Note 6: On the MAX260 only, the HP output signal swing is typically 0.75V less than the LP or BP outputs.

Note 7: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.

Note 8: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V however these parameters are only tested to the extent indicated by the MIN or MAX limits.

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INTERFACE SPECIFICATIONS (Note 9)

(V^+ = +5V, V^+ = -5V, T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ Pulse Width	t_{WR}		250	150		ns
Address Setup	t_{AS}		25			ns
Address Hold	t_{AH}		0			ns
Data Setup	t_{DS}		100	50		ns
Data Hold	t_{DH}		10	0		ns
Logic Input High	V_{IH}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}	2.4			V
Logic Input Low	V_{IL}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_B CLK_A $T_A = T_{MIN}$ to T_{MAX}		6	10 60	µA
Input Capacitance	C_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B			15	pF

Note 9: Interface timing specifications are guaranteed by design and are not subject to test.

Pin Description

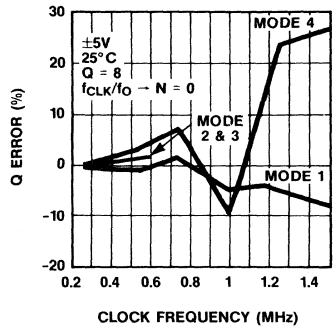
MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
9	9	V^+	Positive supply voltage
17	16	V^-	Negative supply voltage
18	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
11	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
12	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
8	8	CLK OUT	Clock Output for crystal and R-C oscillator operation
19	18	OSC OUT	Connects to crystal or R-C for self clocked operation

MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
5,23	5,23	IN_A,IN_B	Filter inputs
1,21	1,21	BP_A,BP_B	Bandpass outputs
24,22	24,22	LP_A,LP_B	Lowpass outputs
3,14	3,20	HP_A,HP_B	Highpass/Notch/Allpass outputs
16	15	$\overline{WR}$	Write Enable input
15,13, 10,7	14,13, 10,7	A0,A1 A2,A3	Address inputs for f_0 and Q input data locations
20,6	19,6	D0,D1	Data inputs for f_0 and Q programming
	2	OP OUT	Output of uncommitted op-amp on MAX261/62 only. Pin 2 is a no-connect on the MAX260
	4	OP IN	Inverting input of uncommitted op-amp on MAX261/62 only (Non-inverting input is internally connected to ground). Pin 4 is a no-connect on the MAX260.

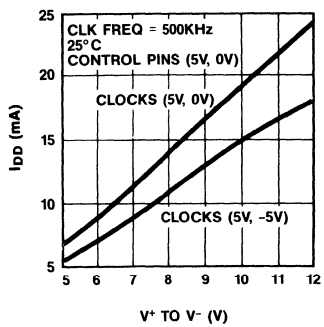
Microprocessor Programmable Universal Active Filters

Typical Operating Characteristics

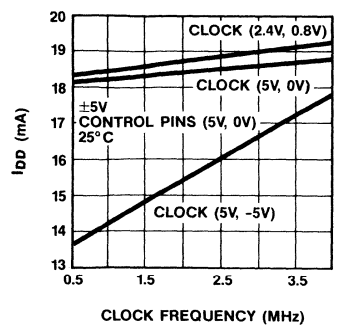
Q ERROR vs CLOCK FREQUENCY MAX260



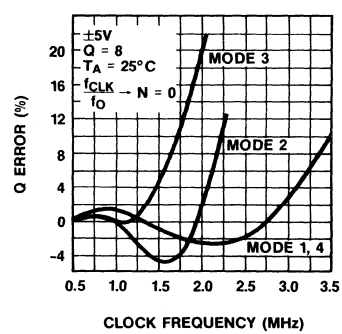
I_{DD} vs POWER SUPPLY VOLTAGE



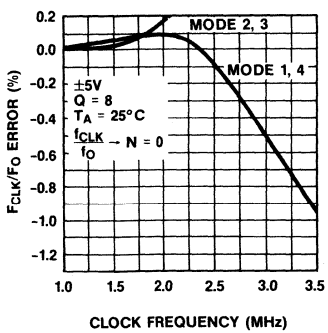
I_{DD} vs CLOCK FREQUENCY



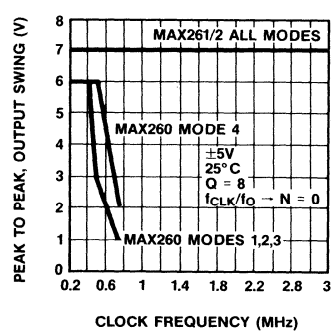
Q ERROR vs CLOCK FREQUENCY MAX261/2



F_{CLK}/F_O ERROR vs CLOCK FREQUENCY MAX261/2



OUTPUT SIGNAL SWING vs CLOCK FREQUENCY



Wideband RMS Noise (db ref. to 2.47V_{RMS}, 7V_{p-p}) **±5V Supplies**

	Mode	Q = 1			Q = 8			Q = 64		
		LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
MAX261/2	1	-84	-90	-84	-80	-82	-85	-72	-73	-85
	2	-88	-90	-88	-84	-82	-84	-77	-73	-76
	3	-84	-90	-88	-80	-82	-82	-73	-73	-74
	4	-83	-89	-84	-79	-81	-85	-71	-73	-85
MAX260	1	-87	-89	-86	-81	-81	-86	-73	-73	-86
	2	-89	-88	-85	-83	-80	-82	-75	-72	-74
	3	-87	-88	-85	-80	-82	-80	-71	-72	-72
	4	-87	-88	-86	-81	-80	-86	-71	-72	-86

Notes:
1. f_{CLK} = 1 MHz for MAX261/2, f_{CLK} = 350kHz for MAX260
2. f_{CLK}/f_0 ratio programmed at N = 63 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX261.

Noise Spectral Distribution
(MAX261, f_{CLK} = 1 MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3 KHz	-87	-87	-86
C Message Weighted	-93	-93	-93

6

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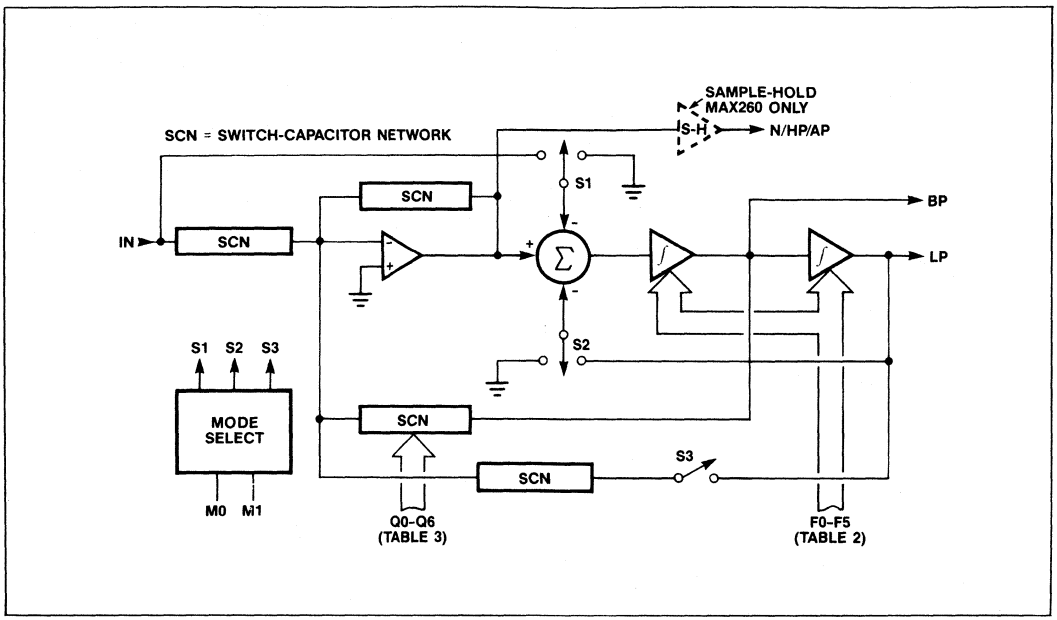

Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX260/61/62 contains two second-order switched-capacitor active filters. Figure 1 shows the filter's state variable topology, employed with two cascaded integrators and one summing amplifier. The MAX261 and MAX262 also contain an uncommitted amplifier. On-chip switches and capacitors provide feedback to control each filter section's f_0 and Q. Internal capacitor ratios are primarily responsible for the accuracy of these parameters. Although these switched-capacitor networks (SCN) are in fact sampled systems, their behavior very closely matches that of continuous filters, such as RC active filters. The ratio of the clock frequency to the filter center frequency (f_{CLK}/f_0) is kept large so that ideal second-order state-variable response is maintained.

The MAX262 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX260 or MAX261 to allow higher operating f_0 frequencies and signal bandwidths. These reduced sample rates result in somewhat more deviation from ideal continuous filter parameters than with the MAX260/61. However, these differences can be compensated using Figure 20 (See "Applications Hints") or Maxim's filter design software.

The MAX260 employs auto-zero circuitry not included in the MAX261 or 262. This provides improved DC characteristics, and improved low frequency performance at the expense of high end f_0 and signal bandwidth. The N/HP/AP outputs of the MAX260 are internally sample-and-held, as a result of its auto-zero operation. Signal swing at this output is somewhat reduced as a result (MAX260 only). See Table 1 for bandwidth comparisons of the three filters.

Maxim also provides design programs which aid in converting filter response specifications into the f_0 and Q program codes used by the MAX260 series devices. This software also precompensates f_0 and Q when low sample rates are used.

It is important to note that in all MAX260 series filters, the filter's internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Quick Look Design Procedure

The MAX260, MAX261 and MAX262, with Maxim's filter design software, greatly simplifies the design procedures for many active filters. Most designs can be realized using a three step process described in this section. If the design software is not used, or if the filter complexity is beyond the scope of this section, refer to the remainder of this data sheet for more detailed applications and design information.

```
100  AB$="FILTER A " : GOSUB 150 : REM GET DATA FOR SECTION A
110  ADD = 0 : GOSUB 220 : REM WRITE DATA TO THE PRINTER PORT
120  AB$="FILTER B " : GOSUB 150 : REM GET DATA FOR B
130  ADD = 32 : GOSUB 220 : REM WRITE DATA TO PRINTER PORT
140  GOTO 100
150  PRINT "MODE (1 to 4, see Table 5) "; AB$; : INPUT M
160  IF M<1 OR M>4 THEN GOTO 150
170  PRINT "CLOCK RATIO (0 to 63, N of Table 2) "; AB$; : INPUT F
180  IF F<0 OR F>63 THEN GOTO 170
190  PRINT "Q (0 to 127, N of Table 3) "; AB$; : INPUT Q
200  IF Q<0 OR Q>127 THEN GOTO 190 ELSE : PRINT
210  RETURN
220  LPRINT CHR$(ADD+M-1); : ADD = ADD+4
230  FOR I = 1 TO 3
240  X=(ADD + (F - 4*INT(F/4))) : LPRINT CHR$(X);
250  F=INT(F/4) : ADD = ADD + 4
260  NEXT I
270  FOR I = 1 TO 4
280  X=(ADD + (Q - 4*INT(Q/4))) : LPRINT CHR$(X);
290  Q=INT(Q/4) :: ADD = ADD + 4
300  NEXT I
310  RETURN
```

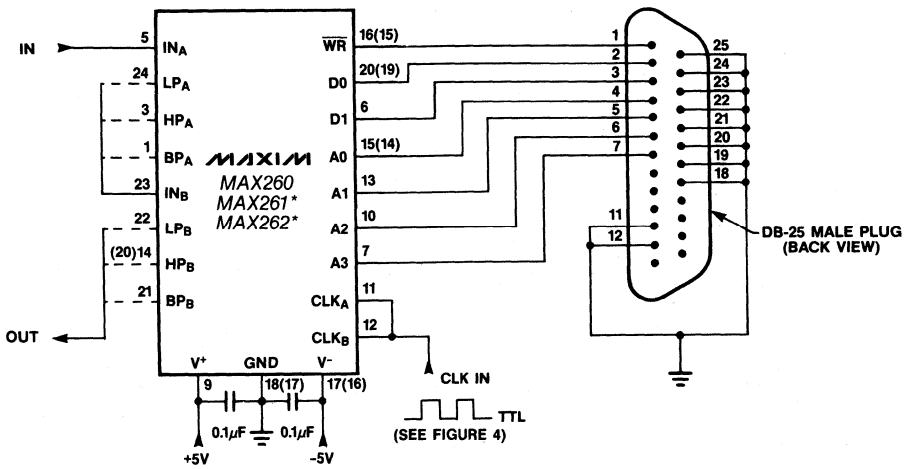

Figure 2. Basic Program and Hardware Connections to Parallel Printer Port for "Quick Look" Using a Personal Computer.

Step 1—Filter Design

Start with the program "PZ" to determine what type of filter is needed. This helps determine the type (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and calculates the pole/zero (f_0) and Q values for each second-order section. Each MAX260/61/62 contains two second-order sections and devices may be cascaded for higher order filters.

Step 2—Generate Programming Coefficients

Starting with the f_0 and Q values obtained in Step 1, use the program "MPP" to generate the digital coefficients which program each second-order section's f_0 and Q. The program displays values for "N" ("N = __ for f_0" and "N = __ for Q"). N is the decimal equivalent of the binary code that sets the filter section's f_0 or Q. These are the same "N"s that are listed in Tables 2 and 3.

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An input clock frequency and filter "Mode" must also be selected in this step, however if a specific clock rate is not selected, "GEN" will pick one. With regard to mode selection, Mode 1 is the most convenient choice for most bandpass and lowpass filters. Exceptions are elliptic bandpass and lowpass filters which require Mode 3. Highpass filters also use Mode 3, while allpass filters use Mode 4. For further information regarding these filter modes see "Filter Operating Modes" in this data sheet.

Step 3—Loading the Filter

When the N values for the f_0 and Q of each second-order filter section are determined, the filter can then be programmed and operated. What follows is a convenient method of programming the filter and evaluating a design if a personal computer is available.

A short Basic program loads data into the MAX260/261/262 via the personal computer's parallel printer port. The program asks for the filter Mode as well as the N values for the f_0 and Q of each section. These coefficients are then loaded into the filter in the form of ASCII characters. This program may be used with or without Maxim's other filter design software. The program and the appropriate hardware connections for a Centronics type printer port are shown in Figure 2.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ will calculate the pole frequencies, Q's, zeros, and the number of stages needed.

Program MPP. For programmed filters, MPP computes the input codes to use and describes the expected performance of the design.

Program FR. When a design of one or more stages is completed, FR checks the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Program PR.BAS Allows a MAX260/61/62 to be programmed via a personal computer. The Mode, f_0, and Q of each section are typed in, and the proper codes are sent to the filter via the computer's parallel printer port. This program is also provided in Figure 2.

Other design programs are also included for use with other Maxim filter products.

Other Filter Products

Maxim has developed a number of other filter products in addition to the MAX260, MAX261 and MAX262:

PIN PROGRAMMABLE ACTIVE FILTERS—A dual second-order universal filter that needs no external components. A Microprocessor interface is not required.

MAX263 0.4Hz to 30kHz f_0 range
MAX264 1Hz to 75kHz f_0 range

RESISTOR AND PIN PROGRAMMABLE FILTERS—A dual second-order universal filter where f_0 adjustment beyond pin-programmable resolution employs external resistors.

MAX265 0.4Hz to 30kHz f_0 range. Includes two uncommitted op-amps.
MAX266 1Hz to 75kHz f_0 range. Includes two uncommitted op-amps.
MF10 Industry Standard. Resistor Programmed Only

PIN PROGRAMMABLE BANDPASS FILTERS—A dual second-order bandpass that needs no external components. A Microprocessor interface is not required.

MAX267 0.4Hz to 30kHz f_0 range

MAX268 1Hz to 75kHz f_0 range

PROGRAMMABLE ANTI-ALIAS FILTER—A programmable dual second-order continuous (not switched) lowpass filter. No clock noise is generated. Designed for use as an anti-alias filter in front of, or as a smoothing filter following, any sampled filter or system.

MAX270 1kHz to 25kHz Cutoff Frequency Range

5th ORDER LOW PASS FILTER—Features zero offset and drift errors for designs requiring high DC accuracy.

MAX280, LT1062 0.1Hz to 20kHz Cutoff Frequency Range

Detailed Description

f_0 and Q Programming

Figure 3 shows a block diagram of the MAX260. Each 2nd-order filter section has its own clock input and independent f_0 and Q control. The actual center frequency is a function of the filter's clock rate, 6-bit f_0 control word (see Table 2), and operating Mode. The Q of each section is also set by a separate programmed input (see Table 3). This way each half of a MAX260/61/62 is tuned independently so that complex filter polynomials can be realized. Equations which convert program code numbers to f_{CLK}/f_0 and Q values are listed in the notes beneath Tables 2 and 3.

Table 1. Typical Clock and Center Frequency Limits

PART	Q	MODE	f_{CLK}	f_0
MAX260	1	1	1Hz-400kHz	0.01Hz-4.0kHz
	1	2	1Hz-425kHz	0.01Hz-6.0kHz
	1	3	1Hz-500kHz	0.01Hz-5.0kHz
	1	4	1Hz-400kHz	0.01Hz-4.0kHz
	8	1	1Hz-500kHz	0.01Hz-5.0kHz
	8	2	1Hz-700kHz	0.01Hz-10.0kHz
	8	3	1Hz-700kHz	0.01Hz-5.0kHz
	8	4	1Hz-600kHz	0.01Hz-4.0kHz
	64	1	1Hz-750kHz	0.01Hz-7.5kHz
	90	2	1Hz-500kHz	0.01Hz-7.0kHz
	64	3	1Hz-400kHz	0.01Hz-4.0kHz
	64	4	1Hz-750kHz	0.01Hz-7.5kHz
MAX261	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz

PART	Q	MODE	f_{CLK}	f_0
MAX261	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz
MAX262	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

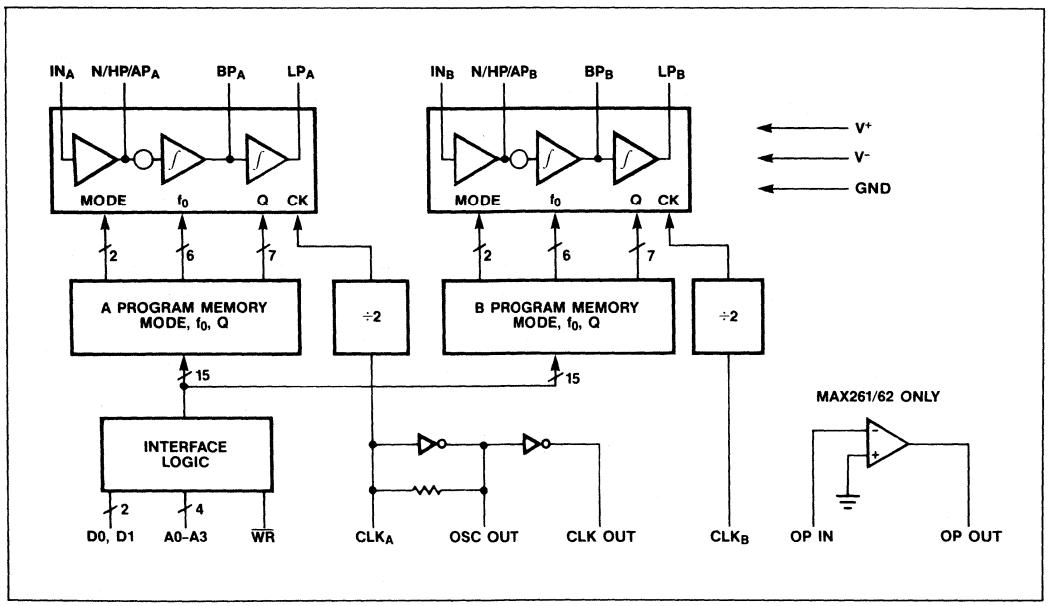

Figure 3. MAX260/61/62 Block Diagram

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Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0	0
102.10	72.20	42.41	29.99	1	0	0	0	0	0	1
103.67	73.31	43.98	31.10	2	0	0	0	0	1	0
105.24	74.42	45.55	32.21	3	0	0	0	0	1	1
106.81	75.53	47.12	33.32	4	0	0	0	1	0	0
108.38	76.64	48.69	34.43	5	0	0	0	1	0	1
109.96	77.75	50.27	35.54	6	0	0	0	1	1	0
111.53	78.86	51.84	36.65	7	0	0	0	1	1	1
113.10	79.97	53.41	37.76	8	0	0	1	0	0	0
114.67	81.08	54.98	38.87	9	0	0	1	0	0	1
116.24	82.19	56.55	39.99	10	0	0	1	0	1	0
117.81	83.30	58.12	41.10	11	0	0	1	0	1	1
119.38	84.42	59.69	42.21	12	0	0	1	1	0	0
120.95	85.53	61.26	43.32	13	0	0	1	1	0	1
122.52	86.64	62.83	44.43	14	0	0	1	1	1	0
124.09	87.75	64.40	45.54	15	0	0	1	1	1	1
125.66	88.86	65.97	46.65	16	0	1	0	0	0	0
127.23	89.97	67.54	47.76	17	0	1	0	0	0	1
128.81	91.80	69.12	48.87	18	0	1	0	0	1	0
130.38	92.19	70.69	49.98	19	0	1	0	0	1	1
131.95	93.30	72.26	51.10	20	0	1	0	1	0	0
133.52	94.41	73.83	52.20	21	0	1	0	1	0	1
135.08	95.52	75.40	53.31	22	0	1	0	1	1	0
136.66	96.63	76.97	54.43	23	0	1	0	1	1	1
138.23	97.74	78.53	55.54	24	0	1	1	0	0	0
139.80	98.86	80.11	56.65	25	0	1	1	0	0	1
141.37	99.97	81.68	57.76	26	0	1	1	0	1	0
142.94	101.08	83.25	58.87	27	0	1	1	0	1	1
144.51	102.89	84.82	59.98	28	0	1	1	1	0	0
146.08	103.30	86.39	61.09	29	0	1	1	1	0	1
147.65	104.41	87.96	62.20	30	0	1	1	1	1	0
149.23	105.52	89.54	63.31	31	0	1	1	1	1	1
150.80	106.63	91.11	64.42	32	1	0	0	0	0	0
152.37	107.74	92.68	65.53	33	1	0	0	0	0	1
153.98	108.85	94.25	66.64	34	1	0	0	0	1	0
155.51	109.96	95.82	67.75	35	1	0	0	0	1	1
157.08	111.07	97.39	68.86	36	1	0	0	1	0	0
158.65	112.18	98.96	69.98	37	1	0	0	1	0	1
160.22	113.29	100.53	71.09	38	1	0	0	1	1	0
161.79	114.41	102.10	72.20	39	1	0	0	1	1	1
163.36	115.52	102.67	73.31	40	1	0	1	0	0	0
164.93	116.63	105.24	74.42	41	1	0	1	0	0	1
166.50	117.74	106.81	75.53	42	1	0	1	0	1	0
168.08	118.85	108.38	76.64	43	1	0	1	0	1	1
169.65	119.96	109.96	77.75	44	1	0	1	1	0	0
171.22	121.07	111.53	78.86	45	1	0	1	1	0	1
172.79	122.18	113.10	79.97	46	1	0	1	1	1	0
174.36	123.29	114.66	81.08	47	1	0	1	1	1	1

Table 2. f_{CLK}/f_0 Program Selection Table (Continued)

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
175.93	124.40	116.24	82.19	48	1	1	0	0	0	0
177.50	125.51	117.81	83.30	49	1	1	0	0	0	1
179.07	126.62	119.38	84.41	50	1	1	0	0	1	0
180.64	127.73	120.95	85.53	51	1	1	0	0	1	1
182.21	128.84	122.52	86.64	52	1	1	0	1	0	0
183.78	129.96	124.09	87.75	53	1	1	0	1	0	1
185.35	131.07	125.66	88.86	54	1	1	0	1	1	0
186.92	132.18	127.23	89.97	55	1	1	0	1	1	1
188.49	133.29	128.81	91.08	56	1	1	1	0	0	0
190.07	134.40	130.38	92.19	57	1	1	1	0	0	1
191.64	135.51	131.95	93.30	58	1	1	1	0	1	0
193.21	136.62	133.52	94.41	59	1	1	1	0	1	1
194.78	137.73	135.09	95.52	60	1	1	1	1	0	0
196.35	138.84	136.66	96.63	61	1	1	1	1	0	1
197.92	139.95	138.23	97.74	62	1	1	1	1	1	0
199.49	141.06	139.80	98.85	63	1	1	1	1	1	1

Notes: 1) For the MAX260/61, $f_{CLK}/f_0 = (64 + N)\pi/2$ in Mode 1, 3, and 4, where N varies from 0 to 63.
2) For the MAX262, $f_{CLK}/f_0 = (26 + N)\pi/2$ in Mode 1, 3, and 4, where N varies 0 to 63.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$. The functions are then:
MAX260/61 $f_{CLK}/f_0 = 1.11072\ (64 + N)$, MAX262 $f_{CLK}/f_0 = 1.11072\ (26 + N)$

Table 3. Q Program Selection Table

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.500*	0.707*	0*	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1

Notes: 4) * Writing all 0s into Q0A-Q6A on Filter A activates a low power shutdown mode. BOTH filter sections are deactivated. Therefore this Q value is only achievable in filter B.

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Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)

6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

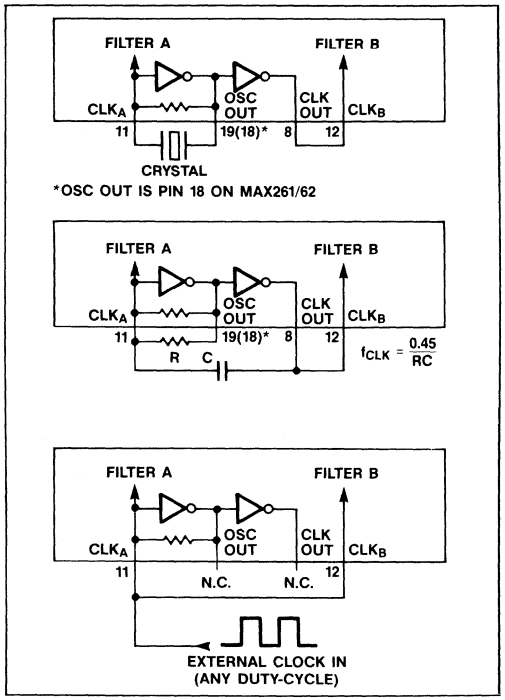

Figure 4. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX260/61/62 can operate with a crystal, resistor-capacitor (RC) network, or an external clock generator as shown in Figure 4. If an RC oscillator is used, the clock rate, f_{CLK}, nominally equals 0.45/RC.

The duty cycle of the clock at CLK_A and CLK_B is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Microprocessor Interface

f_0, Q, and Mode selection data is stored in an internal program memory. The memory contents are updated by writing to addresses selected by A0-A3. D0 and D1 are the data inputs. A map of the memory locations is shown in Table 4. Data is stored in the selected address on the rising edge of $\overline{WR}$. Address and data inputs are TTL and CMOS compatible when the filter is powered from ±5 volts. With other power supply voltages, CMOS logic levels should be used. Interface timing is shown in Figure 5. Note: Clock inputs CLK_A and CLK_B have no relation to the digital interface. They control the switched-capacitor filter sample rate only.

Some noise may be generated on the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

Table 4. Program Address Locations

DATA BIT		ADDRESS				LOCATION
D0	D1	A3	A2	A1	A0	
FILTER A						
$M0_A$	$M1_A$	0	0	0	0	0
$F0_A$	$F1_A$	0	0	0	1	1
$F2_A$	$F3_A$	0	0	1	0	2
$F4_A$	$F5_A$	0	0	1	1	3
$Q0_A$	$Q1_A$	0	1	0	0	4
$Q2_A$	$Q3_A$	0	1	0	1	5
$Q4_A$	$Q5_A$	0	1	1	0	6
$Q6_A$		0	1	1	1	7
FILTER B						
$M0_B$	$M1_B$	1	0	0	0	8
$F0_B$	$F1_B$	1	0	0	1	9
$F2_B$	$F3_B$	1	0	1	0	10
$F4_B$	$F5_B$	1	0	1	1	11
$Q0_B$	$Q1_B$	1	1	0	0	12
$Q2_B$	$Q3_B$	1	1	0	1	13
$Q4_B$	$Q5_B$	1	1	1	0	14
$Q6_B$		1	1	1	1	15

Note: Writing 0 into $Q0_A$-$Q6_A$ (address locations 4-7) on Filter A activates shutdown mode. BOTH filter sections deactivate.

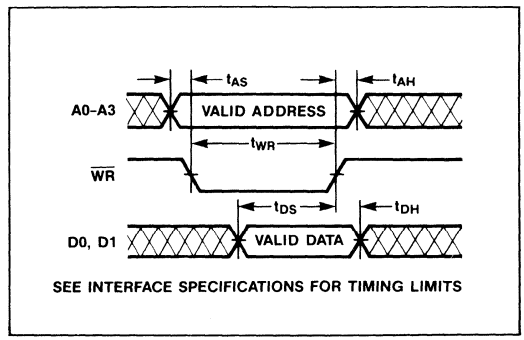

Figure 5. Interface Timing

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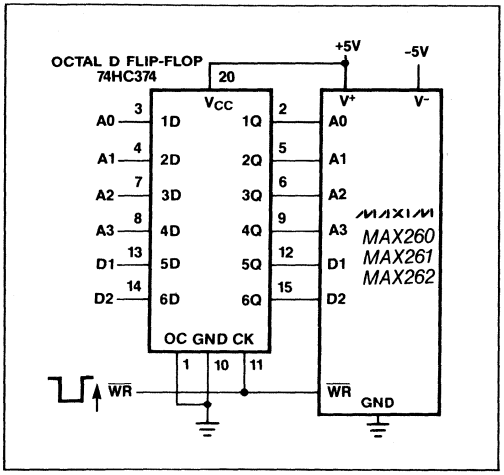

Figure 6. Buffering/Latching Logic Inputs

Shutdown Mode

The MAX260/61/62 enters a shutdown/standby mode when all zeroes are written to the Q addresses of filter A ($Q0_A$-$Q6_A$). When shut down, power consumption with ±5V supplies typically drops to 10mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes

There are several ways in which the summing amplifier and integrators in each MAX260/61/62 filter section can be configured. The four most versatile interconnections (modes) are selected by writing to inputs M0 and M1 (See Tables 4 and 5). These modes use no external components. A fifth mode, 3A, makes use of an additional op-amp (included in the MAX261 and 262) and external resistors but uses the same internal configuration, and is selected with the same programming code, as Mode 3.

Figures 7 through 11 show symbolic representations of the MAX260 filter modes. Only one second-order section is shown in each case. The A and B sections of one MAX260/61/62 can be programmed for different modes if desired. The f_0, f_N (notch), Q, and various output gains in each case are shown in Table 5.

Filter Mode Selection

MODE 1 (Figure 7) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc.. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

Mode 1, along with Mode 4, supports the highest clock frequencies (See Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 7). The gain of the lowpass and notch outputs

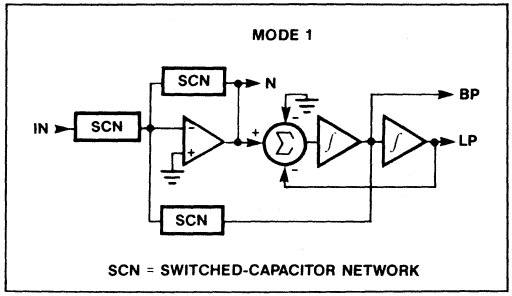

Figure 7. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

Table 5. Filter Modes for Second-Order Functions

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \to 0$)	H_{ON2} ($f \to f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes: f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op-amp.

MODE 2 (Figure 8) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (See Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (See Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together. This is demonstrated in the Wide Passband Chebyshev Bandpass design example.

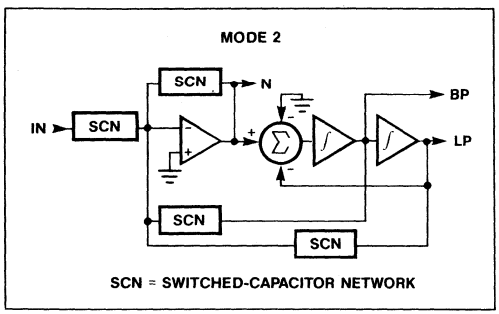

Figure 8. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

MODE 3 (Figure 9) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with MODE 1 (See Table 1).

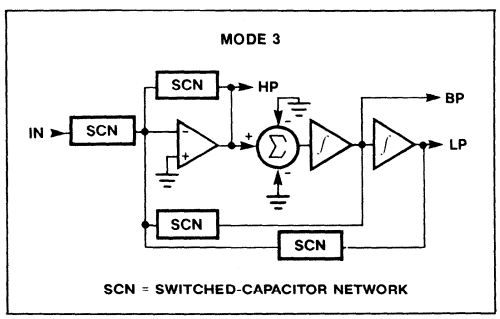

Figure 9. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

MODE 3A (Figure 10) uses a separate op-amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op-amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

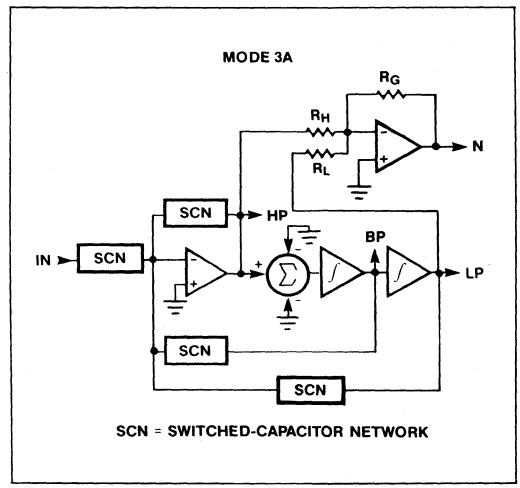

Figure 10. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used

MODE 4 (Figure 11) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (See Figure 20).

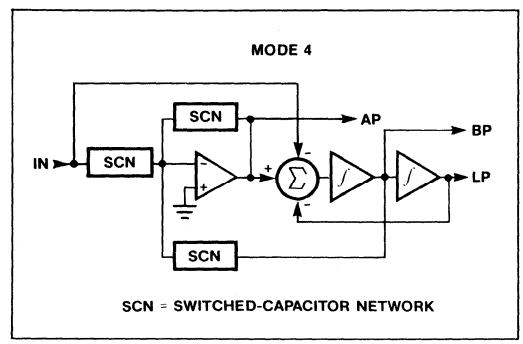

Figure 11. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

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Description of Filter Functions

BANDPASS (Figure 12)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (See Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP} \frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_o$

f_0 = $\omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 13)

$$G(s) = H_{OLP} \frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 14)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP} \frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

NOTCH (Figure 15)

Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

f_n = $\omega_n/2\pi$

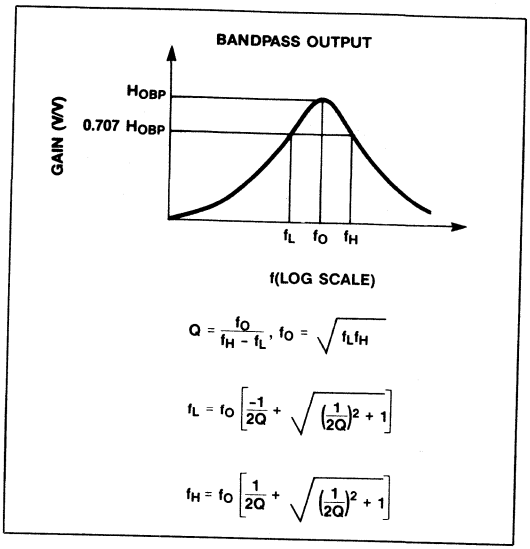

Figure 12. Second-Order Bandpass Characteristics

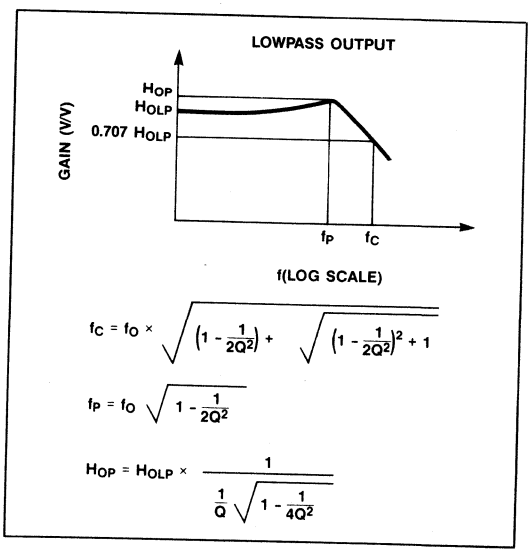

Figure 13. Second-Order Lowpass Characteristics

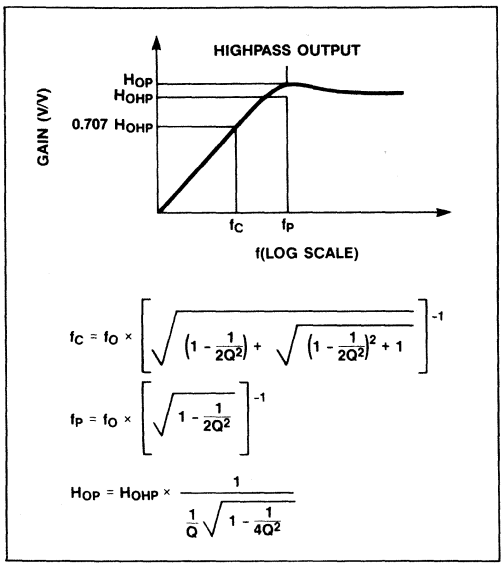

Figure 14. Second-Order Highpass Characteristics

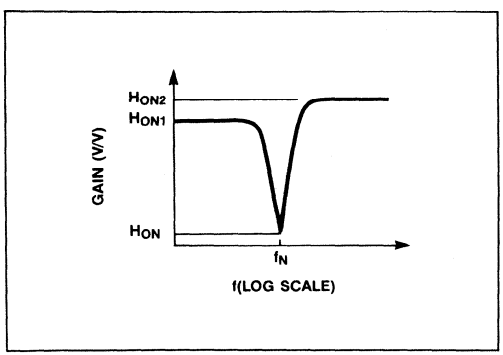

Figure 15. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for DC < f < $f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the MAX260/61/62. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 20 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 6, the total Q and bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

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In high order bandpass filters, stages with different f_0s and Qs are also often cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$H_1(f_{0BP}) = H(f_{01})/G_1$ = Section 1's Gain at f_{0BP}

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{OBP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times$ etc.

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\ [(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{1Z} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

Application Hints

Power Supplies

The MAX260/61/62 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±5V dual supplies. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or biased to $V^+/2$. Figure 16 shows circuit connections for single supply operation.

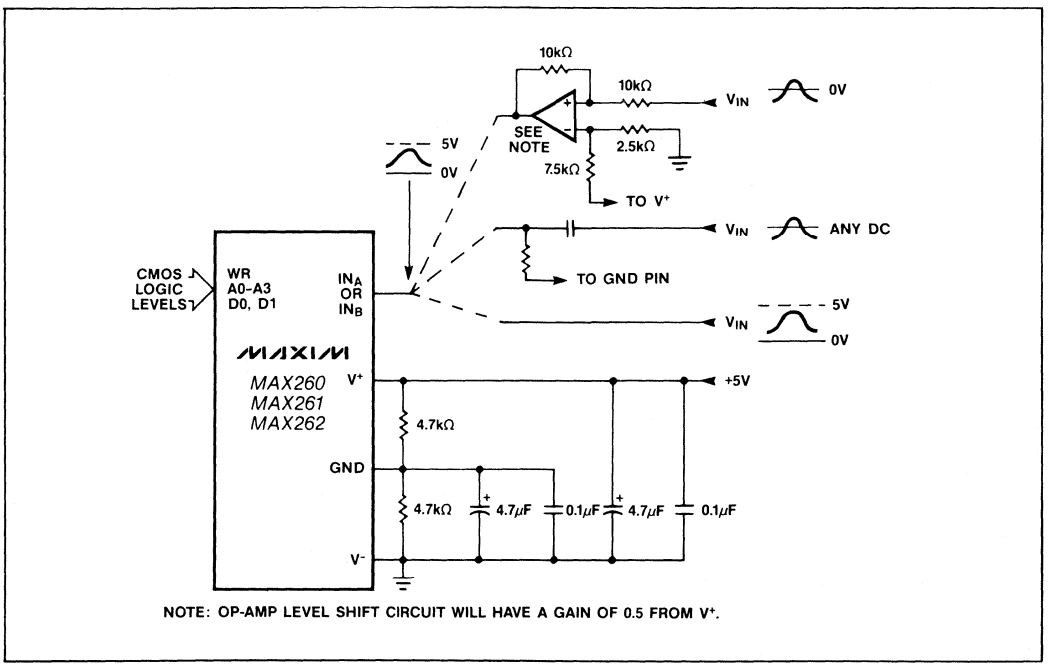

Figure 16. Power Supply and Input Connections for Single Supply Operation

When power supplies other than ±5V are used, CMOS input logic levels (HIGH = V^+, LOW = GND or V^-) are required for $\overline{WR}$, D0-D1, A0-A3, CLK_A and CLK_B. With ±5V supplies, either TTL or CMOS levels can be used. Note however that power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum is preferred.) and 0.1µF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 16.

Output Swing and Clipping

MAX260/61/62 outputs are designed to drive 10kΩ loads. For the MAX261 and MAX262, all filter outputs swing to within 0.15V of each supply rail with a 10kΩ load. In the MAX260 only, an internal sample-hold circuit reduces voltage swing at the N/HP/AP output compared to LP and BP. N/HP/AP therefore swings to within 1V (10kΩ load) of either rail on the MAX260.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example lets assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

Clock Feedthrough and Noise

Typical wideband noise for MAX260 series devices is $0.5mV_{pp}$ from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX260 series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This can also be attenuated with an RC smoothing filter as shown with the MAX261 in Figure 17.

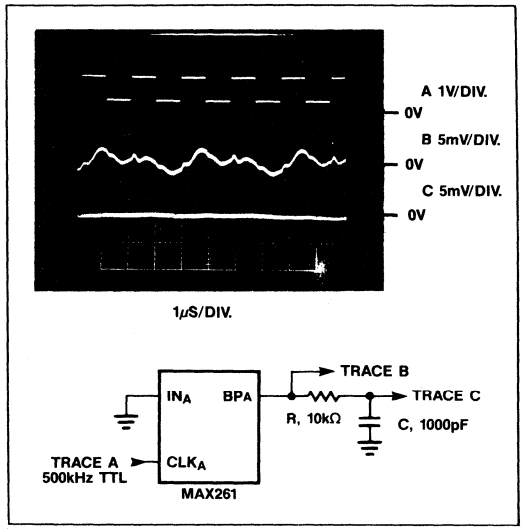

Figure 17. MAX261 Bandpass Output Clock Noise

Some noise also may be generated at the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

Input Impedance

The input to each filter is the switched capacitor circuit shown in Figure 18. In the MAX260, the input capacitor charges to the input voltage V_{IN} during the first half clock cycle. During the second half-cycle its charge is transferred to the feedback capacitor. The resultant input impedance can be approximated by:

$$R_{IN} = 1/(C_{IN}f_{CLK}/2) = 2/(C_{IN}f_{CLK}).$$

C_{IN} is around 12pF, hence for a clock frequency of 500kHz, R_{IN} = 333kΩ. The input also has about 5pF of fixed capacitance to ground.

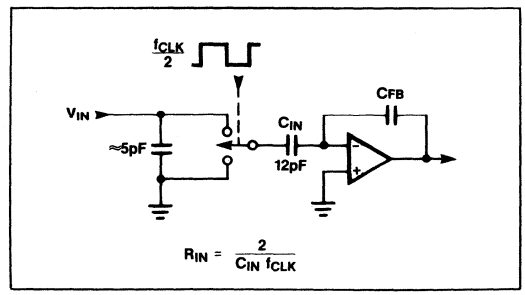

Figure 18. MAX260 Input Model

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The MAX261/262 input structure is shown in Figure 19. Here C_A = 12pF and C_B = 0.016pF and only C_B is switched, so the input resistance is 750 times larger compared to the MAX260 (R_{IN} = 250MΩ). The MAX261/62 has a fixed capacitance of approximately 5pF to ground.

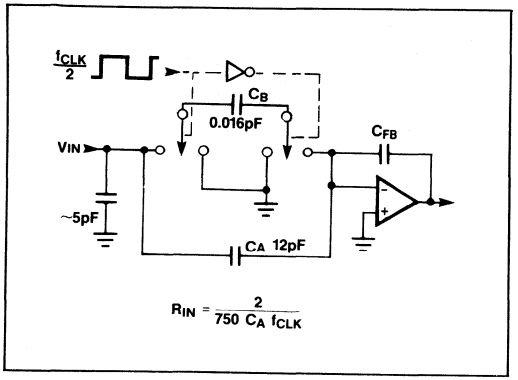


Figure 19. MAX261/262 Input Model

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 20 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX260 series devices and in fact occur with all types of sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX262 does employ a lower range of f_{CLK}/f_0 ratios than the MAX260 or MAX261 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 20 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 20 applies for Modes 1 and 3. When using Figure 20 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

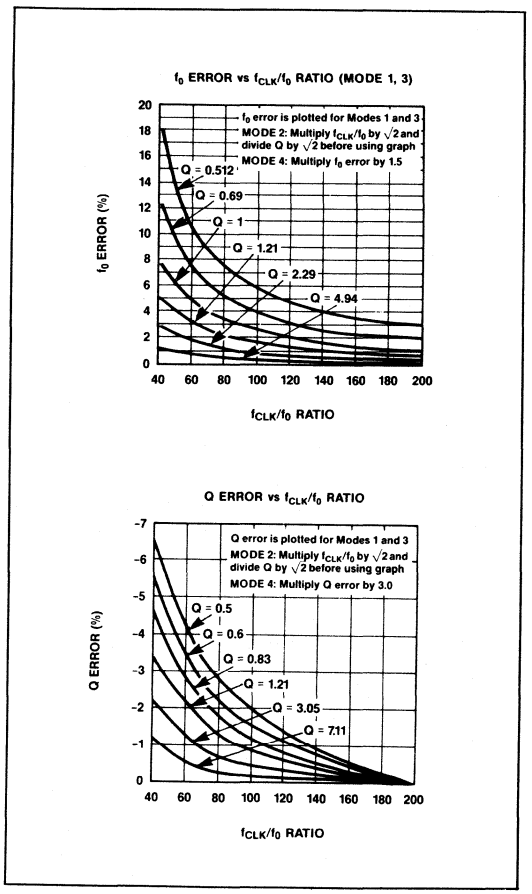


Figure 20. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX260 series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

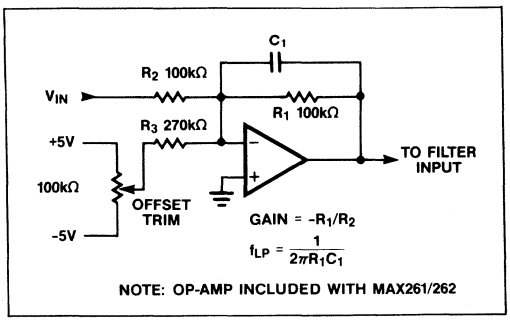


Figure 21. Circuit for DC Offset Adjustment

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX262 uses lower f_{CLK}/f_0 ratios than the MAX260/61 and for this reason is more likely to require input filtering than the MAX260 or MAX261.

Trimming DC Offset

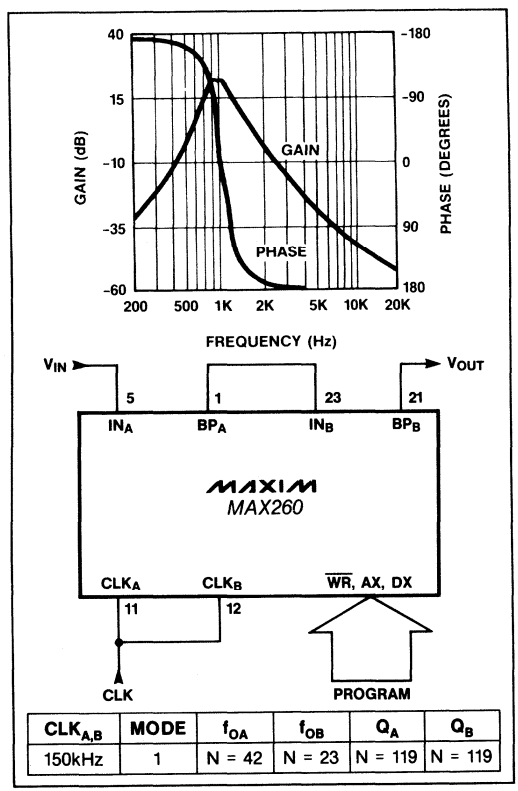
The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 21. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

Design Examples

Fourth-Order Chebyshev Bandpass Filter

Figure 22 shows both halves of a MAX260 cascaded to form a fourth-order Chebyshev bandpass filter. The desired parameters are:

Center frequency (f_0)	= 1 kHz
Pass bandwidth	= 200 Hz
Stop Bandwidth	= 600 Hz
Max. passband ripple	= 0.5 dB
Min. stopband Attenuation	= 15 dB



$CLK_{A,B}$	MODE	f_{OA}	f_{OB}	Q_A	Q_B
150kHz	1	N = 42	N = 23	N = 119	N = 119

Figure 22. Fourth-Order Chebyshev Bandpass Filter

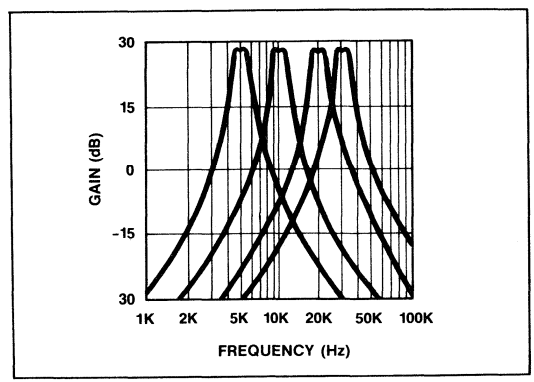


Figure 23. MAX261 Fourth-Order Chebyshev Bandpass Using Coefficients of Figure 22.)

From the above parameters, the order (number of poles), and the f_0 and Q of each section can be determined. Such a derivation is beyond the scope of this data sheet, however there are a number of sources which provide design data for this procedure. These include look-up tables, design texts and computer programs. Design software is available from Maxim to provide comprehensive solutions for most popular filter configurations. The A and B section parameters for the above filter are:

f_{0A} = 904 Hz f_{0B} = 1106 Hz
Q_A = 7.05 Q_B = 7.05

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To implement this filter, both halves operate in Mode 1 and use the same clock. See selection Tables 2 and 3. The programmed parameters are:

$CLK_A = CLK_B = 150$ kHz
$f_{CLK}/f_{0A} = 166.50$ (Mode 1, N=42), actual $f_{0A} = 902.4$Hz
$f_{CLK}/f_{0B} = 136.66$ (Mode 1, N=23), actual $f_{0B} = 1099.7$Hz
$Q_A = Q_B = 7.11$ (Mode 1, N=119)

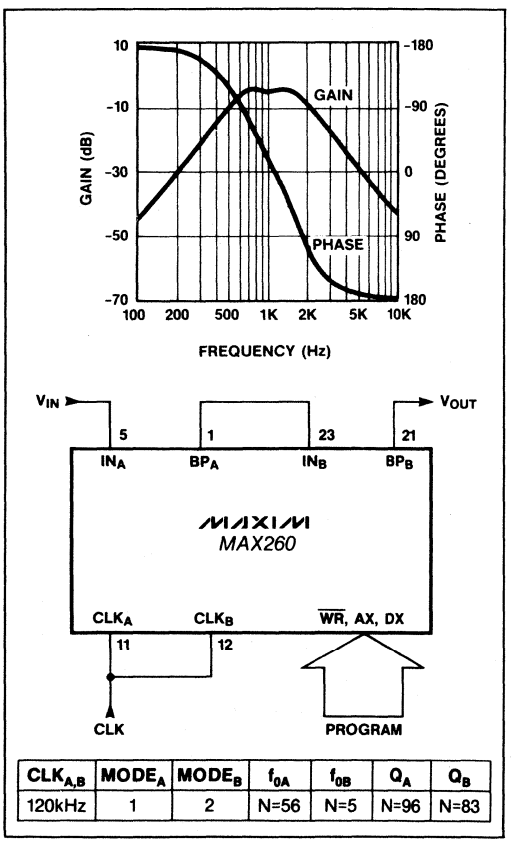
Sampling errors are very small at this f_{CLK}/f_0 ratio so the actual realized Q is very close to 7.05 (See Figure 20 or Filter Program MPP). Often the realized Q will not be exactly the target value at high Qs because programming resolution lowers as Q increases. This doesn't affect most filter designs, since 3-digit Q accuracy is practically never required, and a Q resolution of 1 is provided up to Qs of 10. The overall filter gain at f_0 is 16.4V/V or 24.3dB (See Cascading Filters section). If another gain is required, amplification or attenuation must be added at the input, output, or between stages.

In Figure 23, a series of response curves are shown for the above configuration using a MAX261 with clock frequencies ranging from 750kHz to 4MHz (f_0 from 500Hz to 30kHz). Note that the rightmost curve shows about 2dB of gain peaking compared to the lower frequency curves, indicating the upper limit of usable filter accuracy at this Q (See Table 1)

Wide Passband Chebyshev Bandpass

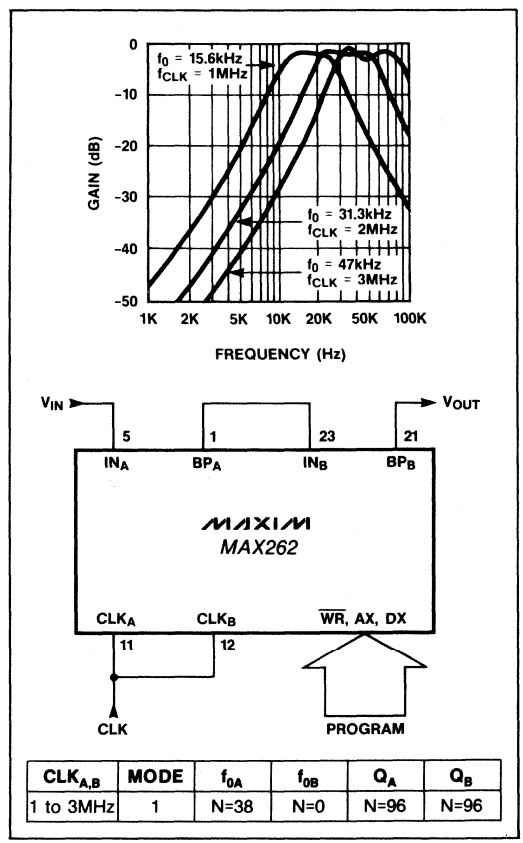
In this example (Figure 24) the desired parameters are:

Center frequency (f_0)	= 1 kHz
Pass bandwidth	= 1 kHz
Stop bandwidth	= 3 kHz
Max passband ripple	= 1 dB
Min stopband Attenuation	= 20 dB



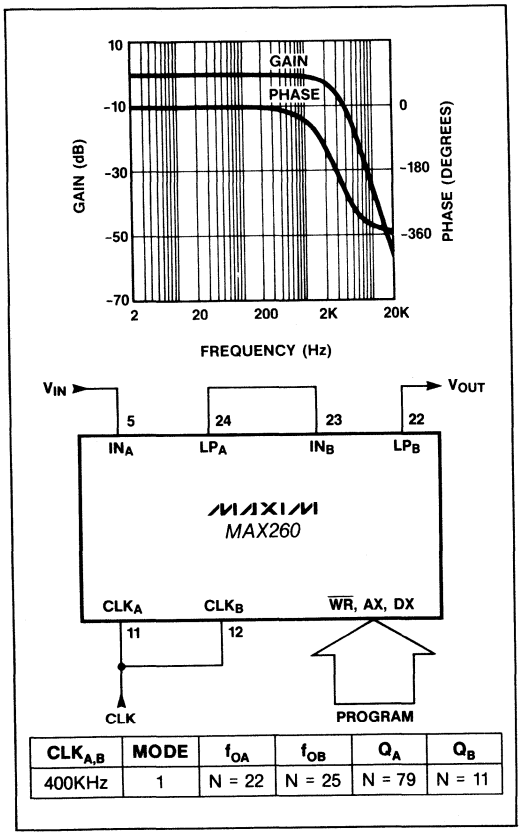
$CLK_{A,B}$	$MODE_A$	$MODE_B$	f_{0A}	f_{0B}	Q_A	Q_B
120kHz	1	2	N=56	N=5	N=96	N=83

Figure 24. Wide Passband Chebyshev Bandpass Filter



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
1 to 3MHz	1	N=38	N=0	N=96	N=96

Figure 25. High Frequency Chebyshev Bandpass Filter



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400KHz	1	N = 22	N = 25	N = 79	N = 11

Figure 26. Fourth-Order Butterworth Lowpass

From the above parameters, we use either lookup tables, design texts or Maxim's filter design programs to generate the order (number of poles), and the f_0 and Q of each second-order section. The A and B parameters are:

f_{0A} = 639 Hz f_{0B} = 1564 Hz
Q_A = 2.01 Q_B = 2.01

To implement this filter, section A operates in Mode 1 and section B uses Mode 2 to provide a wider overall range of f_{CLK}/f_0 ratios. This way one clock frequency can drive both sections A and B. See selection Tables 2 and 3.

$CLK_A = CLK_B$ = 120 kHz
f_{CLK}/f_{0A} = 188.49 (Mode 1, N=56), actual f_{0A} = 636.6 Hz
f_{CLK}/f_{0B} = 76.64 (Mode 2, N=5), actual f_{0B} = 156.5 Hz
Q_A = 2.000 (Mode 1, N=96), Q_B = 2.01 (Mode 2, N=83)

The overall passband gain at f_0 will be 0.64V/V or -3.9dB.

High Frequency Chebyshev Bandpass

The same Chebyshev response shape shown in Figure 24 is implemented at higher frequencies with a MAX262 in Figure 25. The curves show plots for center frequencies of 15.6kHz, 31.3kHz, and 47kHz. Not only is this faster than the MAX260 implementation but Mode 1 can be used in both halves of the MAX262 for this filter because the range of available f_{CLK}/f_0 ratios is wider with the MAX262 than the MAX260.

Fourth-Order Butterworth Lowpass

Figure 26 shows a fourth-order Butterworth lowpass with a cutoff frequency of 3kHz. Section A and B of a MAX260 are cascaded. The f_0 and Q parameters for each section are:

f_{0A} = 3kHz f_{0B} = 3kHz
Q_A = 1.307 Q_B = 0.541

Mode 1 and a 400kHz clock are used. Because of low Q values, the sampling errors of Figure 20 begin to look significant in this case. From the graphs, using f_{CLK}/f_0 ratio near 133, f_0A will be about 4% high, f_0B will be 1.5% high. Q_A will be -1.2% low, and Q_B will be -0.5% low. If these errors are not a problem, the corrections can be ignored. They are included here for best possible accuracy:

$CLK_A = CLK_B$ = 400 kHz
f_{CLK}/f_{0A} = 135.08 (N=22), f_{0B} = 2961 Hz (-1.3% correction)
f_{CLK}/f_{0B} = 139.80 (N=25), f_{0A} = 2861 Hz (-4.6% correction)
Q_A = 1.306 (N=79, Q resolution prevents +0.5% correction)
Q_B = 0.547 (N=11, +1.1% correction)

Measured wideband noise for this filter is 123μV RMS. If Mode 2 were used, the noise would be 87μV RMS. For lower noise with either Mode the first section should have the highest Q (Section A in this example).

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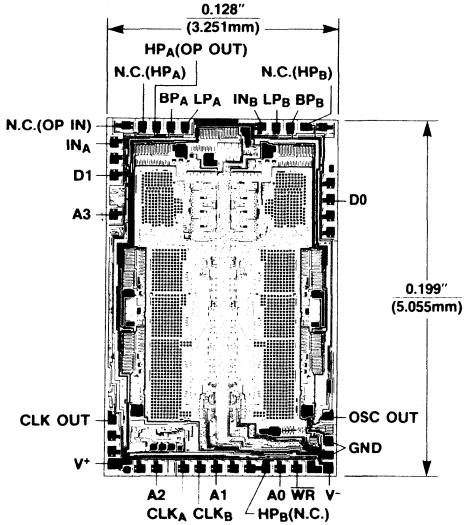
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX261BCNG	0°C to +70°C	Plastic DIP	2%
MAX261AENG	-40°C to +85°C	Plastic DIP	1%
MAX261BENG	-40°C to +85°C	Plastic DIP	2%
MAX261ACWG	0°C to +70°C	Wide SO	1%
MAX261BCWG	0°C to +70°C	Wide SO	2%
MAX261AMRG	-55°C to +125°C	CERDIP	1%
MAX261BMRG	-55°C to +125°C	CERDIP	2%
MAX262ACNG	0°C to +70°C	Plastic DIP	1%
MAX262BCNG	0°C to +70°C	Plastic DIP	2%
MAX262AENG	-40°C to +85°C	Plastic DIP	1%
MAX262BENG	-40°C to +85°C	Plastic DIP	2%
MAX262ACWG	0°C to +70°C	Wide SO	1%
MAX262BCWG	0°C to +70°C	Wide SO	2%
MAX262AMRG	-55°C to +125°C	CERDIP	1%
MAX262BMRG	-55°C to +125°C	CERDIP	2%

** All devices—24-pin 0.3" wide packages*

Chip Topography



NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX261/62 ONLY

MAXIM

Pin Programmable Universal and Bandpass Filters

General Description

The MAX263/264 and MAX267/268 CMOS switched-capacitor active filters are designed for precision filtering applications. Center frequency, Q, and operating mode are all selected via pin-strapped inputs. The MAX263/264 uses no external components for a variety of bandpass, lowpass, highpass, notch and allpass filters. The MAX267/268 is dedicated to bandpass applications and includes an uncommitted op-amp. Two second-order filter sections are included in both devices.

An input clock and a 5-bit programming input precisely set the filter center/corner frequency. Q is also programmed from 0.5 to 64. Separate clock inputs for each filter half operate with either an external clock or a crystal.

The MAX263 and 267 operate with center frequencies up to 57kHz while the MAX264 and 268 extend the f_0 range to 140kHz by employing lower f_{CLK}/f_0 ratios. The MAX263/264 is supplied in 28 pin wide DIP and small outline packages while the MAX267/268 is supplied in 24 pin narrow DIP and wide SO packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Matched Tracking Filters

Features

- ♦ **Filter Design Software Available**
- ♦ **32-Step Center Frequency Control**
- ♦ **128-Step Q Control**
- ♦ **Independent Q and f_0 Programming**
- ♦ **Guaranteed Clock to f_0 Ratio—1% (A grade)**
- ♦ **75kHz f_0 Range (MAX264/268)**
- ♦ **Single +5V and ±5V Operation**

Ordering Information

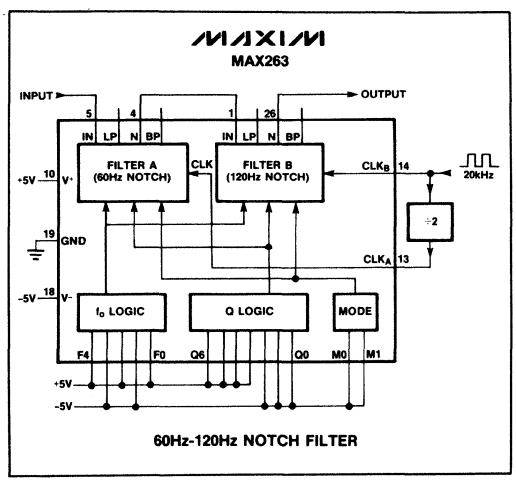
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX263ACPI	0°C to +70°C	Plastic DIP	1%
MAX263BCPI	0°C to +70°C	Plastic DIP	2%
MAX263AEPI	-40°C to +85°C	Plastic DIP	1%
MAX263BEPI	-40°C to +85°C	Plastic DIP	2%
MAX263ACWI	0°C to +70°C	Wide SO	1%
MAX263BCWI	0°C to +70°C	Wide SO	2%
MAX263AMJI	-55°C to +125°C	CERDIP	1%
MAX263BMJI	-55°C to +125°C	CERDIP	2%
MAX264ACPI	0°C to +70°C	Plastic DIP	1%
MAX264BCPI	0°C to +70°C	Plastic DIP	2%

(Ordering Information continued on last page.)

* *MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*

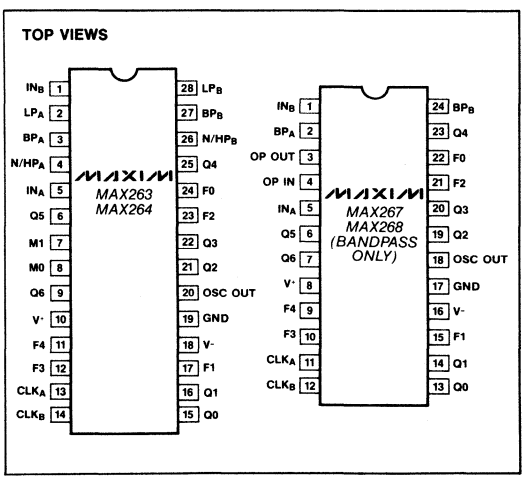
MAX267/268 packages are 24-pin 0.3" wide DIP and 24-pin 0.3" wide SO (Small Outline).

Typical Application



60Hz-120Hz NOTCH FILTER

Pin Configuration



Pin Programmable Universal and Bandpass Filters

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^--0.3V to V^++0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX26XXCXX ..... 0°C to +70°C
  MAX26XXEXX ..... -40°C to +85°C
  MAX26XXMXX ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and $\overline{Q}$ inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	$T_A = T_{MIN}$ to T_{MAX}	MAX26XA MAX26XB		±0.2 ±0.2	±1.0 ±2.0	%
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	$T_A = T_{MIN}$ to T_{MAX} Q = 0.5 to 16 Q = 0.5 to 16 Q = 32 Q = 32 Q = 64 Q = 64	 MAX26XA MAX26XB MAX26XA MAX26XB MAX26XA MAX26XB		 ±1 ±1 ±2 ±2 ±4 ±4	 ±6 ±10 ±10 ±15 ±15 ±22	%
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX263/4A MAX263/4B		±0.1 ±0.1	±0.25 ±0.5	dB
Gain Temperature Coefficient	Lowpass (at D.C.) Bandpass (at f_0)			-5 +20		ppm/°C
Output Offset Voltage (Note 3)	$T_A = T_{MIN}$ to T_{MAX}, Q = 4 Mode 1 BP Output	MAX263/67A MAX263/67B MAX264/68A MAX264/68B		±0.05 ±0.05 ±0.05 ±0.05	±0.20 ±0.30 ±0.20 ±0.30	V
	Mode 1 LP,N Outputs	MAX263A MAX263B MAX264A MAX264B		±0.40 ±0.80 ±0.40 ±0.80	±0.90 ±1.60 ±0.90 ±1.60	
	Mode 3 BP, HP Outputs	MAX263A MAX263B MAX264A MAX264B		±0.10 ±0.10 ±0.10 ±0.10	±0.20 ±0.30 ±0.20 ±0.30	
	Mode 3 LP Output	MAX263A MAX263B MAX264A MAX264B		±0.50 ±0.90 ±0.50 ±0.90	±1.00 ±1.60 ±1.00 ±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 $T_A = T_{MIN}$ to T_{MAX}			±0.75		mV/°C
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP 4th-Order LP 4th-Order BP			See Typ. Oper. Char. 90 100		μV_{RMS}

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and Q inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Harmonic Distortion at f_0	Q = 4, V_{IN} = $1.5V_{PP}$			-57		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX}	MAX263/67 MAX264/68		14 14	20 20	mA
Shutdown Supply Current (Note 5)	Q0-Q6 = all 0			2.5		mA
f_0, Q Programming Inputs	T_A = T_{MIN} to T_{MAX}, F0-F4, Q0-Q6 High Threshold Low Threshold		V^+-0.5		 V^-+0.5	V
Clock Inputs	T_A = T_{MIN} to T_{MAX}, CLK_A, CLK_B High Threshold Low Threshold		2.4		 0.8	V
Input Leakage Current	T_A = T_{MIN} to T_{MAX} CLK_B = V^+ or V^- CLK_A = V^+ or V^- M0, M1, F0-F4, Q0-Q6 = V^+-0.5V or V^-+0.5V M0, M1, F0-F4, Q0-Q6 = V^+ or V^-			 6 20 5	10 60 200 	µA
INTERNAL AMPLIFIERS						
Output Signal Swing	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source Sink			50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/µs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

(V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 1MHz f_{CLK}/f_0 = 197.92 for the MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, T_A = +25°C unless otherwise noted.)

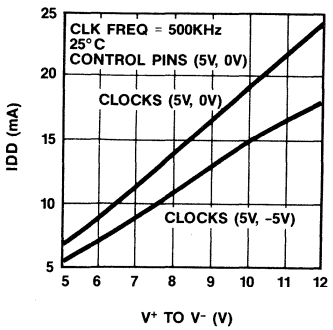
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 6)		
Maximum Clock Frequency				(Note 6)		
f_{CLK}/f_0 Ratio Error (Notes 1, 7)	Q = 8	MAX26XA MAX26XB		±0.1 ±0.1	±1 ±2	%
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 7)	Q = 8 f_{CLK}/f_0 = 197.92 f_{CLK}/f_0 = 138.23	 MAX263/67A MAX263/67B MAX264/68A MAX264/68B		 ±2 ±2 ±2 ±2	 ±5 ±10 ±5 ±10	%
Output Signal Swing	All Outputs			±2		V
Power Supply Current				7		mA
Shutdown Current				0.45		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 197.92 on the MAX263/67, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 138.23 on the MAX264/68.
Note 2: Q accuracy tested at Q = 0.5, 1, 2, 4, 8, 16, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.
Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 750kHz.
Note 4: Output noise is measured with an RC output smoothing filter at 4 × f_0 to remove clock feedthrough.
Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. Power supply current is typically 4mA higher with TTL clock input levels.
Note 6: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.
Note 7: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V however these parameters are only tested to the extent indicated by the MIN or MAX limits.

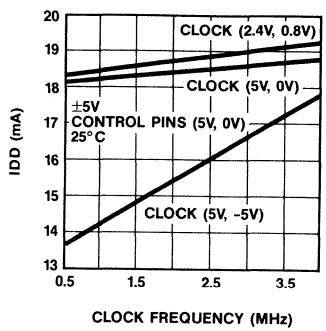
Pin Programmable Universal and Bandpass Filters

Typical Operating Characteristics

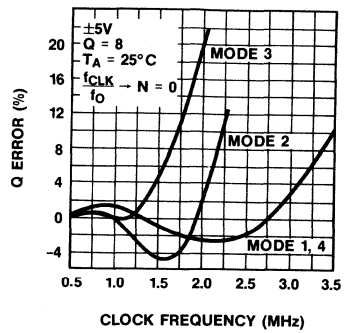
IDD vs POWER SUPPLY VOLTAGE



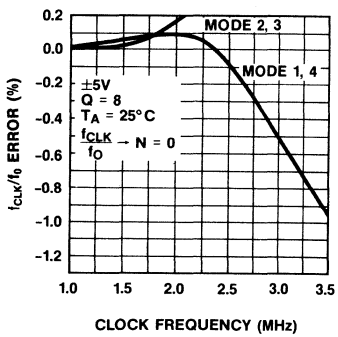
IDD vs CLOCK FREQUENCY



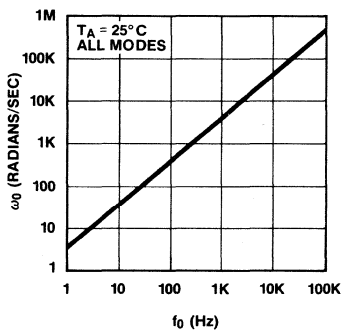
Q vs CLOCK FREQUENCY



f_{CLK}/f_0 vs CLOCK FREQUENCY



ω_0 vs f_0



Wideband RMS Noise (db ref. to 2.47V_{RMS}, 7V_{p-p}), ±5V Operation

Mode	Q = 1			Q = 8			Q = 64		
	LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
1	-84	-90	-84	-80	-82	-85	-72	-73	-85
2	-88	-90	-88	-84	-82	-84	-77	-73	-76
3	-84	-90	-88	-80	-82	-82	-73	-73	-74
4	-83	-89	-84	-79	-81	-85	-71	-73	-85

Notes:
1. f_{CLK} = 1MHz
2. f_{CLK}/f_0 ratio programmed at N = 31 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX263.

Noise Spectral Distribution
(MAX263/67, f_{CLK} = 1 MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3kHz	-87	-87	-86
C Message Weighted	-93	-93	-93

Pin Description

MAX263 MAX264 PIN #	MAX267 MAX268 PIN #	NAME	FUNCTION
10	8	V^+	Positive supply voltage
18	16	V^-	Negative supply voltage
19	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
13	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
14	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
20	18	OSC OUT	Connects to crystal for self clocked operation
5, 1	5, 1	IN_A, IN_B	Filter inputs
3, 27	2, 24	BP_A, BP_B	Bandpass outputs
2, 28		LP_A, LP_B	Lowpass outputs (MAX263/264 only)
4, 26		HP_A, HP_B	Highpass/Notch/Allpass outputs (MAX263/264 only)
8, 7		M0, M1	Mode select inputs (MAX267/268 are fixed in Mode 1)
24, 17, 23 12, 11	22, 15, 21 10, 9	F0-F4	Clock/center frequency ratio (f_{CLK}/f_0) programming inputs
15, 16, 21 22, 25, 6 9	13, 14, 19 20, 23, 6 7	Q0-Q6	Q programming inputs
	4	OP IN	Inverting input of uncommitted op-amp on MAX267/268 only. Noninverting input is internally connected to ground.
	3	OP OUT	Output of uncommitted op-amp on MAX267/268 only.

Pin Programmable Universal and Bandpass Filters

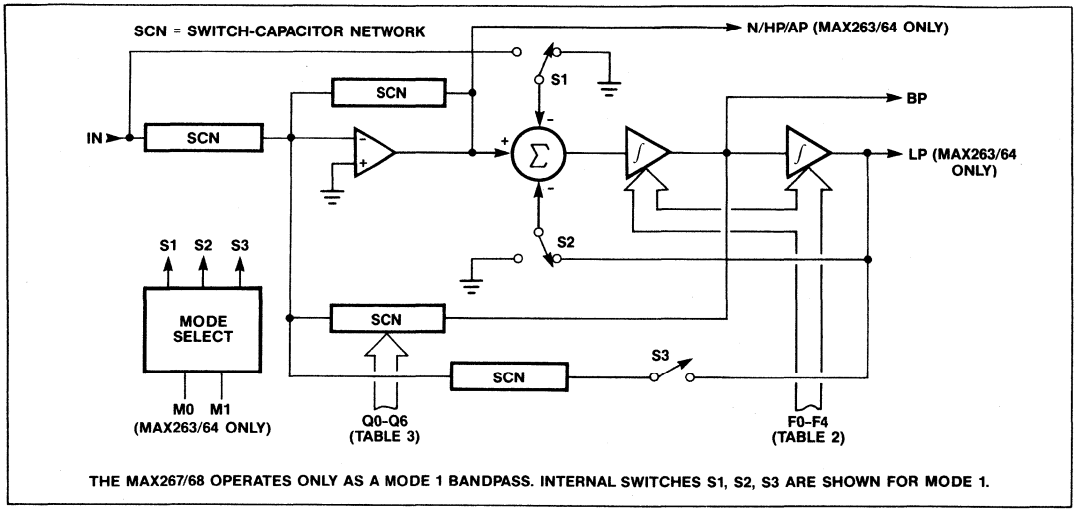


Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX26X device contains two second-order filters. In Figure 1, a block diagram of the state variable topology employed in one filter section shows how on-chip switched capacitor networks provide adjustable feedback to control f_0 and Q. Shared programming inputs require that both halves of the filter be set for the same f_{CLK}/f_0 ratio and Q. In the MAX263 and MAX264 universal filters, switches S1-S3 are controlled by inputs M0 and M1 to set the filter operating mode. The MAX267/68 bandpass filter operates only in Mode 1.

The MAX264/68 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX263/67 to allow higher signal bandwidths and a wider programming range. The reduced f_{CLK}/f_0 ratios result in somewhat more deviation from ideal continuous filter parameters than with the MAX263/67, however these differences can be compensated using Figure 17 (See "Applications Hints") or Maxim's filter design software.

The second-order sections in the MAX263/64/67/68 are identical and may be used as matched dual tracking filters, or can be cascaded to form higher-order filters. They can also be combined with external resistors and amplifiers for multiple feedback all-pole bandpass filters.

In all MAX26X series filters, the internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Quick Look Design Procedure

MAX26X series filters, with Maxim's filter design software, greatly simplify the design procedure for many active filters. Most designs can be realized using the steps in this section. If the filter software is not used, or if the complexity is beyond the scope of this section, refer to the remainder of this data sheet for more detailed application information.

Step 1—Filter Design

Starting with the design program "PZ", determine what type of filter is needed. PZ helps determine the type (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and calculates the pole/zero (f_0) and Q values for each second-order section. Each MAX26X contains two such sections and devices may be cascaded for higher order filters.

An alternate technique for bandpass filters uses multiple feedback (see Figure 13). If this is employed, the filter design program "BP" should be used instead of PZ and Step 2 is not used.

Step 2—Generate Programming Coefficients

If multiple feedback is not used, start with the f_0 and Q values obtained with PZ in Step 1 and use the program "MPP" to generate the digital program codes for f_{CLK}/f_0 and Q. MPP displays "N" values for f_0 and Q where N is the decimal equivalent of the binary pin-program codes. These are listed in Tables 2 and 3.

An input clock and filter "Mode" must also be selected in this step, however, if a specific clock rate is not selected, "MPP" will pick one. With regard to mode selection, Mode 1 (only possible mode for MAX267/68) is the most convenient choice for most bandpass and lowpass filters except for elliptics which require Mode 3. Highpass filters also use Mode 3, while allpass filters require Mode 4. For details regarding mode selection see "Filter Operating Modes". When a clock frequency (or frequencies) is selected and the programming codes for f_{CLK}/f_0 and Q are determined, the filter can then be programmed and operated.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ will calculate the pole frequencies, Q's, zeros, and the number of stages needed.

Program MPP. For programmed filters, MPP computes the input codes to use and describes the expected performance of the design.

Program BP. In the special case of bandpass filters, an alternate mode of operation is the "Multiple Feedback Technique". BP calculates the resistor values and the bandpass frequency response for this mode. An advantage of multiple feedback is that identical programming and one clock frequency can be used for all stages.

Program FR. When a design of one or more stages is completed, FR checks the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Detailed Description

f_0 and Q Programming

Figure 2 shows a block diagram of a complete filter. Each 2nd-order filter section has its own clock input, however, package pin limitations require that f_0, Q, and Mode control be shared by both sections. The actual center frequency is a function of the filter's clock rate, 5-bit f_0 control word (see Table 2), and operating Mode.

For some filter designs, the MAX263/64/67/68 may require separate clocks for each second-order section since separate programming inputs are not provided. Such designs may be implemented with different clock inputs, or, in the case of bandpass filters, by using multiple feedback and one clock (see "Description of Filter Functions"). When implementing two or more matched filters, however, the programming restrictions are easily overcome and one clock can still be used as demonstrated by the design example in Figure 21. Another alternative is to use the MAX260/261/262 microprocessor programmed filters or the MAX265/266 resistor programmed filters which allow independent programming of each filter section. Refer to the device data sheets for further details on those products.

Pin Programmable Universal and Bandpass Filters

Table 1. Typical Clock and Center Frequency Limits (MAX267/268 are operated in Mode 1 only.)

PART	Q	MODE	f_{CLK}	f_0
MAX263/ 267	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz
	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz

PART	Q	MODE	f_{CLK}	f_0
MAX264/ 268	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

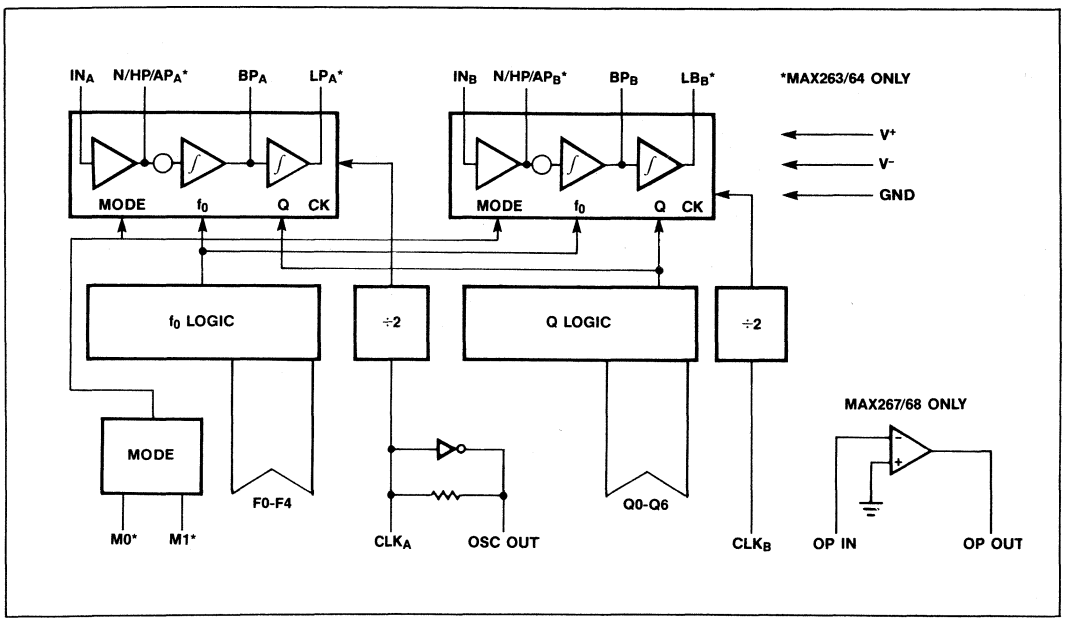


Figure 2. MAX263/264/267/268 Block Diagram

Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE					
MAX263/67		MAX264/68							
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0
103.67	73.31	43.98	31.10	1	0	0	0	0	1
106.81	75.53	47.12	33.32	2	0	0	0	1	0
109.96	77.75	50.27	35.54	3	0	0	0	1	1
113.10	79.97	53.41	37.76	4	0	0	1	0	0
116.24	82.19	56.55	39.99	5	0	0	1	0	1
119.38	84.42	59.69	42.21	6	0	0	1	1	0
122.52	86.64	62.83	44.43	7	0	0	1	1	1
125.66	88.86	65.97	46.65	8	0	1	0	0	0
128.81	91.80	69.12	48.87	9	0	1	0	0	1
131.95	93.30	72.26	51.10	10	0	1	0	1	0
135.08	95.52	75.40	53.31	11	0	1	0	1	1
138.23	97.74	78.53	55.54	12	0	1	1	0	0
141.37	99.97	81.68	57.76	13	0	1	1	0	1
144.51	102.89	84.82	59.98	14	0	1	1	1	0
147.65	104.41	87.96	62.20	15	0	1	1	1	1
150.80	106.63	91.11	64.42	16	1	0	0	0	0
153.98	108.85	94.25	66.64	17	1	0	0	0	1
157.08	111.07	97.39	68.86	18	1	0	0	1	0
160.22	113.29	100.53	71.09	19	1	0	0	1	1
163.36	115.52	102.67	73.31	20	1	0	1	0	0
166.50	117.74	106.81	75.53	21	1	0	1	0	1
169.65	119.96	109.96	77.75	22	1	0	1	1	0
172.79	122.18	113.10	79.97	23	1	0	1	1	1
175.93	124.40	116.24	82.19	24	1	1	0	0	0
179.07	126.62	119.38	84.81	25	1	1	0	0	1
182.21	128.84	122.52	86.64	26	1	1	0	1	0
185.35	131.07	125.66	88.86	27	1	1	0	1	1
188.49	133.29	128.81	91.08	28	1	1	1	0	0
191.64	135.51	131.95	93.30	29	1	1	1	0	1
194.78	137.73	135.09	95.52	30	1	1	1	1	0
197.92	139.95	138.23	97.74	31	1	1	1	1	1

Notes: 1) For the MAX263/67, $f_{CLK}/f_0 = \pi(N+32)$ in Mode 1, 3, and 4, where N varies form 0 to 31.
2) For the MAX264/68, $f_{CLK}/f_0 = \pi(N+13)$ in Mode 1, 3, and 4, where N varies 0 to 31.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$.

Pin Programmable Universal and Bandpass Filters

Table 3. Q Program Selection Table (Continued on following page)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Note 4	Note 4	0	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1

Notes: 4) Writing all 0s into Q0-Q6 activates a low power shutdown mode. BOTH filter sections are deactivated.

Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)
6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

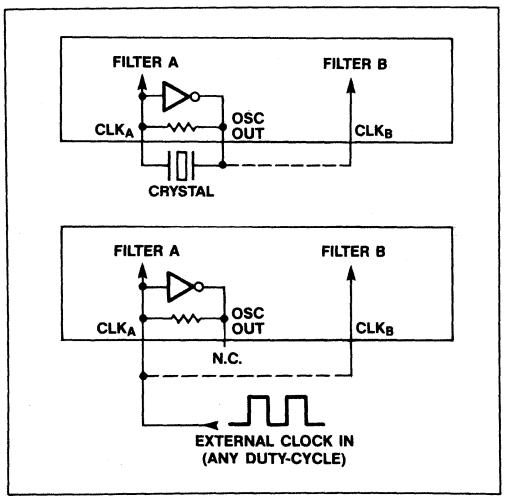


Figure 3. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX263/64/67/68 can operate with a crystal or an external clock generator as shown in Figure 3. The duty cycle of the clock at CLK_A and CLK_B is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Shutdown Mode

The filter enters a shutdown mode when all Q inputs, Q0-Q6, are tied low. When shut down, power consumption with ±5V supplies typically drops to 25mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes (MAX263/264 Only)

The MAX263/264's filter sections can be configured in four basic "Modes" as selected by inputs M0 and M1 (see Table 4). The MAX267/68 operates only in Mode 1. A fifth mode, 3A, uses an external op amp and resistors but is selected the same way and uses the same internal configuration as Mode 3.

Figures 4 through 8 show symbolic representations of the MAX263/64 filter modes. Only one second-order section is shown in each case, however the f_0, Q, and Mode select inputs are common to both halves of the IC. The f_0, f_N (notch), Q, and various output gains for each mode are shown in Table 4.

Filter Mode Selection

All operating modes listed in this section can be used with the MAX263/64. The MAX267/28 bandpass filter operates only in Mode 1.

MODE 1 (Figure 4) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc.. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

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Table 4. Filter Modes for Second-Order Functions—MAX263/264 (MAX267/268 = MODE 1, BP only)

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \rightarrow 0$)	H_{ON2} ($f \rightarrow f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes: f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

Mode 1, along with Mode 4, supports the highest clock frequencies (see Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 4). The gain of the lowpass and notch outputs is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op amp. In multiple feedback filters, the gain is set by the feedback resistors.

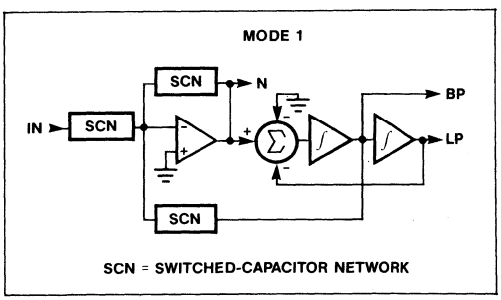

Figure 4. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

MODE 2 (Figure 5) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (see Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (see Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together.

MODE 3 (Figure 6) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with Mode 1 (see Table 1).

MODE 3A (Figure 7) uses a separate op amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

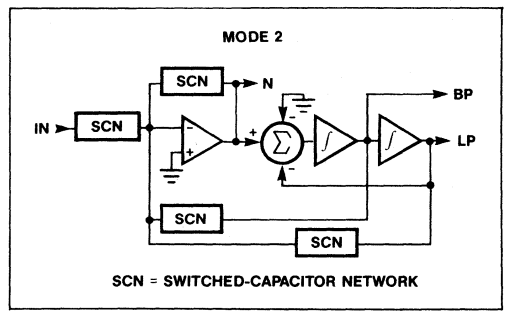

Figure 5. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

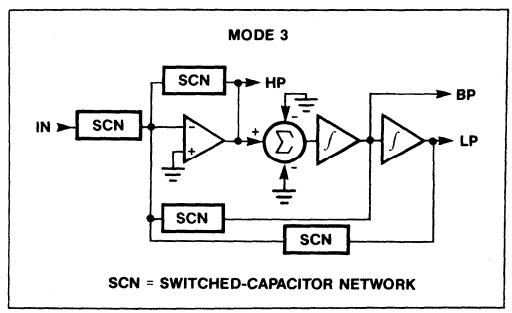

Figure 6. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

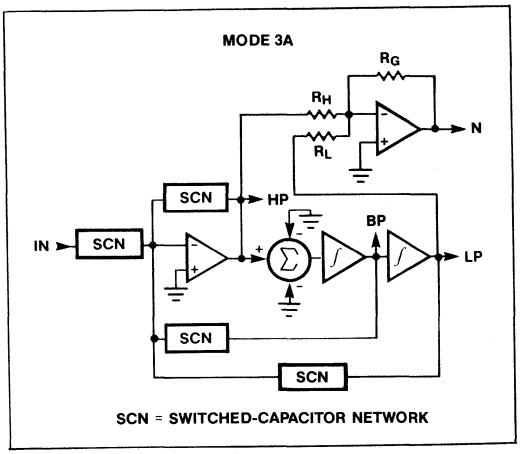

Figure 7. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used.

MODE 4 (Figure 8) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (see Figure 17).

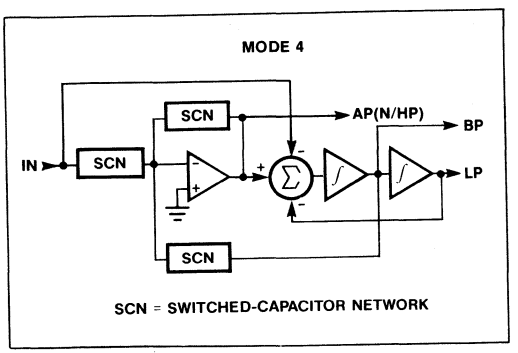

Figure 8. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

Description of Filter Functions

The MAX263/64 performs all filter functions listed in this section. The MAX267/68 operates only as a bandpass filter.

BANDPASS (Figure 9)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (see Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP}\frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_o$

f_0 = $\omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 10)

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 11)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

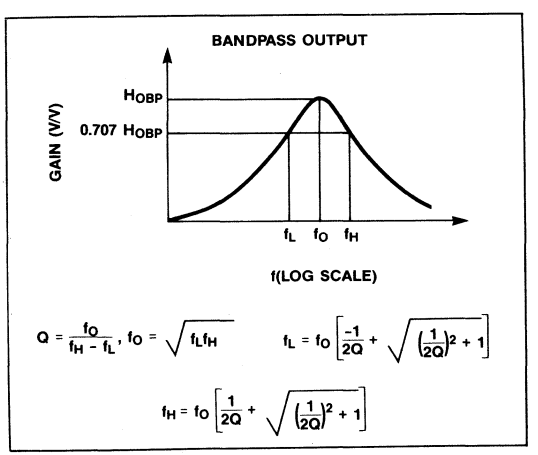

Figure 9. Second-Order Bandpass Characteristics

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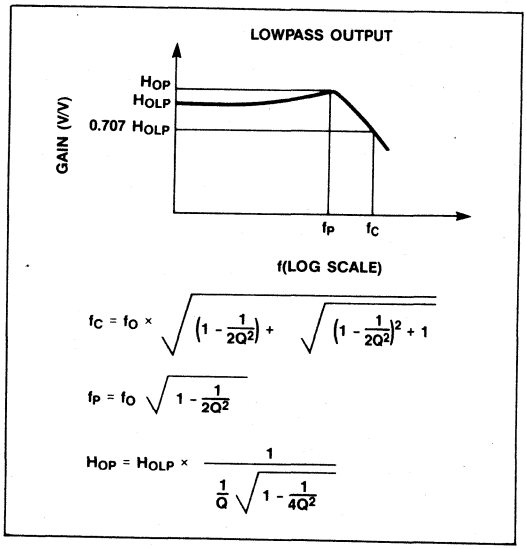


Figure 10. Second-Order Lowpass Characteristics

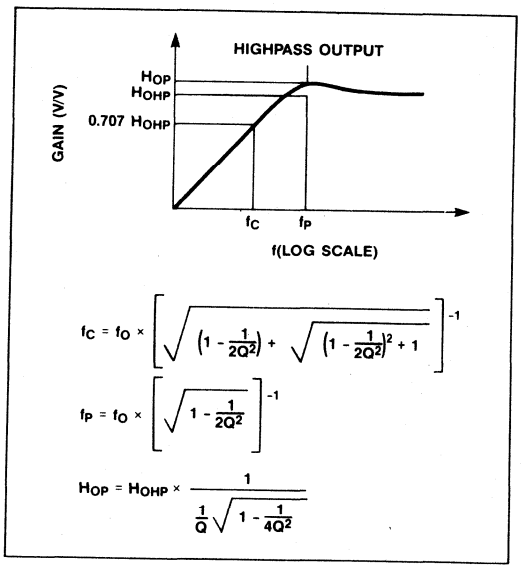


Figure 11. Second-Order Highpass Characteristics

NOTCH (Figure 12)

Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

$f_n = \omega_n/2\pi$

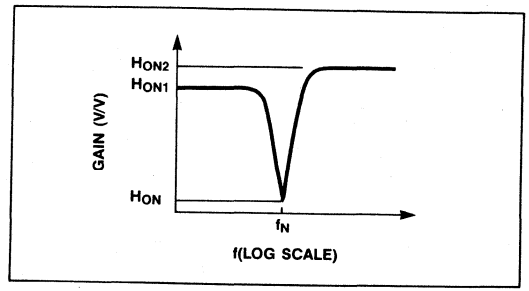


Figure 12. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for DC < f < $f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the filter. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 17 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Pin Programmable Universal and Bandpass Filters

Multiple Feedback Bandpass Filters

An alternate implementation of all-pole bandpass filters (i.e. Butterworth, Chebyshev) requires only one clock and common programming for all second-order sections. This can be useful with MAX26X pin-programmed filters since the two second-order halves must be programmed with the same f_{CLK}/f_0 ratio and Q (although they may use different clocks).

As shown in Figure 13, external resistors connect the outputs of cascaded filter sections to a summing op-amp at the input. Since each 2nd-order section inverts (gain = -Q) the output from odd numbered sections (except for the first) must be inverted before being fed back as in the 8th-order example in Figure 13. The MAX267/68 has an on-chip amplifier for this purpose but the MAX263/64 requires external op-amp(s).

In multiple feedback filters, the bandpass response is a function of the clock, f_{CLK}/f_0 ratio, Q, and feedback resistor ratios. In Table 5, constants for calculating resistor ratios in common bandpass configurations are listed. Maxim's filter design program "BP" also selects resistors for multiple feedback bandpass designs. A 4th-order design example (Figure 13) best illustrates how Table 5 is used.

Multiple Feedback Example

Requirements: 4th-order Chebyshev with 1 dB passband ripple, f_0 = 10kHz, and bandwidth (BW) = 2kHz.

1) The overall filter Q is $Q_F = f_0/BW = 10kHz/2kHz = 5$
2) From Table 5: $K_Q = 1.8219$
3) The Q of each 2nd-order selection is $Q_R = Q_F \times K_Q = 5 \times 1.8219 = 9.09$
4) R_F is selected, 10kΩ is a convenient value.
5) $R_2 = K_2 R_F (Q_R/2)^2 = 1.5039 \times 10k \times (9.109/2)^2 = 312k$
   In higher order filters, the general equation is: $R_N = K_N R_F (Q_R/2)^N$
6) R_0 sets the overall gain, A: $R_0 = K_0 R_F (Q_R/2)^2/A$, so for a gain of 1: $R_0 = 1.0930 \times 10k \times (9.109/2)^2/1 = 226.8k$. In higher order filters the general equation is $R_0 = K_0 R_F (Q_R/2)^M$ where M = (order of filter)/2.
7) The filter f_0 can be programmed using a wide range of clock frequencies and f_{CLK}/f_0 ratios. If f_{CLK} = 1MHz, then f_{CLK}/f_0 = 100 (code 00000 = 100.53) results in f_0 = 10kHz.
8) A 2.5pF to 10pF capacitor may be required across R_2 to prevent response peaking.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded without multiple feedback. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 5, the total Q and

Table 5. Multiple Feedback Bandpass Filter Constants

TYPE (RIPPLE)	ORDER	K0	K2	K3	K4	KQ
Butterworth	4	2.0000	4.0000			1.4142
(3.0 dB)	6	2.3704	2.6667	9.1429		1.5000
	8	2.9142	2.000	5.8284	14.315	1.5307
Chebyshev	4	1.6983	2.9512			0.8430
(0.1 dB)	6	1.3183	1.2137	4.5125		1.5473
	8	0.7986	0.5782	1.8809	2.0343	2.2176
Chebyshev	4	1.5757	2.5998			1.0378
(0.2 dB)	6	1.1128	0.9894	3.7271		1.8413
	8	0.5891	0.4551	1.4954	1.3309	2.6057
Chebyshev	4	1.3405	2.0161			1.4029
(0.5 dB)	6	0.8143	0.6897	2.6447		2.3944
	8	0.3389	0.3040	1.0114	0.6365	3.3406
Chebyshev	4	1.0930	1.5039			1.8219
(1.0 dB)	6	0.5822	0.4756	1.8475		3.0354
	8	0.1869	0.2038	0.6840	0.3002	4.1981
Chebyshev	4	0.9192	1.1934			2.1688
(1.5 dB)	6	0.4515	0.3616	1.4145		3.5705
Chebyshev	4	0.7850	0.9767			2.4881
(2.0 dB)	6	0.3641	0.2878	1.1308		4.0660
Chebyshev	4	0.6769	0.8148			2.7962
(2.5 dB)	6	0.3005	0.2353	0.9275		4.5462
Chebyshev	4	0.5875	0.6886			3.1013
(3.0 dB)	6	0.2519	0.1959	0.7739		5.0231

Pin Programmable Universal and Bandpass Filters

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

In high order bandpass filters that do not use multiple feedback, stages with different f_0s and Qs may also be cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0s, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$H_1(f_{0BP}) = H(f_{01})/G_1$ = Section 1's Gain at f_{0BP}

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{OBP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times$ etc.

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\,[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{Z1} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

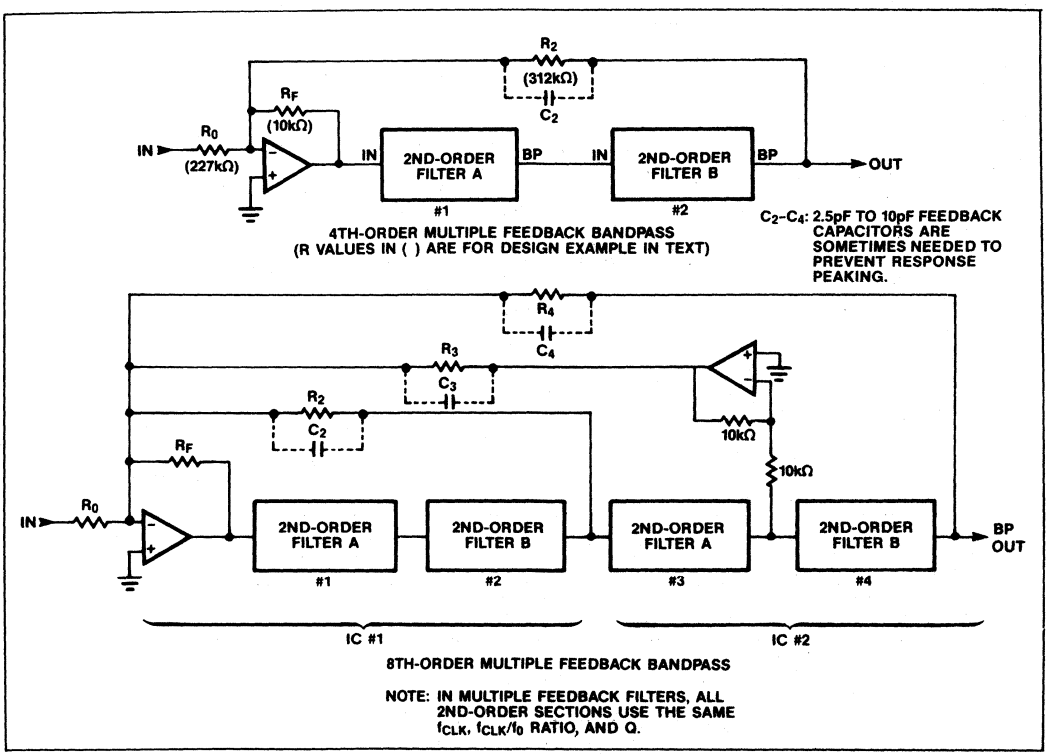


Figure 13. Multiple Feedback Bandpass Block Diagram (See Text for R Values)

Application Hints

Power Supplies

The MAX263/64/67/68 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±6V dual supplies. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or biased to $V^+/2$. Figure 14 shows circuit connections for single supply operation.

Power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum is preferred.) and 0.1µF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 14.

Output Swing and Clipping

MAX26X outputs are designed to swing to within 0.15V of each supply rail with a 10kΩ load.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example lets assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

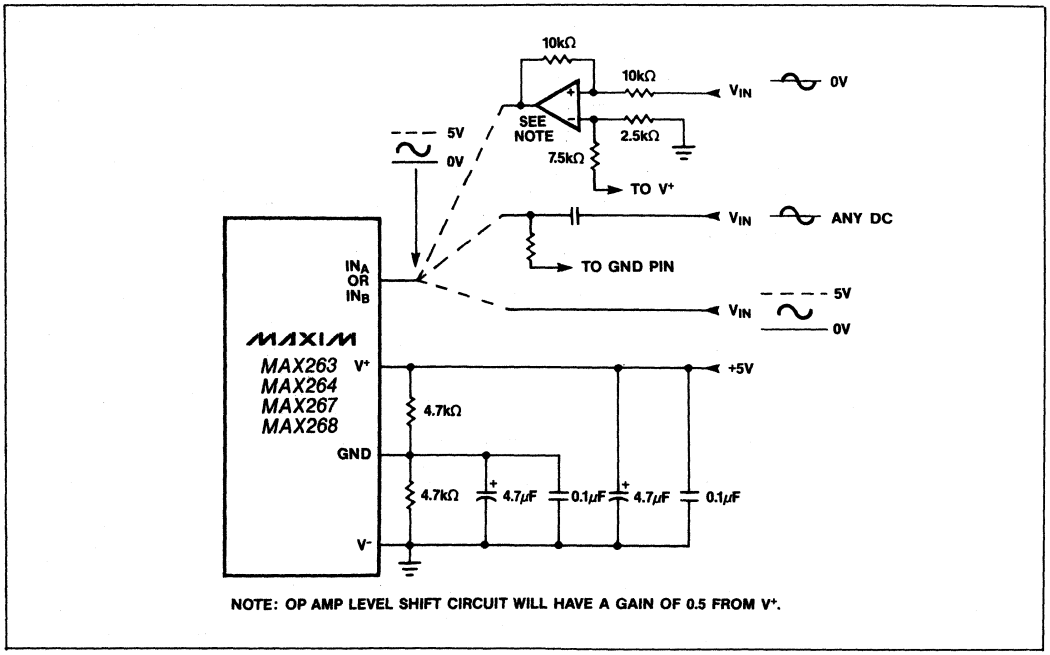


Figure 14. Power Supply and Input Connections for Single Supply Operation

Pin Programmable Universal and Bandpass Filters

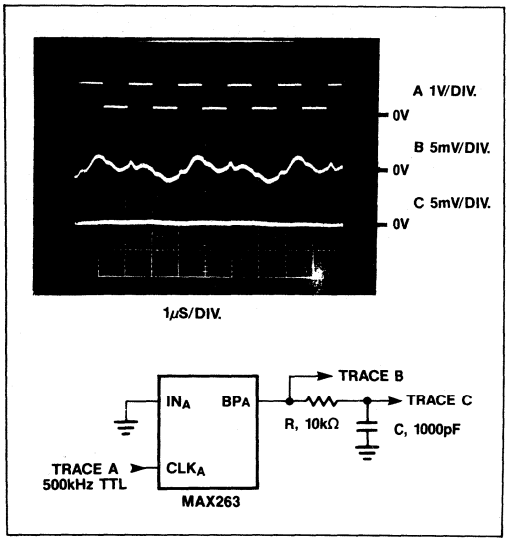


Figure 15. MAX263 Bandpass Output Clock Noise

Clock Feedthrough and Noise

Typical wideband noise for MAX26X series devices is $0.5mV_{pp}$ from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX26X series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This can also be attenuated with an RC smoothing filter as shown with the MAX263 in Figure 15.

Input Impedance

The filter input model is shown in Figure 16. Input capacitor C_A is shunted by C_B which is switched at one half the input clock frequency ($F_{CLK}/2$). The input impedance is described by: $R_{IN} = 2/(C_A \times f_{CLK})$. There is also a fixed stray capacitance of about 5pF to ground.

Digital Inputs

Filter programming is accomplished by tying input pins M0, M1, F0-F4, and Q0-Q6 to high or low voltage levels, typically V^+ and V^-. Inputs are not internally pulled up or down so these inputs must not be left unconnected. Input thresholds are guaranteed to be no higher than $V^+ -0.5V$ and no lower than $V^- +0.5V$. If pull-up resistors are used with switches at the programming inputs as might be the case in prototype

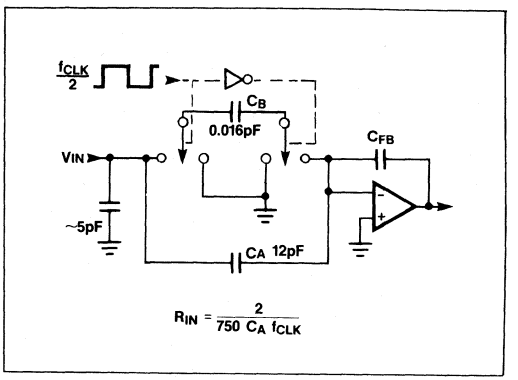


Figure 16. MAX263/64/67/68 Input Model

breadboards, the pull-up resistors should be no more than 3.3kΩ.

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 17 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX26X series devices and in fact occur with all sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX264/68 does employ a lower range of f_{CLK}/f_0 ratios than the MAX263/67 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 17 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 17 applies for Modes 1 and 3. When using Figure 17 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

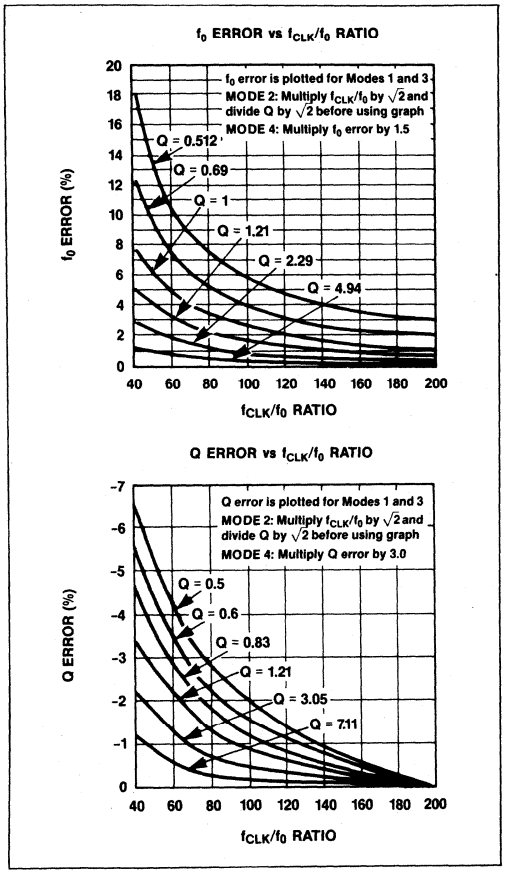


Figure 17. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX26X series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX264/68 uses lower f_{CLK}/f_0 ratios than the MAX263/67 and for this reason is more likely to require input filtering than the MAX263 or MAX267.

Trimming DC Offset

The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 18. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

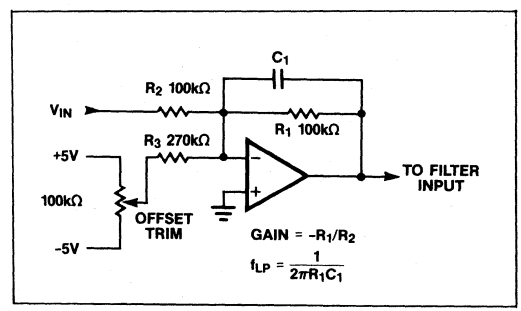


Figure 18. Circuit for DC Offset Adjustment

Design Examples

4th-Order Multiple Feedback Bandpass—MAX268

In Figure 19, a pin-programmed MAX268 operates as a 4th-order 50kHz Chebyshev bandpass. The specifications are:

Center frequency (f_0) = 50kHz
Pass bandwidth = 10kHz
Max. passband ripple = 0.1dB
Gain at center freq. = 1V/V

Two identical 2nd-order sections and the internal op amp are used with multiple feedback. The general form is as in Figure 13. Maxim's design program, BP, generates the programming codes and feedback resistor values. With a 2.5MHz crystal clock the realized parameters are:

Center frequency = 50.305kHz
Pass Bandwidth = 10.07kHz
Programmed f_{CLK}/f_0 ratio = 50.27 (N = 3)
Programmed Q = 4.27 (N = 113)
(desired Q = 4.215)
Actual Q (with error correction) = 4.21
Resistors: R_2 = 131kΩ, R_0 = 75kΩ, R_F = 10kΩ

Pin Programmable Universal and Bandpass Filters

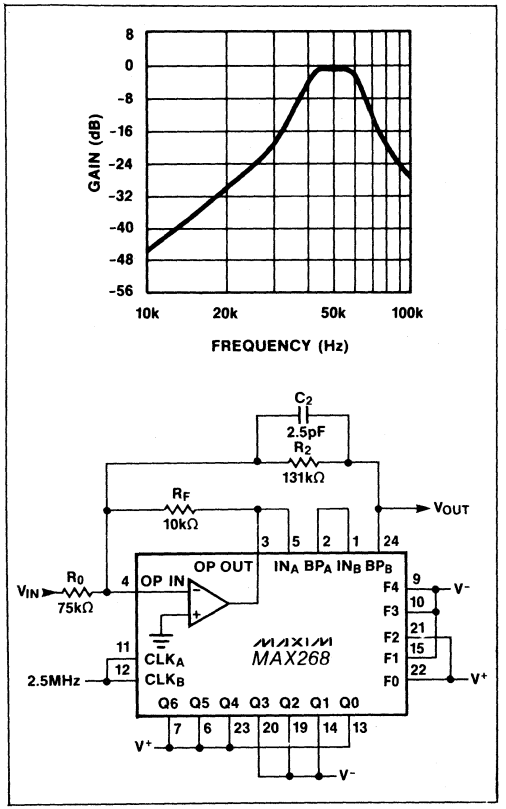


Figure 19. 4th-Order 50kHz Chebyshev Bandpass Using Multiple Feedback

Other clock rates and f_{CLK}/f_0 ratios can be chosen to implement the same filter, but larger f_{CLK}/f_0 ratios provide performance closer to the ideal. Capacitor C_2 may be needed to prevent response peaking at the passband edge. In this example C_2 = 2.5pF.

Multiple feedback can also be extended to 8th-order designs while still using one clock by adding a second MAX268 and 2 additional feedback resistors. These can also be calculated with the design program, BP. Note that for filter order above 4, the feedback signal from odd filter sections is inverted before it is summed (see Figure 13).

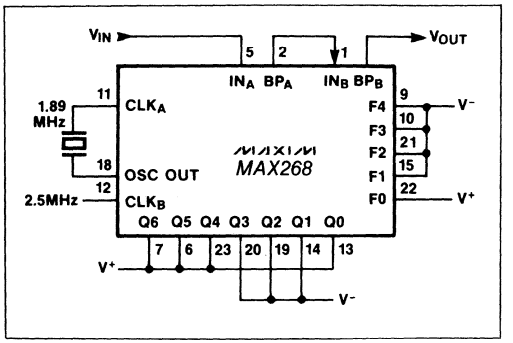


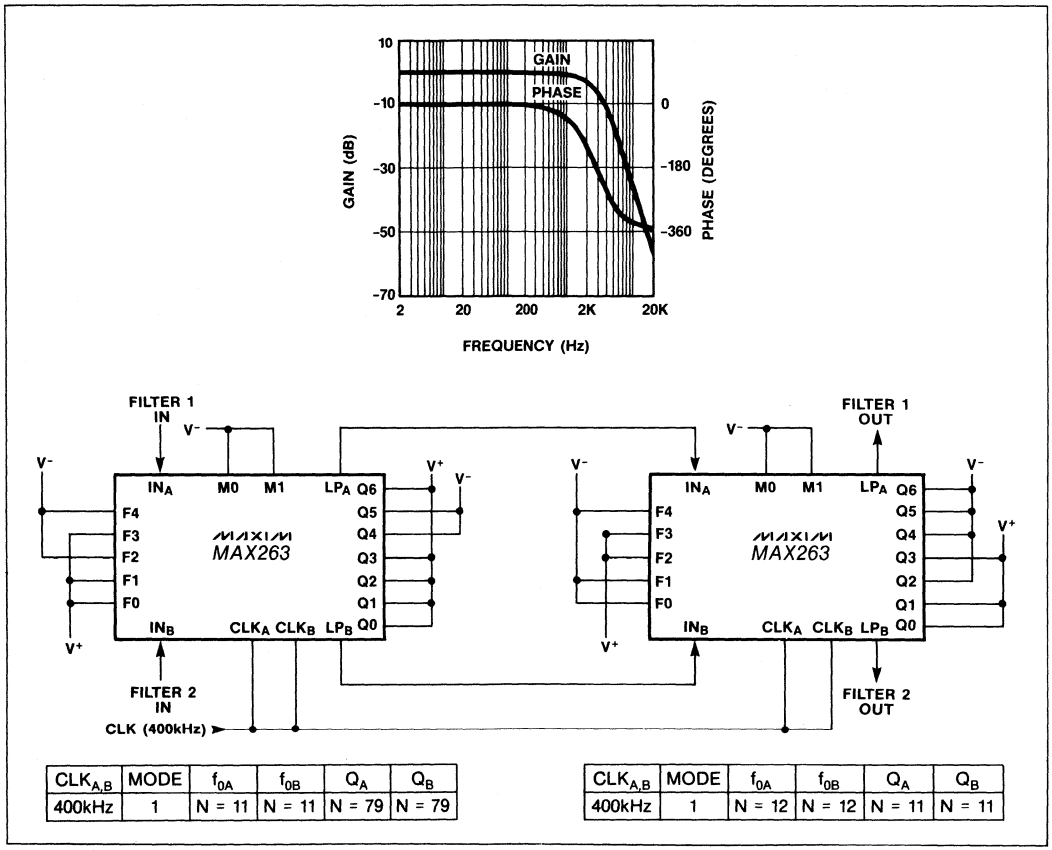
Figure 20. 4th-Order 50kHz Chebyshev Bandpass Using No External Resistors

4th-Order Bandpass (No Multiple Feedback)—MAX268

Without multiple feedback, the previous example can be implemented with no external components, however separate clocks are required for CLK_A and CLK_B (Figure 20). The target specifications are the same as before. The realized parameters are now:

CLK_A = 1.89MHz, CLK_B = 2.5MHz
Center frequency = 50kHz
Pass bandwidth = 10kHz
Programmed f_{CLK}/f_0 ratio = 43.98 (N = 1)
Programmed Q = 4.27 (N = 113) (desired Q = 4.215)
Actual Q (with error correction) = 4.2

With the chosen f_{CLK}/f_0 ratio, a crystal may be used at CLK_A while a divided system clock, if available (2.5, 5, 10, or 20MHz), drives CLK_B. This is suggested because CLK_A has internal circuitry to drive a crystal while CLK_B does not. Other clock sources may be used with a different programmed f_{CLK}/f_0 as long as the ratio between CLK_A and CLK_B remains the same as above. Another advantage of this circuit is that higher center frequencies can be achieved relative to equivalent multiple feedback designs because lower Q sections are used compared to multiple feedback.



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 11	N = 11	N = 79	N = 79

$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 12	N = 12	N = 11	N = 11

Figure 21. Dual Tracking 3kHz 4th-Order Lowpass

Dual 4th-Order Tracking Lowpass—MAX263

In Figure 21, two Butterworth lowpass filters are set up to accurately track each other. By "splitting" two MAX263s only one clock is needed. The specifications are:

Cutoff frequency = 3kHz
$f_{0A} = f_{0B}$ = 3kHz
Q_A = 1.307, Q_B = 0.541

These values can be programmed directly into the filter. However, since the Qs are low, sampling errors may be large enough to deserve attention. From Figure 17, if f_{CLK}/f_0 is near 130 (f_{CLK} is 400kHz), f_{0A} and f_{0B} will be about 4% and 1.5% high respectively. Q_A and Q_B will be 1.2% and 0.5% low. These errors may not be large enough to worry about but are corrected here (within the programming resolution of the MAX263) by the filter design programs PZ and MPP. f_{0A} and f_{0B} are programmed to different values (N_A = 11, N_B = 12) for this reason.

Mode 1, $CLK_A = CLK_B$ = 400kHz
f_{CLK}/f_{0A} = 135.08, N = 11
(target f_{0A} = 2961Hz, actual = 3008Hz)
f_{CLK}/f_{0B} = 138.23, N = 12
(target f_{0B} = 2894Hz, actual = 3015Hz)
Q_A = 1.31, N = 79 (actual Q_A = 1.30)
Q_B = 0.547, N = 11 (actual Q_A = 0.542)

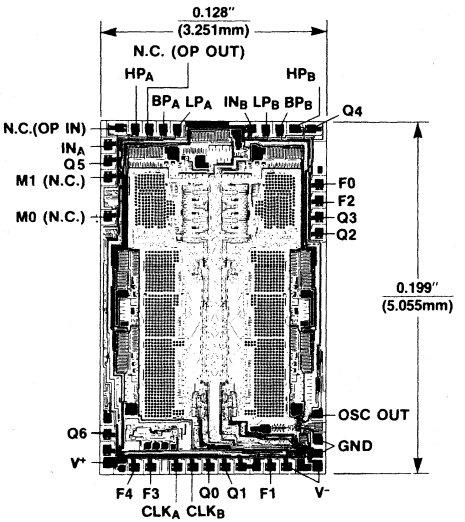
Pin Programmable Universal and Bandpass Filters

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX264AEPI	-40°C to +85°C	Plastic DIP	1%
MAX264BEPI	-40°C to +85°C	Plastic DIP	2%
MAX264ACWI	0°C to +70°C	Wide SO	1%
MAX264BCWI	0°C to +70°C	Wide SO	2%
MAX264AMJI	-55°C to +125°C	CERDIP	1%
MAX264MBJI	-55°C to +125°C	CERDIP	2%
MAX267ACNG	0°C to +70°C	Plastic DIP	1%
MAX267BCNG	0°C to +70°C	Plastic DIP	2%
MAX267AENG	-40°C to +85°C	Plastic DIP	1%
MAX267BENG	-40°C to +85°C	Plastic DIP	2%
MAX267ACWG	0°C to +70°C	Wide SO	1%
MAX267BCWG	0°C to +70°C	Wide SO	2%
MAX267AMRG	-55°C to +125°C	CERDIP	1%
MAX267BMRG	-55°C to +125°C	CERDIP	2%
MAX268ACNG	0°C to +70°C	Plastic DIP	1%
MAX268BCNG	0°C to +70°C	Plastic DIP	2%
MAX268AENG	-40°C to +85°C	Plastic DIP	1%
MAX268BENG	-40°C to +85°C	Plastic DIP	2%
MAX268ACWG	0°C to +70°C	Wide SO	1%
MAX268BCWG	0°C to +70°C	Wide SO	2%
MAX268AMRG	-55°C to +125°C	CERDIP	1%
MAX268BMRG	-55°C to +125°C	CERDIP	2%

** MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*
MAX267/268 packages are 24-pin 0.3" wide DIP and 24-pin 0.3" wide SO (Small Outline).

Chip Topography



NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX 267/268 ONLY

ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

Resistor/Pin Programmed Universal Active Filters

General Description

The MAX265 and MAX266 switched-capacitor active filters are designed for precision filtering applications. Each contains two independent, second-order building blocks which can be configured as a lowpass, highpass, bandpass, notch or allpass filter by adding a few external resistors. Any of the classical filter configurations (Butterworth, Chebyshev, elliptic, etc.) can be built. Two uncommitted op amps are included on chip.

Separate clock input pins are provided for both second-order filter blocks. The clock source can be either a crystal or external clock input. The center or cutoff frequency (f_{CLK}/f_0 ratio) is set by a 6-bit pin-strapped programming input and with resistors.

The MAX265 operates with center frequencies up to 40kHz and while the MAX266 operates with f_0s to 140kHz by employing a lower range of f_{CLK}/f_0 ratios. The filters operate with supplies ranging from ±2.37V to ±6.3V as well as a single +5V power. The MAX265/266 is supplied in 28-pin wide DIP and small outline packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

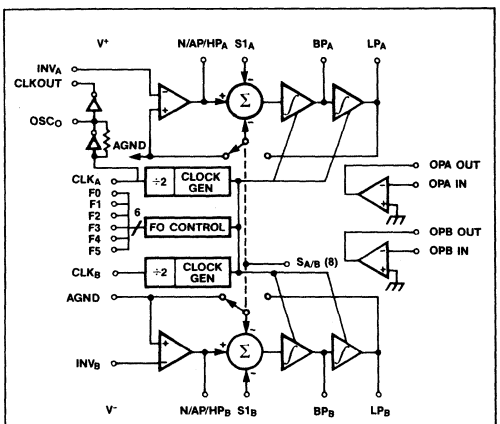
Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Telecommunications Test Equipment

Block Diagram



MAX265/266

Features

- ◆ Filter Design Software
- ◆ 64-Step Frequency Control
- ◆ Resistor Adjustment of Frequency
- ◆ 140kHz Center Frequency Range (MAX266)
- ◆ Single +5V and ±5V Operation

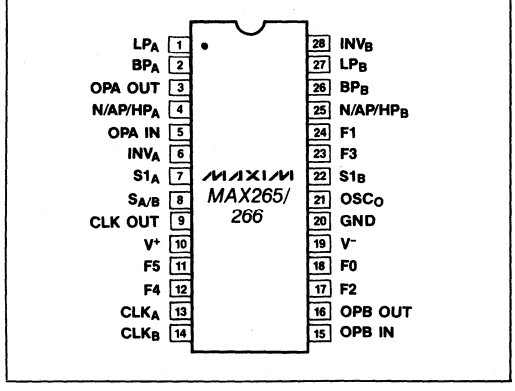
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX265ACPI	0°C to +70°C	Plastic DIP	1%
MAX265BCPI	0°C to +70°C	Plastic DIP	2%
MAX265AEPI	-40°C to +85°C	Plastic DIP	1%
MAX265BEPI	-40°C to +85°C	Plastic DIP	2%
MAX265ACWI	0°C to +70°C	Wide SO	1%
MAX265BCWI	0°C to +70°C	Wide SO	2%
MAX265AMJI	-55°C to +125°C	CERDIP	1%
MAX265BMJI	-55°C to +125°C	CERDIP	2%
MAX266ACPI	0°C to +70°C	Plastic DIP	1%
MAX266BCPI	0°C to +70°C	Plastic DIP	2%
MAX266AEPI	-40°C to +85°C	Plastic DIP	1%
MAX266BEPI	-40°C to +85°C	Plastic DIP	2%
MAX266ACWI	0°C to +70°C	Wide SO	1%
MAX266BCWI	0°C to +70°C	Wide SO	2%
MAX266AMJI	-55°C to +125°C	CERDIP	1%
MAX266BMJI	-55°C to +125°C	CERDIP	2%

** MAX265/266 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" Wide SO (Small Outline).*

6

Pin Configuration



19-3701; Rev 0; 5/91

MAXIM

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

General Description

The MAX270/MAX271 are digitally-programmed, dual second-order continuous-time lowpass filters. Their typical dynamic range of 96dB surpasses most switched capacitor filters which require additional filtering to remove clock noise. The MAX270/MAX271 are ideal for anti-aliasing and DAC smoothing applications and can be cascaded for higher-order responses.

The two filter sections are independently programmable by either microprocessor (µP) control or pin strapping. Cutoff frequencies in the 1kHz to 25kHz range can be selected.

The MAX270 has an on-board, uncommitted op amp, while the MAX271 has an internal track-and-hold (T/H).

Applications

Lowpass Filtering

Anti-Aliasing Filter

Output Smoothing

Low-Noise Applications

Anti-Aliasing and Track-and-Hold (MAX271)

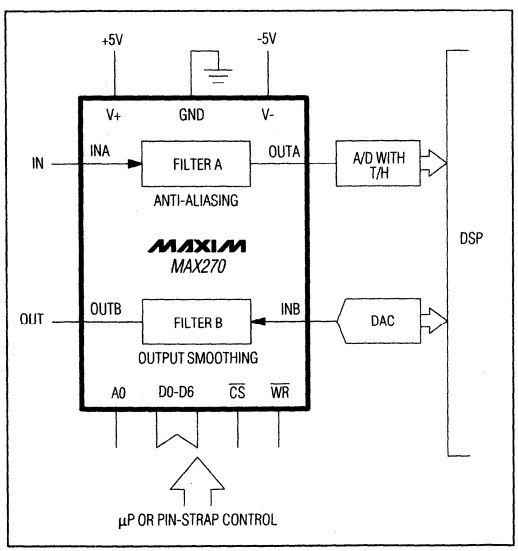
Features

- ♦ **Continuous-Time Filtering - No Clock Required**
- ♦ **Dual 2nd-Order Lowpass Filters**
- ♦ **Sections Independently Programmable: 1kHz to 25kHz**
- ♦ **96dB Dynamic Range**
- ♦ **No External Components**
- ♦ **Cascadable for Higher Order**
- ♦ **Low-Power Shutdown Mode**
- ♦ **Track-and-Hold (MAX271)**

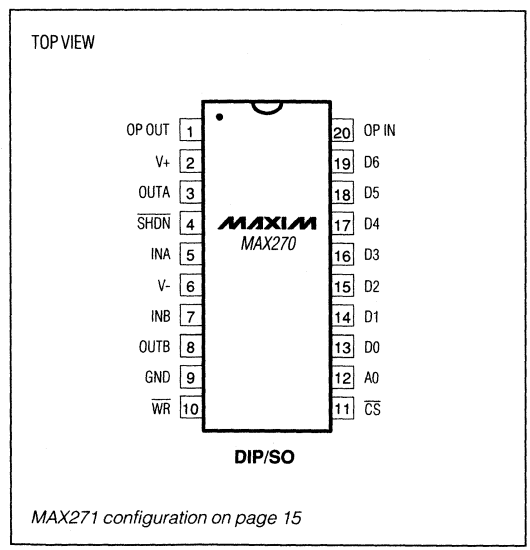
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX270CPP	0°C to +70°C	20 Plastic DIP
MAX270CWP	0°C to +70°C	20 Wide SO
MAX270EPP	-40°C to +85°C	20 Plastic DIP
MAX270EWP	-40°C to +85°C	20 Wide SO
MAX270MJP	-55°C to +125°C	20 CERDIP
MAX271CNG	0°C to +70°C	24 Plastic DIP
MAX271CWG	0°C to +70°C	24 Wide SO
MAX271ENG	-40°C to +85°C	24 Plastic DIP
MAX271EWG	-40°C to +85°C	24 Wide SO
MAX271MRG	-55°C to +125°C	24 CERDIP

Typical Operating Circuit



Pin Configurations



MAX271 configuration on page 15

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... -0.3V, +17V
V+ to GND ..... -0.3V, +8.5V
V- to GND ..... +0.3V, -8.5V
Input Voltage to GND, Any Input Pin ..... V- -0.3V, V+ +0.3V
Duration of Output Short Circuit to GND ..... Indefinite
Continuous Total Power Dissipation (T_A = +70°C)
MAX270:
Plastic DIP (derate 8mW/°C above +70°C) 640mW
Wide SO (derate 10mW/°C above +70°C) 800mW
CERDIP (derate 11.1mW/°C above +70°C) 889mW
MAX271:
Plastic DIP (derate 8.7mW/°C above +70°C) 696mW
Wide SO (derate 11.7mW/°C above +70°C) 941mW
CERDIP (derate 12.5mW/°C above +70°C) 1000mW
Operating Temperature Ranges:
MAX27_C_ _ ..... 0°C to +70°C
MAX27_E_ _ ..... -40°C to +85°C
MAX27_M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Operating Frequency Range	(Note 1)			2		MHz
Programmed Cutoff Frequency (f_C) Range				1-25		kHz
Programmed Cutoff Frequency Error	f_C code = 53 (2.536kHz typ)			±2.9		%
	f_C code = 127 (25kHz typ)			±9.5		
Filter Gain	f_C code = 0 (1kHz typ), T_A = T_{MIN} to T_{MAX}	f_{IN} = 1kHz	-3.6		-2.4	dB
		f_{IN} = 8kHz			-33	
	f_C code = 127 (25kHz typ), T_A = T_{MIN} to T_{MAX}	f_{IN} = 25kHz	-6		-0.5	
		f_{IN} = 200kHz		-34		
Maximum Gain (Peaking)	f_C code = 0 (1kHz typ)				0.15	dB
	f_C code = 127 (25kHz typ)			0.15		
Wideband Noise	50Hz to 50kHz Bandwidth	f_C code = 0 (1kHz typ)		12		µVRMS
		f_C code = 127 (25kHz typ)		38		
DC CHARACTERISTICS						
DC Output Signal Swing OUTA, OUTB, OP OUT (MAX270) OUTA, OUTB, T/H OUT (MAX271)	R_{LOAD} = 5kΩ, T_A = T_{MIN} to T_{MAX}		-3		3	V
Offset Voltage at Outputs OUTA, OUTB, OP OUT (MAX270) OUTA, OUTB (MAX271)			-2		2	mV
DC Input Leakage Current INA, INB (MAX270) INA, INB (MAX271)	T_A = T_{MIN} to T_{MAX}		-1		1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC FILTER CHARACTERISTICS - MAX270					
Total Harmonic Distortion (THD)	f_C code = 44 (2.01kHz typ), V_{IN} = 3.5V_{p-p} at 390.625Hz (Notes 2, 3)			-70	dB
Signal/(Noise + Distortion) (SINAD)			73		
Spurious-Free Dynamic Range (SFDR)		70			
UNCOMMITTED AMPLIFIER - MAX270					
Slew Rate			1.2		V/µs
Bandwidth			2		MHz
TRACK-AND-HOLD - MAX271					
Hold Settling Time	To 0.1% (Note 4)		500		ns
Acquisition Time	To 0.1% (Note 5)		1.8		µs
Hold Step			1		mV
Droop Rate	T_A = T_{MIN} to T_{MAX}		30		µV/µs
Offset Voltage at T/H OUT	Includes filter offset	-6		6	mV
T/H OUT Disabled Output Leakage Current	T_A = T_{MIN} to T_{MAX}, $\overline{T}$/H = 0V (Track Mode)	-10		10	µA
Total Harmonic Distortion (THD)	f_C code = 44 (2.01kHz typ), V_{IN} = 3.5V_{p-p} at 390.625Hz, Sampling rate = 50kHz (Notes 2, 6, 7)			-70	dB
Spurious-Free Dynamic Range (SFDR)		70			
DIGITAL INPUTS					
Digital Input High Voltage	T_A = T_{MIN} to T_{MAX} (Note 8)	2.4			V
Digital Input Low Voltage				0.8	
Digital Input Current	T_A = T_{MIN} to T_{MAX}, Digital input held at ±5V, includes MODE (MAX271) (Note 8)	-1		1	µA
POWER REQUIREMENTS					
Supply Voltage Range			±2.375 to ±8		V
Supply Current	T_A = T_{MIN} to T_{MAX} (Note 9)			6.5	mA
Shutdown Supply Current	T_A = T_{MIN} to T_{MAX} (Note 10)			15	µA
Power-Supply Rejection Ratio (PSRR) at 1kHz	f_C code = 0 (1kHz typ), V+ = 5VDC + 100mVp-p at 1kHz		30		dB

Note 1: All internal amplifiers limited to 2MHz bandwidth.
Note 2: Only filter A tested for these parameters.
Note 3: Spurious-Free Dynamic Range is the ratio of the fundamental to the largest of any harmonic or noise spur in dB.
Note 4: Includes T/H propagation delays. With 5kΩ, parallel 100pF load.
Note 5: ±2V input step settling 0.1% with 5kΩ parallel 100pF load.
Note 6: $\overline{T}$/H pin toggled at sampling rate, 50% duty cycle.
Note 7: THD and SFDR specifications for T/H include contributions from filter.
Note 8: Digital pins include $\overline{SHDN}$, $\overline{WR}$, $\overline{CS}$, A0, D0-D6 (MAX270) and $\overline{SHDN}$, T/H A/$\overline{B}$, $\overline{WR}$, T/H EN, $\overline{CS}$, A0, A1, D0-D6, $\overline{T}$/H (MAX271).
Note 9: Input of uncommitted op amp floating with a 5kΩ feedback resistor from input to output.
Note 10: $\overline{WR}$, $\overline{CS}$, A0, D0-D6 held at +5V; $\overline{SHDN}$ = 0V (MAX270). $\overline{WR}$, $\overline{CS}$, A0, A1, D0-D6, $\overline{TH}$, T/H A/B, T/H, MODE held at +5V; $\overline{SHDN}$ = 0V (MAX271).

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

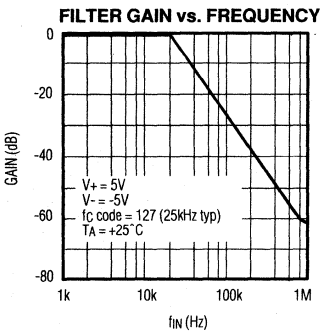
TIMING CHARACTERISTICS (Figure 2)

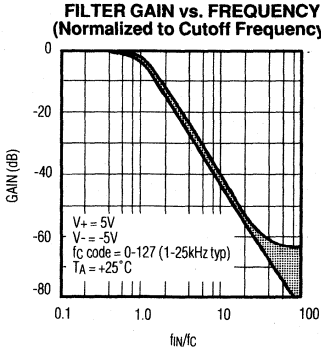
(V+ = 5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

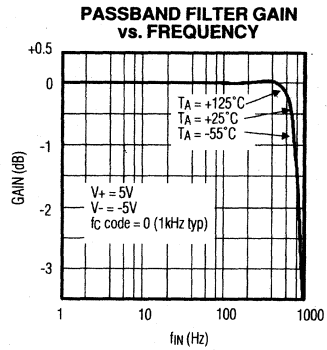
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup	t_{WS}				0	ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{WH}				0	ns
$\overline{WR}$ Pulse Width	t_{WV}		100			ns
Address-Setup Time	t_{AS}		30			ns
Address-Hold Time	t_{AH}		10			ns
Data-Setup Time	t_{DS}		30			ns
Data-Hold Time	t_{DH}		10			ns

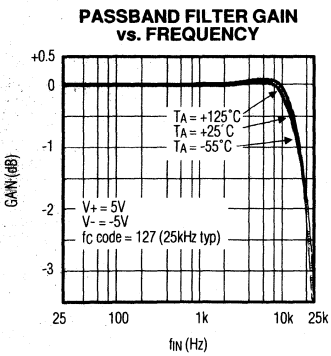
Note 11: All input control signals specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a +1.6V voltage level.

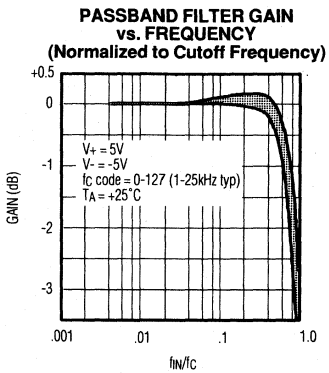
Typical Operating Characteristics

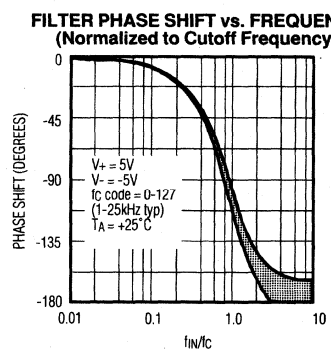








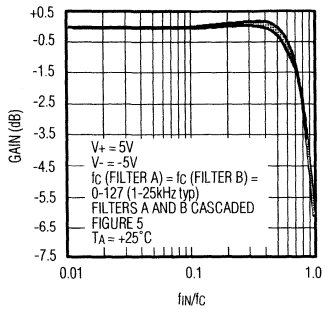




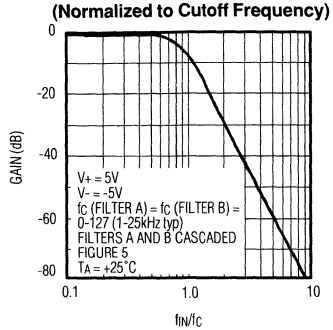
Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Typical Operating Characteristics (continued)

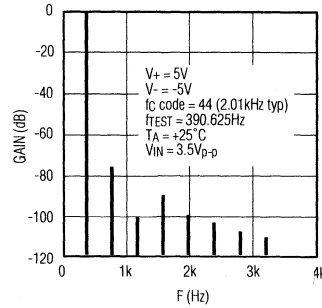
CASCADED FILTER GAIN vs. FREQUENCY (Normalized to Cutoff Frequency)



CASCADED FILTER GAIN vs. FREQUENCY (Normalized to Cutoff Frequency)



FILTER HARMONIC DISTORTION

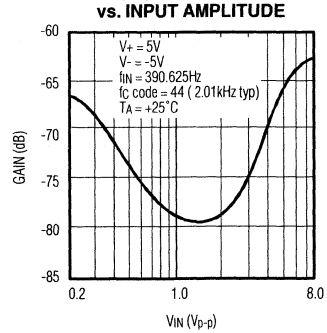


FILTER TOTAL HARMONIC DISTORTION + NOISE vs. INPUT FREQUENCY

fIN (Hz)	fC Code	fC (Hz) (Typ)	THD + NOISE (dB)
190	0	1k	-78
390	44	2.01k	-73
1367	100	7.01k	-67
4875	127	25k	-66

V+ = 5V, V- = -5V; VIN = 3.5VP-P; TA = +25°C

FILTER TOTAL HARMONIC DISTORTION + NOISE vs. INPUT AMPLITUDE

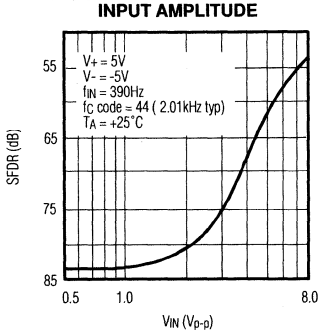


MAX271 FILTER + TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. INPUT FREQUENCY

fIN (Hz)	fC Code	fC (Hz) (Typ)	SFDR (dB)
195	0	1k	73.5
781	72	4.01k	69.5
1562.5	105	8.08k	66
3906	124	19.4k	61.5

V+ = 5V, V- = -5V; VIN = 3.5VP-P;
T/H SWITCHED AT 50kHz, 50% DUTY CYCLE;
TA = +25°C

MAX271 FILTER + TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. INPUT AMPLITUDE



MAX271 FILTER + TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY

FSAMPLE (Hz)	fIN (Hz)	fC Code	fC (Hz)	SFDR (dB)
100k	781	72	4.01k	72
200k	1562	105	8.08k	72
500k	3906	124	19.4k	64

V+ = 5V, V- = -5V; VIN = 3.5VP-P;
T/H SWITCHED AT 50% DUTY CYCLE;
TA = +25°C

6

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Detailed Description

Figures 1a, 1b, and 1c show the MAX270/MAX271 functional diagrams. Both the MAX270 and MAX271 contain two independent, second-order, Sallen-Key, lowpass filter sections, A and B, to provide a frequency vs. gain rolloff of approximately 40dB/decade. These are not switched-capacitor filters, but have a continuous-time design similar to discrete active filters built around op amps. The MAX270/MAX271 eliminate clock noise and aliasing problems which limit low-noise performance of switched-capacitor filters; resulting dynamic range is over 96dB.

Each filter section contains two banks of programmable capacitors, controlled by an internal 7-bit memory, which set filter cutoff frequencies (f_C) from 1kHz to 25kHz. The filters provide two program modes. In µP mode, cutoff frequencies are programmed by writing 7-bit data to one of two memory addresses (one for each filter section). Alternately, a pin-strap programming mode programs both filter sections simultaneously. In this mode, both memory latches are transparent (not addressable), and data pins D0-D6 may be pin strapped (hardwired) to set a common f_C for both filter sections.

The filters are trimmed at the wafer level, setting Q for a maximum of 0.15dB passband peaking for f_C programmed to 1kHz. Maximum passband peaking at other codes is typically less than 0.15dB. Filter Q is not user-programmable.

The MAX270 includes an uncommitted op amp (noninverting input grounded); the MAX271 has an on-chip T/H that tracks and holds the output of either filter section (selectable). The held output is provided at T/H OUT. T/H functions are controlled by writing control bits to internal registers (in µP mode) or by control pins directly (in pin-strap mode).

The MAX270 and MAX271 provide a low quiescent current shutdown mode controlled by the $\overline{SHDN}$ pin, which turns off internal amplifiers and floats all outputs, reducing quiescent operating current to less than 15µA. When the MAX271 is in µP mode, shutdown mode is selected by writing control bits to memory (the $\overline{SHDN}$ pin is disabled).

Pin Descriptions

MAX270

PIN #	NAME	FUNCTION
1	OP OUT	Uncommitted Op-Amp Output
2	V+	Positive Supply Voltage
3	OUTA	Filter A Output
4	$\overline{SHDN}$	$\overline{SHUTDOWN}$ Control. Low level floats OUTA, OUTB, and OP OUT and places device into shutdown mode.
5	INA	Filter A Input
6	V-	Negative Supply Voltage
7	INB	Filter B Input
8	OUTB	Filter B Output
9	GND	Ground
10	$\overline{WR}$	$\overline{WRITE}$ Control Input. A low level writes data D0-D6 to program memory addressed by A0. High level latches data.
11	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input. Must be low for $\overline{WR}$ input to be recognized.
12	A0	Three-Level Address Input– logic high: addresses filter A logic low: addresses filter B connect to V-: pin-strap mode
13-19	D0-D6	7-Bit Data Inputs. Allows programming of 128 cutoff frequencies in a 1kHz to 25kHz range.
20	OP IN	Uncommitted Op-Amp Input

Note: All digital input levels are TTL and CMOS compatible, unless otherwise stated.

MAX271 Pin Description on next page

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Pin Descriptions (continued)

MAX271

PIN #	NAME	FUNCTION, µP MODE (MODE = GND OR V-)	FUNCTION, PIN-STRAP MODE (MODE = V+)
1	T/H OUT	Track-and-Hold Output	
2	V+	Positive Supply Voltage	
3	OUTA	Filter A Signal Output	
4	$\overline{SHDN}$	X	$\overline{SHUTDOWN}$ Control. A low level floats outputs and places device into shutdown mode.
5	INA	Filter A Signal Input	
6	V-	Negative Supply Voltage	
7	INB	Filter B Signal Input	
8	MODE	Selects µP mode when tied to GND or V- and pin-strap mode when connected to V+.	
9	OUTB	Filter B Signal Output	
10	GND	Ground	
11	T/H A/$\overline{B}$	X	Track-and-Hold Input Control. A high/low level internally connects OUTA/OUTB to input of Track-and-Hold.
12	$\overline{WR}$	$\overline{WRITE}$ Control Input. A low level writes data D0-D6 to program memory addressed by A1, A0 (or performs function as described for address inputs). High level latches data.	X
13	T/H EN	X	Track-and-Hold Output Control. Low level floats T/H OUT. Connect pin high for normal operation.
14	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input. Must be low for $\overline{WR}$ input to be recognized.	X
15, 16	A1, A0	Address and µP Control Inputs. 0, 0 Programs fc, filter A. 0, 1 Programs fc, filter B. 1, 0 Controls T/H functions: D0 performs T/H EN pin function. D1 performs T/H A/$\overline{B}$ pin function. 1, 1 Controls device shutdown: D0 performs $\overline{SHDN}$ pin function. Note: The $\overline{WR}$ pin must be strobed low to initiate a program/function (Figure 2).	X
17-23	D0-D6	7-bit Data Inputs. Allows programming of 128 cutoff frequencies (also performs control functions as described above).	7-bit Data Inputs. Program memory latches are transparent in this mode. Connect pins high or low to program filters A and B simultaneously to the same fc.
24	$\overline{T}$/H	Track-and-Hold Control. Low level causes T/H OUT to track selected filter output. Filter output level held at T/H OUT synchronous with $\overline{T}$/H rising transition.	

X = Pin has no function in this mode.

Note: All digital input levels are TTL and CMOS compatible, unless otherwise stated.

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

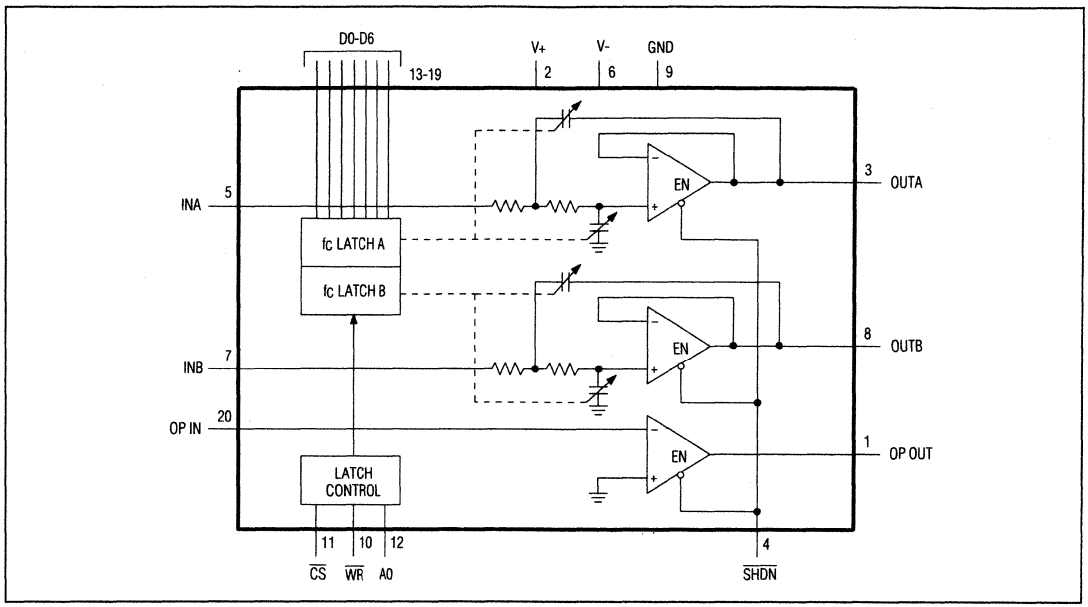


Figure 1a. MAX270 Block Diagram

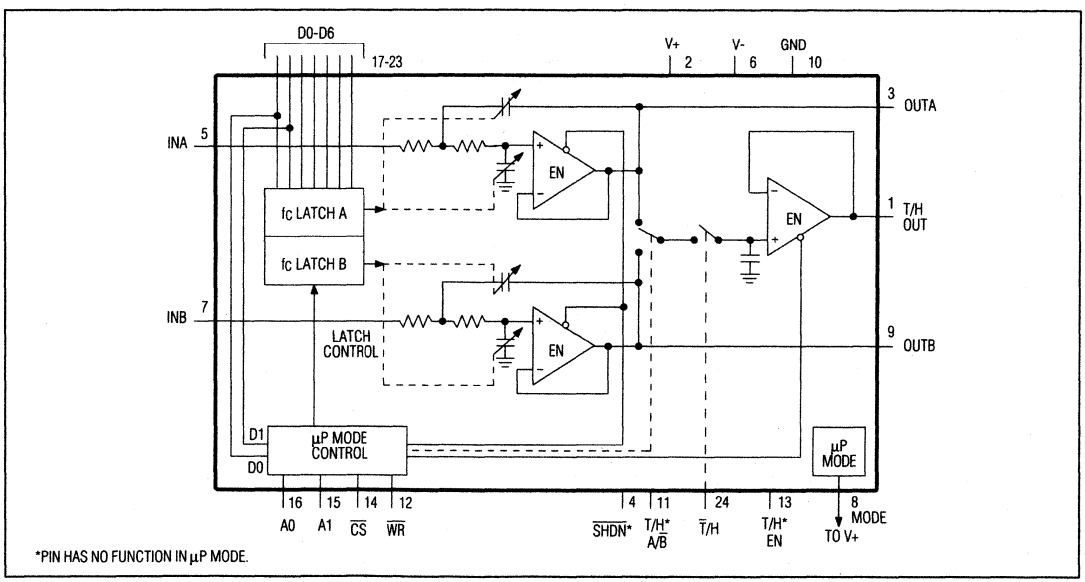


Figure 1b. MAX271 Block Diagram - µP Mode

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

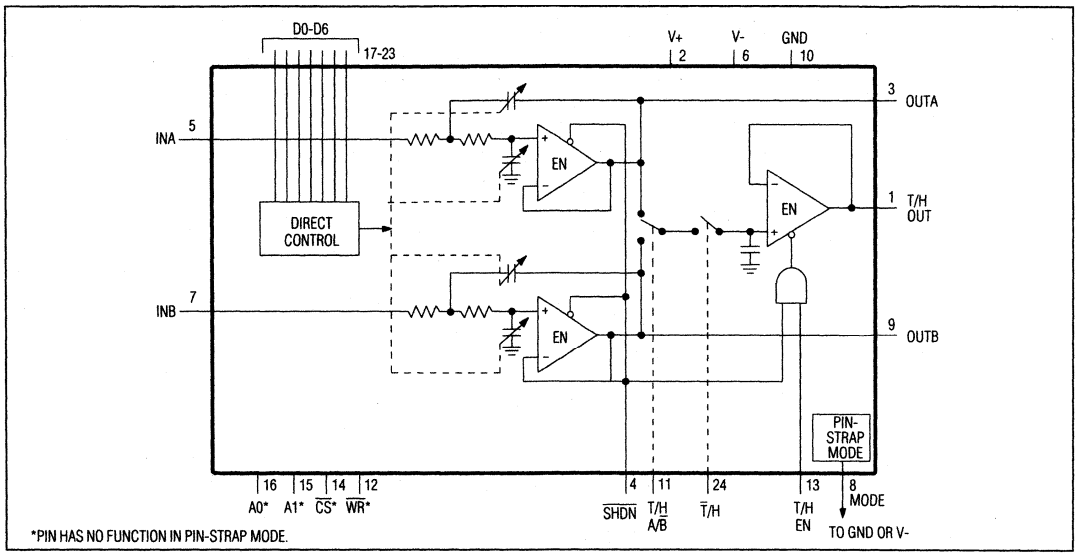


Figure 1c. MAX271 Block Diagram - Pin-Strap Mode

Filter Programming

Cutoff Frequency

f_C is the frequency of 3dB attenuation in the filter response.

Table 1 shows how data pins D0-D6 allow programming of 128 cutoff frequencies from 1kHz to 25kHz.

The equations for calculating f_C from the programmed code are as follows:

$$f_C = \frac{87.5}{87.5 - CODE} \times 1kHz \quad \text{for codes 0-63 } (f_C = 1kHz \text{ to } 3.57kHz)$$

$$f_C = \frac{262.5}{137.5 - CODE} \times 1kHz \quad \text{for codes 64-127 } (f_C = 3.57kHz \text{ to } 25kHz)$$

where CODE is the data on pins D0-D6 (0-127). D6 is the most significant bit (MSB).

Actual cutoff frequencies are subject to some error for each programmed code. Highest accuracy occurs at CODE = 0 where filters are trimmed for a 1kHz cutoff frequency. At higher codes, CODE vs. f_C errors increase; the frequency error at CODE = 127 (highest code) remains typically within ±9.5%. This means that the actual filter cutoff frequency, when programmed to CODE = 127, falls between 22.63kHz and 27.38kHz.

6

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Table 1. Programmed Cutoff Frequency Codes (Typ)

PROGRAMMED CODE	fc (kHz)	PROGRAMMED CODE	fc (kHz)	PROGRAMMED CODE	fc (kHz)	PROGRAMMED CODE	fc (kHz)
0	1.000	32	1.576	64	3.571	96	6.325
1	1.011	33	1.605	65	3.620	97	6.481
2	1.023	34	1.635	66	3.671	98	6.645
3	1.035	35	1.666	67	3.723	99	6.818
4	1.047	36	1.699	68	3.777	100	7.008
5	1.060	37	1.732	69	3.832	101	7.191
6	1.073	38	1.767	70	3.888	102	7.394
7	1.087	39	1.804	71	3.947	103	7.608
8	1.100	40	1.842	72	4.007	104	7.835
9	1.114	41	1.881	73	4.069	105	8.076
10	1.129	42	1.923	74	4.133	106	8.333
11	1.143	43	1.966	75	4.200	107	8.606
12	1.158	44	2.011	76	4.268	108	8.898
13	1.174	45	2.058	77	4.338	109	9.210
14	1.190	46	2.108	78	4.411	110	9.545
15	1.206	47	2.160	79	4.487	111	9.905
16	1.223	48	2.215	80	4.565	112	10.294
17	1.241	49	2.272	81	4.646	113	10.714
18	1.259	50	2.333	82	4.729	114	11.170
19	1.277	51	2.397	83	4.816	115	11.666
20	1.296	52	2.464	84	4.906	116	12.209
21	1.315	53	2.536	85	5.000	117	12.804
22	1.335	54	2.611	86	5.097	118	13.461
23	1.356	55	2.692	87	5.198	119	14.189
24	1.378	56	2.777	88	5.303	120	15.000
25	1.400	57	2.868	89	5.412	121	15.909
26	1.422	58	2.966	90	5.526	122	16.935
27	1.446	59	3.070	91	5.645	123	18.103
28	1.470	60	3.181	92	5.769	124	19.444
29	1.495	61	3.301	93	5.898	125	21.000
30	1.521	62	3.431	94	6.034	126	22.826
31	1.548	63	3.571	95	6.176	127	25.000

Programmed code is the data on pins D0-D6 (0-127). D6 is the MSB.

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

MAX270 Control Interface

The A0 pin is a three-level input that selects the memory addresses for updating cutoff frequency data in µP mode:

A0	SELECTS
Logic Low	Filter B
Logic High	Filter A

Figure 2 shows µP-mode interface timing.

Connecting A0 to the negative supply selects pin-strap mode. Pin-strap mode allows filter programming with no timing requirements. Internal memory latches are disabled, permitting filters A and B to be programmed directly to f_C data strapped on D0-D6. This mode disables $\overline{CS}$ and $\overline{WR}$ controls, and filters A and B are programmed to the same f_C.

A low level on the $\overline{SHDN}$ pin shuts down all amplifiers and floats OUTA, OUTB, and OP OUT. Current consumption drops to less than 15µA in this mode.

MAX271 Control Interface

Connecting the MODE pin to GND or V- selects the µP mode. In this mode, addressable program memory controls filter cutoff frequency programming and all T/H functions, except $\overline{T}$/H. Refer to Figure 2 for timing characteristics. Table 2 describes available functions:

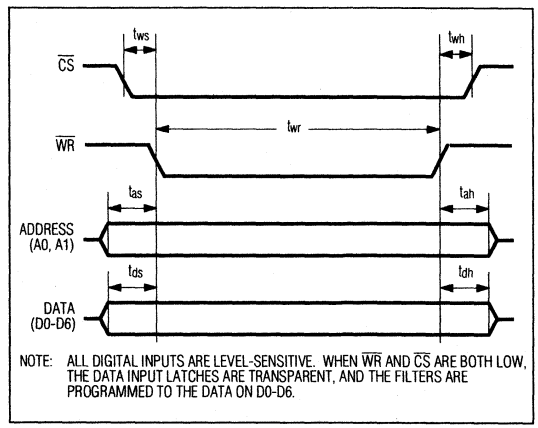


Figure 2. MAX270/MAX271 Digital Timing Diagram

In µP mode, $\overline{SHDN}$, T/H A/$\overline{B}$, and T/H EN pins are disabled. $\overline{T}$/H remains enabled and performs the T/H tracking/holding function.

Tying MODE to V+ selects pin-strap mode. In this mode, both memory latches are transparent, and data on D0-D6 controls the f_C of filters A and B directly (filters A and B are programmed to the same f_C). Pin strap D0-D6 for operation without µP. A0, A1, $\overline{CS}$, and $\overline{WR}$ are disabled.

Table 2. MAX271 µP-Mode Interface

A1	A0	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	7-bit f_C data							Selects filter A
0	1	7-bit f_C data							Selects filter B
1	0	X	X	X	X	X	X	0	T/H OUT disabled
1	0	X	X	X	X	X	X	1	T/H OUT enabled
1	0	X	X	X	X	X	0	X	Selects OUTB as input to T/H
1	0	X	X	X	X	X	1	X	Selects OUTA as input to T/H
1	1	X	X	X	X	X	X	0	Filter shutdown mode. All outputs floated, 15µA max supply current
1	1	X	X	X	X	X	X	1	Removes filter from shutdown mode

X = Don't care

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Digital Threshold Levels

All digital inputs are TTL and CMOS compatible, unless otherwise stated. Inputs are CMOS gates with less than 1µA leakage current and 8pF capacitance loading. Typical logic voltage thresholds are a function of the V+ supply voltage as shown below (voltages are referenced to GND).

V+ (V)	LOGIC THRESHOLD VOLTAGE (V)
8	+2.4
7	+2.3
6	+2.0
5	+1.75
4	+1.5
2.5	+1.0

NOTE: For +5V single-supply operation, where incoming logic signals are referenced to V-, typical logic thresholds are +3.5V. Therefore, a CMOS (rail-to-rail) logic interface is recommended.

Filter Performance

All MAX270/MAX271 internal amplifier and output stages for filter sections, uncommitted op amp, and T/H are identical. The outputs are designed to drive 5kΩ in parallel with a maximum capacitance of 100pF. At higher load levels, the output swing becomes asymmetric. All outputs can be short circuited to GND for an indefinite duration.

The MAX270/MAX271 operating frequency range is limited to aproximately 2MHz by the bandwidth of the internal amplifiers.

Filter Noise

Wideband filter noise over a 50kHz bandwidth is 12µVRMS and 38µVRMS per section for fC programmed to 1kHz and 25kHz, respectively. A dynamic range of over 96dB results.

Filter Input Impedance

At DC, the input impedance at INA and INB is equal to the DC input impedance of the amplifier, which is about 5MΩ. At higher frequencies, internal capacitors contribute to an effective input impedance that may fall as low as 100kΩ at 25kHz.

MAX271 Track-and-Hold

The MAX271 T/H is functionally equivalent to a switched 200pF capacitor buffered by a unity-gain amplifier (Figures 1b, 1c). When the $\overline{T}$/H pin is driven low, the output of filter A or filter B (whichever is selected via control interface) internally connects to the amplifier, and T/H OUT follows the filter output. The offset at T/H OUT (±6mV max) is the combined offset of the filter amplifier and the T/H buffer. When $\overline{T}$/H is pulled high, the switch disconnects the filter signal from the T/H. The T/H capacitor holds the stored charge, and that voltage is buffered at T/H OUT.

A low level at T/H EN floats T/H OUT, enabling multiplexed operation (Figure 3). T/H A/$\overline{B}$ selects between OUTA and OUTB as the T/H input. In µP mode, the T/H EN and T/H OUT functions are controlled by writing control bits to program memory, with T/H EN and T/H OUT pins disabled.

See Typical Operating Characteristics graphs for T/H dynamic accuracy.

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Applications Information

Power-Supply Configurations

MAX270/MAX271 power supplies must be properly bypassed. Best performance is achieved if V+ and V- are bypassed to GND with 4.7µF electrolytic (tantalum is preferred) and 0.1µF ceramic capacitors in parallel. These should be as close as possible to the chip supply pins.

Single supplies in the range of 4.75V to 16V may be used to power the MAX270/MAX271 as shown in Figure 4. Digital logic may be referenced to V- (system ground), but will not maintain TTL compatibility. CMOS (rail-to-rail) logic is recommended. For µP-mode operation with a single supply, the MAX270 A0 pin must be configured with a voltage divider (Figure 4).

Lowest quiescent current in shutdown mode is achieved when A0 is either at V+ or V-.

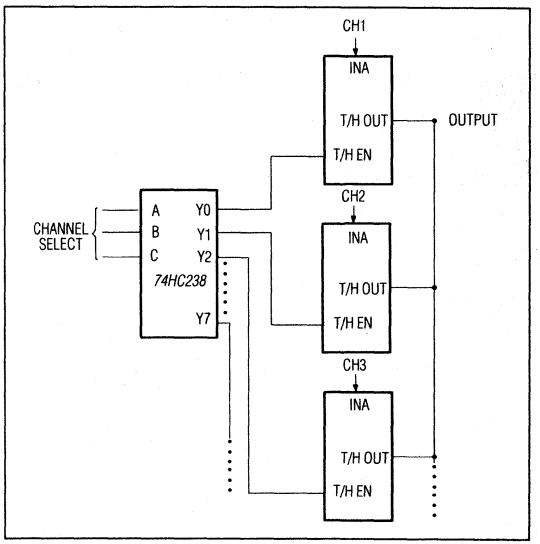


Figure 3. MAX271 Multiplexed Operation

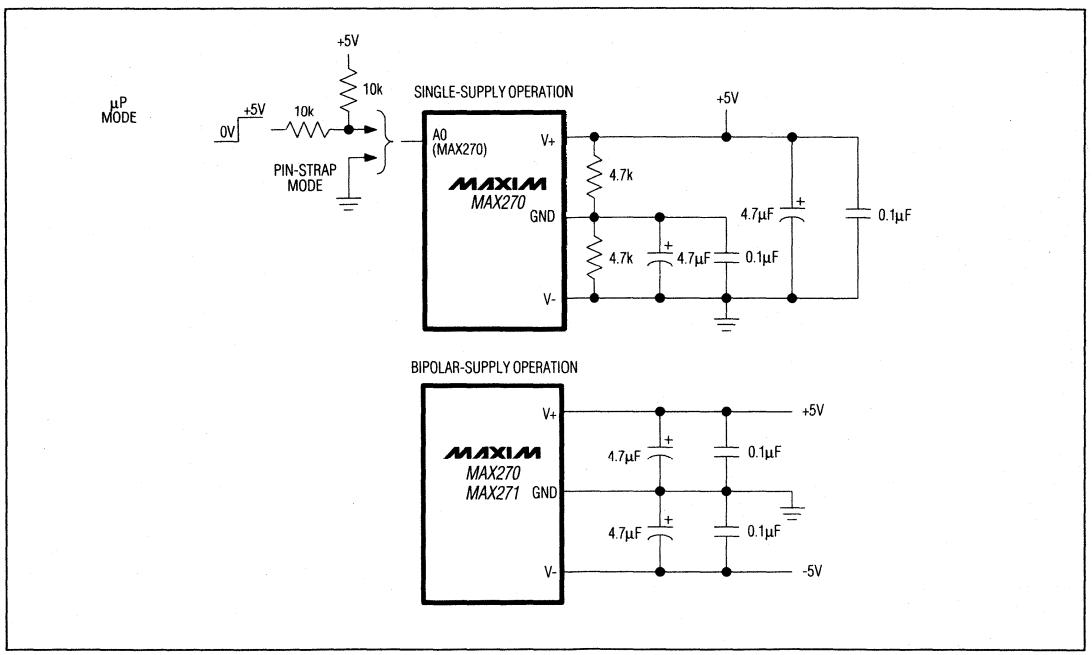


Figure 4. Power-Supply Configurations

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Independent f_C Programming Without a µP

Figure 6 shows how filter sections A and B may be programmed to different cutoff frequencies without the use of a µP. The MAX690 µP supervisory circuit provides the proper programming sequence when the circuit is powered up by controlling the 74HC373 data buffer and the MAX270 addressing pin to load independent f_C data for filters A and B.

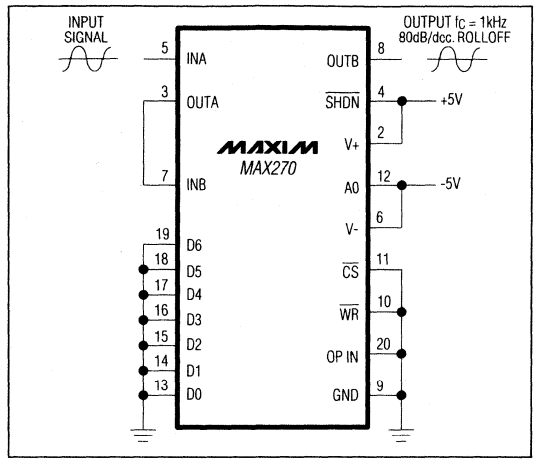


Figure 5. Cascading Filter Sections

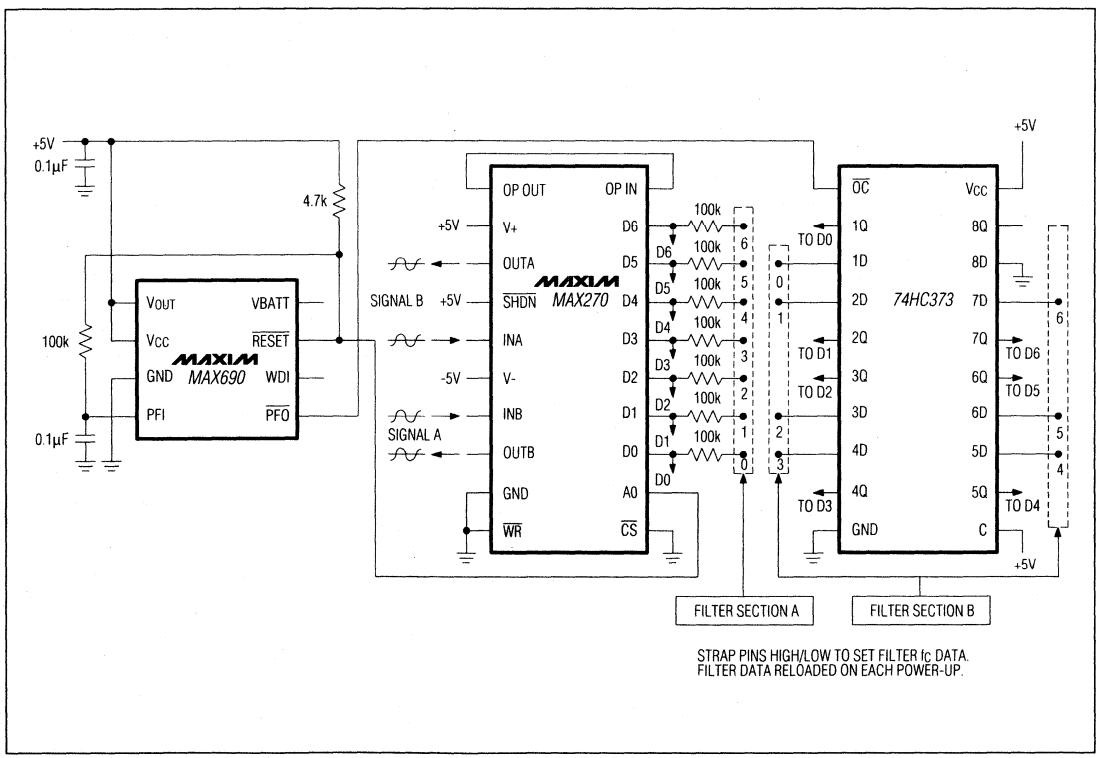
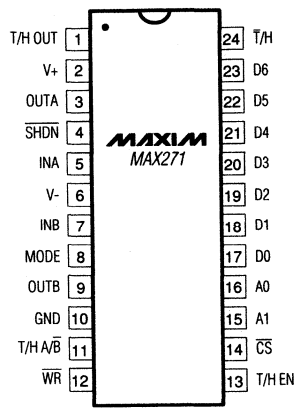


Figure 6. Independent f_C Programming Without a µP

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filters

Pin Configurations (continued)

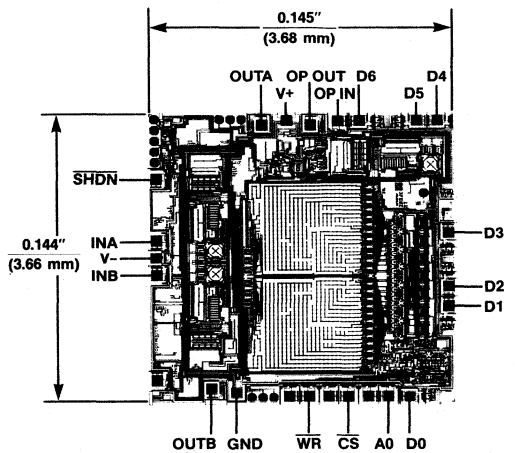
TOP VIEW



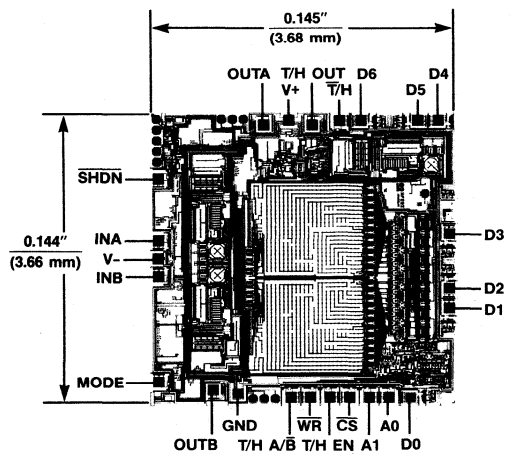
DIP/SO

Chip Topographies

MAX270



MAX271



MAXIM

8th-Order/4th-Order, Continuous-Time Analog Filters

General Description

The MAX274/MAX275 are 8th-order/4th-order, continuous-time analog filters. The MAX274 has four independent, cascadable 2nd-order sections, while the MAX275 has two. Each filter section can implement any all-pole bandpass or lowpass filter response (such as Butterworth, Bessel, and Chebyshev) and is programmed by four external resistors. The filters' continuous-time design offers low noise and a wide dynamic range by eliminating clock noise and aliasing problems characteristic of their switched-capacitor counterparts.

Allowable pole frequencies range from 100Hz to 150kHz (MAX274) and 100Hz to 300kHz (MAX275). Center-frequency accuracy is ±0.9% (MAX275), ±1.0% (MAX274) over the full operating temperature range.

These low-noise filters, with total harmonic distortion less than -86dB, are ideal for lowpass anti-aliasing and digital-to-analog converter output smoothing in high-resolution, data-conversion applications.

Applications

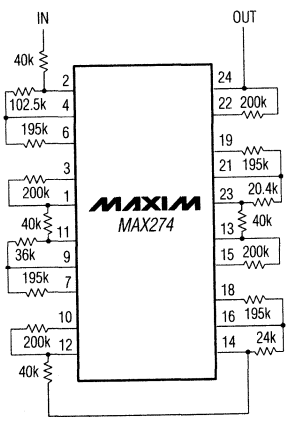
Low-Distortion, Anti-Aliasing Filters

Output Smoothing Filters

Audio/Sonar/Avionics Frequency Filtering

Vibration Analysis

Typical Operating Circuit

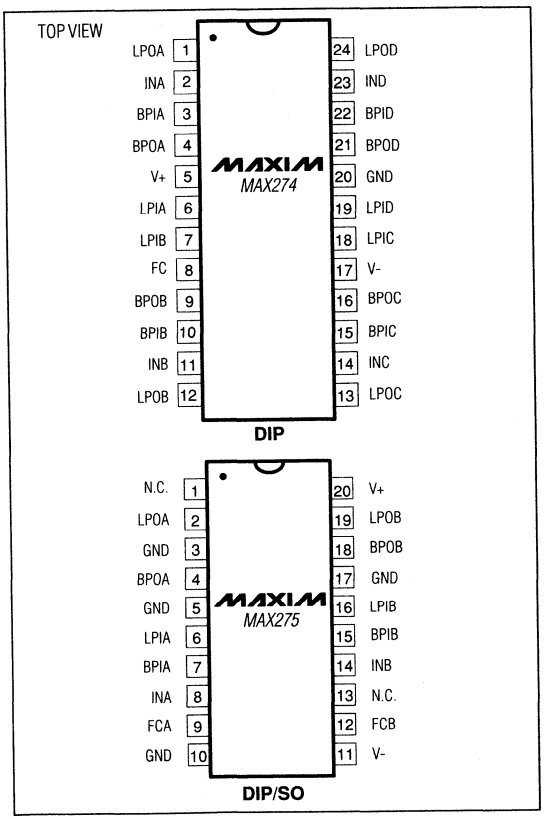


10kHz 8TH-ORDER BUTTERWORTH LOWPASS FILTER

Features

- ♦ **Continuous-Time Filters - No Clock, No Clock Noise**
- ♦ **8th-Order, Quad 2nd-Order Sections (MAX274)**
  4th-Order, Dual 2nd-Order Sections (MAX275)
- ♦ **Lowpass/Bandpass Outputs**
- ♦ **Low Noise; Low Distortion (-86dB Typ)**
- ♦ **±0.9% Frequency Accuracy Over Temperature**
- ♦ **Supplies: ±5V, +5V, +12V, or +15V (MAX274)**
  ±5V or +5V (MAX275)
- ♦ **Pole Frequency Range: 100Hz to 150kHz (MAX274)**
  100Hz to 300kHz (MAX275)
- ♦ **Cascadable for Higher Order**
- ♦ **DIP and SO Packages**

Pin Configurations



5th Order, Zero DC Error, Lowpass Filter

General Description

The MAX280/LTC1062 is a 5th order all pole instrumentation lowpass filter with no DC Error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing excellent DC accuracy.

This resistor and capacitor along with the on-chip 4th order switched capacitor filter form a 5th order lowpass filter. Two MAX280/LTC1062s can be cascaded to form a 10th order lowpass filter.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is 100:1, allowing clock ripple to be easily removed.

The MAX280 is an enhanced version of the LTC1062. Enhancements include tighter specifications on the internal clock oscillator frequency and the buffer amplifier offset voltage.

Applications

Anti-Aliasing Filter

Data Loggers

Digital Voltmeters

Weigh Scales

Strain Gauges

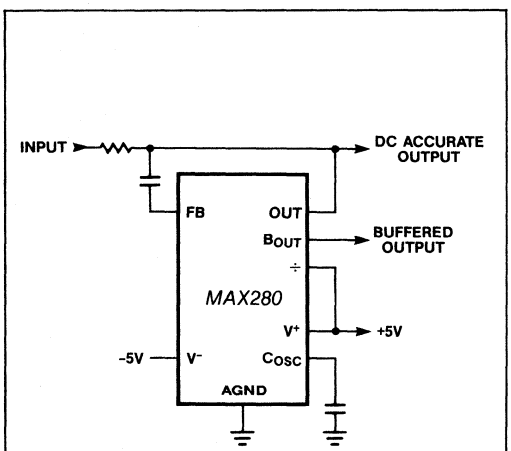
Features

- **Lowpass Filter with No DC Error**
- **Low Passband Noise**
- **DC to 20kHz Cutoff Frequency**
- **5th Order All Pole Filter**
- **Internal or External Clock**
- **Cascadable for Higher Order Rolloff**
- **Buffered Output Available**
- **8-Pin DIP or 16-Pin SOIC**

Ordering Information

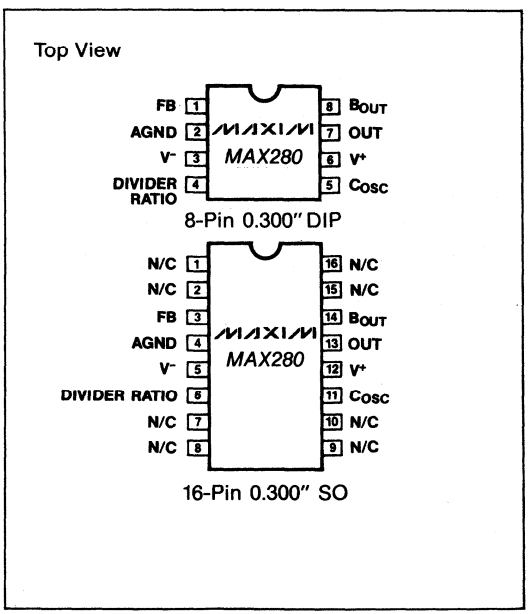
PART	TEMP. RANGE	PACKAGE
MAX280CPA	0°C to +70°C	8 Lead Plastic DIP
MAX280CWE	0°C to +70°C	16 Lead Wide SO
MAX280EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX280EWE	-40°C to +85°C	16 Lead Wide SO
MAX280MJA	-55°C to +125°C	8 Lead CERDIP
LTC1062CN8	-40°C to +85°C	8 Lead Plastic DIP
LTC1062CJ8	-40°C to +85°C	8 Lead CERDIP
LTC1062CS	-40°C to +85°C	16 Lead Wide SO
LTC1062MJ8	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



Lowpass Filter

Pin Configurations



5th Order, Zero DC Error, Lowpass Filter

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage at Any Pin ..... $V^- -0.3V \le V_{IN} \le V^+ +0.3V$
Operating Temperature
MAX280CXX/LTC1062C ..... -0°C to +70°C
MAX280EXX ..... -40°C to +85°C
MAX280MXX/LTC1062M ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 6.25mW/°C above 70°C) 500mW
CERDIP (derate 8.00mW/°C above 70°C) 640mW
SO (derate 9.52mW/°C above 70°C) 762mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, T_A = 25°C, unless otherwise specified, AC output measured at pin 7, Figure 1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Dual Supply Single Supply			 ±2.375 4.75		 ±8.0 16.0	V
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100pF T_A = 25°C $T_A = T_{MIN}$ to T_{MAX}			 5.0 5.0	 7.0 10.0	mA
Input Frequency Range				0-20		kHz
Filter Gain at f_{IN} = 0 $f_{IN} = 0.5f_C$ (Note 1) $f_{IN} = f_C$ $f_{IN} = 2f_C$ $f_{IN} = 4f_C$	f_{CLK} = 100kHz, Pin 4 at V^+ C = 0.01µF, R = 25.78kΩ $T_A = T_{MIN}$ to T_{MAX} $T_A = T_{MIN}$ to T_{MAX} $T_A = T_{MIN}$ to T_{MAX}		 -2 -28 -54	 0 -0.02 -3 -30 -60	 -0.3 	dB
Clock to Cutoff Frequency Ratio f_{CLK}/f_C	f_{CLK} = 100kHz, Pin 4 at V^+ C = 0.01µF, R = 25.78kΩ			100 ± 1		
Filter Gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+ C = 0.01µF, R = 6.5kΩ $T_A = T_{MIN}$ to T_{MAX}		-48	-52		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an ext op amp $T_A = T_{MIN}$ to T_{MAX}		±3.5	±3.8		V
Clock Feedthrough				10		mV_{pp}
INTERNAL BUFFER						
Bias Current	T_A = 25°C $T_A = T_{MIN}$ to T_{MAX}			2 170	50 1000	pA
Offset Voltage	MAX280 LTC1062			0.2 2	2 20	mV
Voltage Swing	R1 = 20kΩ; $T_A = T_{MIN}$ to T_{MAX}		±3.5	±3.8		V
Short Circuit Current Source/Sink				30/2		mA
CLOCK (NOTE 2)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF	MAX280	31	35	39	kHz
		LTC1062	25	35	50	
	$T_A = T_{MIN}$ to T_{MAX} C_{OSC} (Pin 5 to V^-) = 100pF	MAX280	29	35	43	
		LTC1062	15	35	65	
Max Clock Frequency				4		MHz
C_{OSC} Input Sink/Source Current	$T_A = T_{MIN}$ to T_{MAX}			25	80	µA

Note 1: f_C is the frequency where the gain is -3dB with respect to the input signal.
Note 2: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, f_{CLK}/f_C = 100; when pin 4 = GND, f_{CLK}/f_C = 200; pin 4 = V^-, f_{CLK}/f_C = 400.

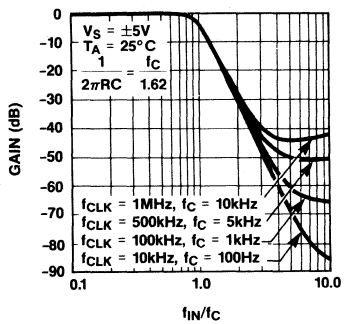
5th Order, Zero DC Error, Lowpass Filter

Pin Description

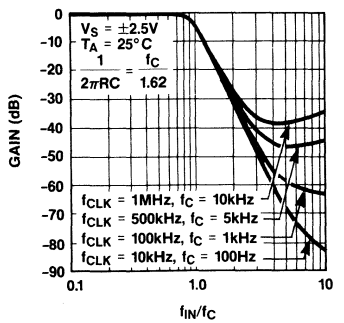
PIN #	NAME	FUNCTION
1	FB	External capacitor couples to the chip through this pin.
2	AGND	Ground. Connect to system ground for dual supply operation or mid-supply for single operation. This pin should be well bypassed using a large capacitor for single supply operation.
3	V^-	Negative supply voltage
4	DIVIDER RATIO	The oscillator frequency is divided by either 1, 2, or 4 depending upon the voltage on this pin. This in turn gives a clock to cutoff frequency ratio when tied to V^+ of 100:1; when tied to GND of 200:1; and when tied to V^- of 400:1.
5	C_{OSC}	Clock input pin for external clock applications. For internal clock operation connect an external capacitor between this pin and V^-.
6	V^+	Positive supply voltage
7	OUT	Input to on-chip buffer amplifier
8	B_{OUT}	Output of buffer amplifier

Typical Operating Characteristics

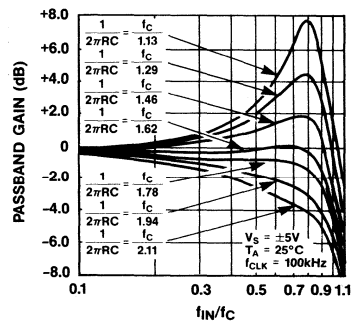
GAIN NORMALIZED TO CUTOFF FREQUENCY (V_S = ±5V)



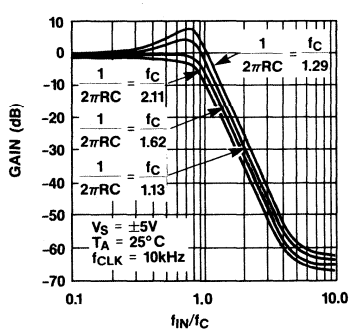
GAIN NORMALIZED TO CUTOFF FREQUENCY (V_S = ±2.5V)



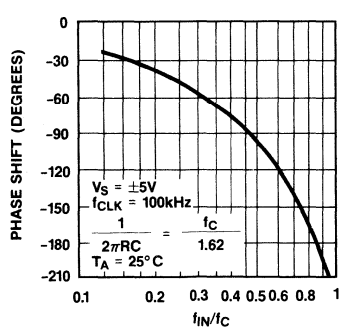
PASSBAND GAIN vs. INPUT FREQUENCY



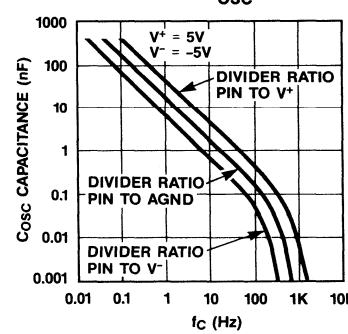
GAIN vs. INPUT FREQUENCY



PASSBAND PHASE SHIFT vs. INPUT FREQUENCY



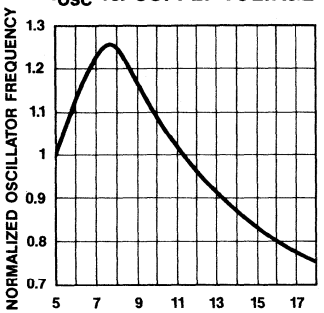
CUTOFF FREQUENCY vs. C_{OSC}



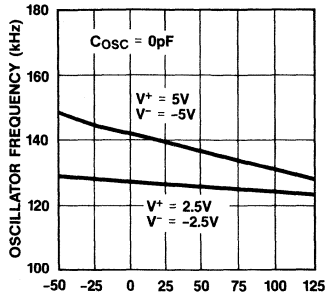
5th Order, Zero DC Error, Lowpass Filter

Typical Operating Characteristics (continued)

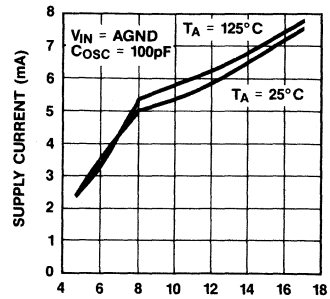
NORMALIZED OSCILLATOR FREQUENCY f_{OSC} vs. SUPPLY VOLTAGE



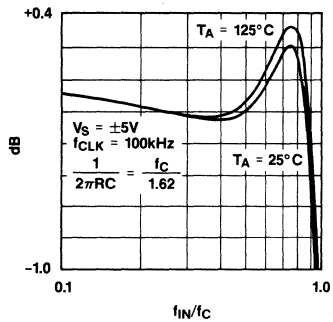
OSCILLATOR FREQUENCY, f_{OSC} vs. AMBIENT TEMPERATURE



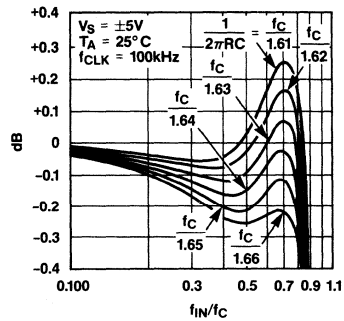
POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



VARIATION OF PASSBAND GAIN WITH TEMPERATURE



PASSBAND GAIN vs. INPUT FREQUENCY



Introduction

Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form a 5th order lowpass filter. The input and output appear across an external resistor and the IC part of the overall filter handles only the AC path of the signal. The DC offsets of the buffer and the switched capacitor network are blocked by the capacitor and do not appear at the zero offset output pin.

Use of this external resistor and capacitor also automatically provides the required anti-aliasing filtering for the sampled filter. Further, low frequency noise in the filter IC is attenuated by the external capacitor since any noise at the FB pin goes through a highpass path to the filter output. The filter output pin is unbuffered. This signal can be buffered by the on-chip buffer or by a high accuracy op amp (such as a chopper stabilized op amp) to obtain a buffered DC accurate system. The on-chip buffer has an offset voltage of 2mV for the MAX280 and 20mV for the LTC1062. The offset voltage for both devices have a typical tempco of 1μV/°C.

Detailed Description

Clock Requirements

Using Divider Ratio

DIVIDER RATIO sets the ratio between the internal f_{CLK} (supplied to the MAX280/LTC1062) and f_{OSC} (the output at the DIVIDER RATIO pin). Connect DIVIDER RATIO to V^+ for a 1/1, to GND for a 1/2, and to V^- for a 1/4 f_{CLK}/f_{OSC} ratio.

Using Internal Oscillator

The internal 140kHz (nominal) oscillator frequency can be modified by connecting an external capacitor

in parallel with the on-chip 33pF capacitor; from the C_{OSC} pin to GND (or to V^- if the capacitor is polarized).

The clock frequency can be calculated by:

$$f_{OSC} = 140kHz\ (33pF/(33pF+C_{OSC})) \quad (1)$$

Due to process tolerances, f_{OSC} can vary by ±62.5% in the LTC1062. In the MAX280, on-chip trimming reduces the f_{OSC} tolerance to ±19.5%. The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the C_{OSC} pin as shown in Figure 2. The new frequency can be computed as:

$$f'_{OSC} = f_{OSC}/(1-4RC_{OSC}f_{OSC}) \quad (2)$$

where f_{OSC} is the value of the oscillator frequency when R = 0. When an external potentiometer is used, the new value of the oscillator frequency is always higher than the one calculated in (equation 1). To achieve a wide tuning range, calculate (equation 1) the ideal f_{OSC}, C_{OSC} pair, then double the value of C_{OSC} and use a 50k potentiometer to adjust f'_{OSC}. For example: to obtain a 1kHz oscillator frequency, C_{OSC} is 3900pF. By using 6800pF for C_{OSC} and a 50kΩ potentiometer, the clock frequency can be adjusted from 500Hz to 1.56kHz. The internal oscillation frequency can be measured directly at the C_{OSC} pin using a low capacitance probe.

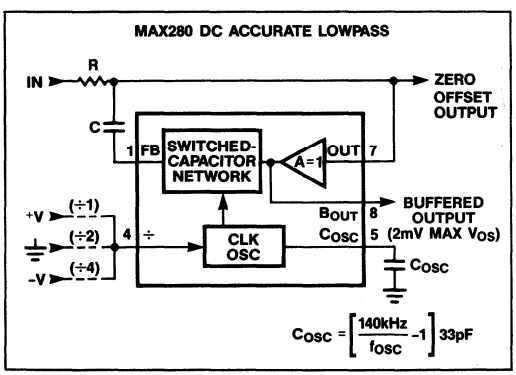


Figure 1. Block Diagram

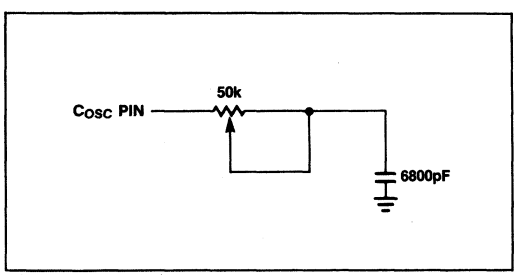


Figure 2. External Oscillator Trim

Using an External Clock

The internal switched capacitor filter requires a clock 100 times higher than the desired cutoff frequency. If an external clock is used the input on the C_{OSC} pin must swing close to the power rails (V^+,V^-). Although standard 74HC00 series CMOS gates do not guarantee CMOS levels with the source and sink currents of the C_{OSC} pin, they will in reality drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and current to simultaneously drive several chips. The typical trip levels of the internal Schmitt trigger sensing C_{OSC} pin are:

POWER SUPPLY		TRIP LEVEL	
V^+ = +2.5V	V^- = -2.5V	V_{IH} = 0.9V	V_{IL} = -1.15V
V^+ = +5.0V	V^- = -5.0V	V_{IH} = 1.4V	V_{IL} = -2.1V
V^+ = +6.0V	V^- = -6.0V	V_{IH} = 1.7V	V_{IL} = -2.5V
V^+ = +5.0V	V^- = 0V	V_{IH} = 3.4V	V_{IL} = 1.35V
V^+ = +10V	V^- = 0V	V_{IH} = 6.4V	V_{IL} = 2.9V
V^+ = +15V	V^- = 0V	V_{IH} = 9.5V	V_{IL} = 4.1V

Choosing External Resistor and Capacitor Values

The external resistor and capacitor is used as part of a feedback loop for the filter and also forms one pole. The internal 4 pole switched capacitor filter is driven by a clock which also determines the filter cutoff frequency. For a maximally flat amplitude response, the clock should be 100 times the desired cutoff frequency and the resistor and capacitor should be chosen such that:

$$\frac{f_C}{1.62} = \frac{1}{2\pi RC}$$

where f_C = filter cutoff frequency, (-3dB point)

For example to implement a 10Hz cutoff filter, a 1kHz clock is required with $1/2\pi RC$ = 10Hz/1.62 = 6.17Hz.

Typically R is chosen to be around 20kΩ. The minimum value of R depends upon the maximum input signal, and the current sinking capability of the FB pin (typically 1mA). So for a 1V peak-to-peak signal, the minimum value of the resistor is 1kΩ.

The passband response for values of $1/(2\pi RC)$ around (f_C/1.62) can be seen on the Passband Gain vs. Input Frequency plot (see Typical Operating Characteristics). If maximum flatness is required (as in Butterworth filters), the RC product should be well controlled. When the input resistor and capacitor cutoff frequency approaches the cutoff frequency of the on-chip 4th order filter, response peaking becomes severe as can be seen in the response plots. However the attenuation slope is virtually unaffected by the resistor and capacitor since it is set by internal circuitry. This can be seen in the Gain vs. Input Frequency plot.

For wide temperature range applications NPO ceramic capacitors are recommended. Their tempcos are around ±20ppm and values are available to 0.1μF.

5th Order, Zero DC Error, Lowpass Filter

Other ceramic capacitors are not recommended due to their large tempcos. Mylar, polystyrene and polypropylene capacitors all provide acceptable performance. Solid tantalum capacitors connected back-to-back and disc ceramic capacitors introduce additional passband errors (0.05-0.1dB).

Applications Information

Filter Input Voltage Range

Every node of the filter typically swings within 1V of both supplies. With the appropriate external resistor and capacitor values, the amplitude response of all the internal and external nodes should not exceed a gain of 0dB with the exception of the FB pin. The amplitude response of the FB pin, where some peaking may occur, is shown in Figure 3. For an input frequency around $0.8f_C$, the gain is 1.7V/V and, with ±5V supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform may occur; however, the filter will not be damaged. The absolute maximum input voltage to any pin should not exceed the power supplies.

Internal Buffer

The internal output buffer of the FB pin and the OUT pin is part of the AC signal path. Hence capacitive loading greater than 30pF may cause gain errors in the passband around the cutoff frequency. The internal buffer can also be used as the filter output, however, there will be a few millivolts of output offset.

Filter Attenuation

The rolloff is 30dB/octave. When the clock rate is increased and hence the cutoff frequency is increased, the filter's maximum attenuation decreases as shown in the Typical Operating Characteristics. This decrease is caused by rolloff at higher frequencies of the loop gains of the various internal feedback paths and is not due to any increase in noise floor.

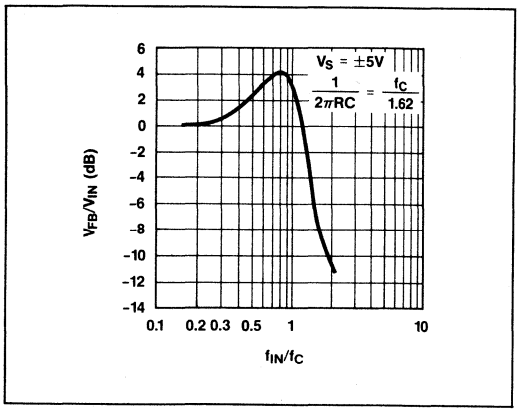


Figure 3. Amplitude Response of FB Pin

Filter Noise

The filter wideband noise is typically $90\mu V_{RMS}$ with ±5V supplies and typically $80\mu V_{RMS}$ for ±2.5V supplies or a +5V single supply. This value is nearly independent of the cutoff frequency. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below 0.1 f_C. Roughly 2/3 of the entire wideband noise is in the band DC to f_C.

Transient Response

Figure 4A shows the step response of the filter. This response approximates that of an ideal 5th order maximally flat (Butterworth) filter. The ringing in the transient response can be reduced by using a Bessel filter. The Bessel filter response can be approximated by setting $1/2\pi RC$ to $f_C/2$ instead of $f_C/1.62$. Figure 4B shows the step response of the Bessel approximation.

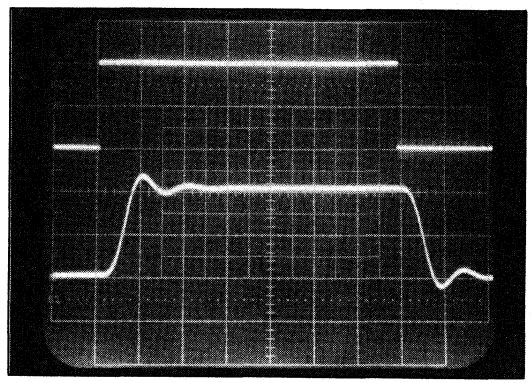


Figure 4A. Step Response of Butterworth Approximation

$$\frac{1}{2\pi RC} = \frac{f_C}{1.62}, \text{ (1mS/div., 0.5V/div.)}$$

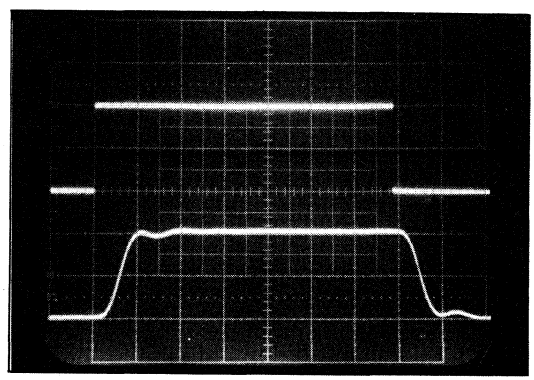


Figure 4B. Step Response of Bessel Approximation

$$\frac{1}{2\pi RC} = \frac{f_C}{2}, \text{ (1mS/div., 0.5V/div.)}$$

5th Order, Zero DC Error, Lowpass Filter

Anti-Aliasing

The internal 4th order switched capacitor filter is a sampled device and as such will alias unless preceded by a band limited signal, or a continuous non-sampled filter. The external resistor and capacitor used to form the 5th filter pole also automatically provides this function. Attenuation is greater than 43dB at the Nyquist frequency.

Single Supply Operation

Figure 5 shows a schematic for single supply operation. The AGND pin and the OUT pin should be biased at 1/2 supply. The value of the resistors R1 and R2 should be chosen to conduct 100μA or more. R′ DC biases the buffer and C′ isolates the buffer from the DC value of the output. Under these conditions the external resistor and capacitor should be adjusted such that $(1/2\pi RC) = f_C/1.84$. This accounts for the extra loading of the R′,C′ combination. R′ and C′ are not required if the input voltage has a DC value around 1/2 supply. If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground. The AGND pin should also be bypassed by a decoupling capacitor.

Clock Feedthrough

Clock feedthrough can be reduced by using a resistor and capacitor at the buffered output pin provided that this pin is used as an output. If an external op amp is used to buffer the DC accurate output, an input resistor and capacitor can be used to eliminate clock feedthrough (see Figure 6) and further reduce the attenuation floor of the filter.

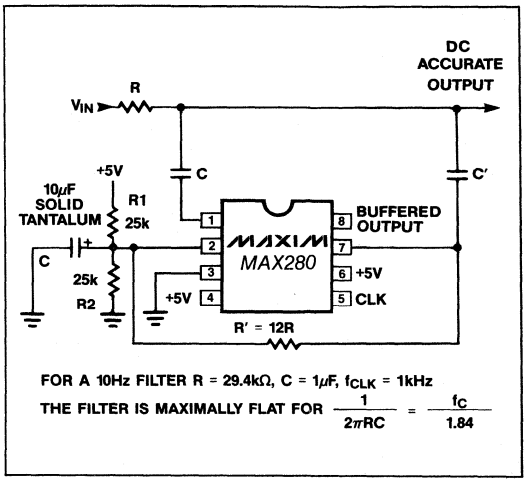
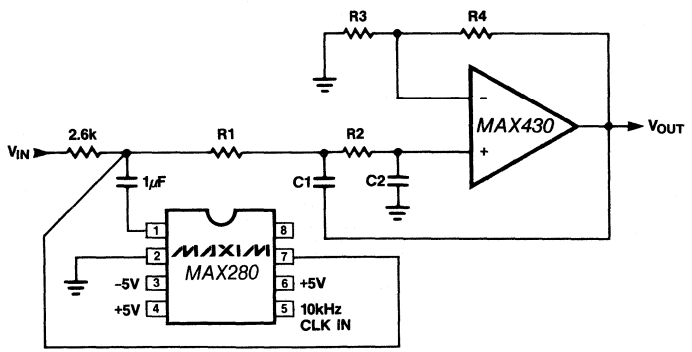


Figure 5. Single 5V Supply 5th Order LP Filter



THE MAX430 IS CONNECTED AS A 2nd ORDER SALLEN AND KEY LOWPASS FILTER WITH A CUTOFF FREQUENCY EQUAL TO THE MAX280. THE ADDITIONAL FILTERING ELIMINATES ANY 10kHz CLOCK FEED THROUGH PLUS DECREASES THE WIDEBAND NOISE OF THE FILTER.

DC OUTPUT OFFSET (REFERRED TO A DC GAIN OF UNITY) = 5μV Max.

WIDEBAND NOISE (REFERRED TO A DC GAIN OF UNITY) = 60μ/VRMS

OUTPUT FILTER COMPONENT VALUES

DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1μF	0.033μF
10	3.57k	32.4k	4.6k	27.4k	0.1μF	0.2μF
101	0.324	32.4k	0.31k	16.9k	0.47μF	1μF

Figure 6. 7th Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment

5th Order, Zero DC Error, Lowpass Filter

Cascading for Higher Order Filters

Two chips can be cascaded with or without intermediate buffers. Figure 7A shows a DC accurate 10th order lowpass filter. The unbuffered output of the first chip directly drives the next stage input. To minimize loading the first resistor and capacitor, the next stage R′ should be much larger. The recommended ratio of R/R′ is 117:1. The values chosen were $1/(2\pi RC) = f_C/1.57$ and $1/(2\pi R'C') = f_C/1.6$. For example, for f_C = 4.16kHz, f_{CLK} = 416kHz, R = 909Ω, R′ = 107kΩ, C = 0.066μF, C′ = 574pF. For this example the maximum passband error occurs around $0.5f_C$ and is -0.6dB. Figure 6B corrects for loading the buffered output when the first stage is used to drive the input of the next stage. This introduces a maximum DC error of 2mV over temperature using the MAX280. Now R and R′ can be similar in value and the passband gain error is reduced typically -0.15dB. The RC values used were $1/(2\pi RC) = f_C/1.59$ and $1/(2\pi R'C') = f_C/1.64$.

Creating Notch Filters

The MAX280/LTC1062 can be used to create a notch because the frequency, where it exhibits -180° phase shift, is inside its passband as shown in Figure 8A. It is repeatable and predictable from part-to-part. An input signal can be summed with the output of the filter to form a notch as shown in Figure 8B. The 180° phase shift of the MAX280/LTC1062 occurs at $f_{CLK}/118.3$ or 0.85 times the lowpass cutoff frequency. For instance, to obtain a 60Hz notch, the clock frequency should be 7.098kHz and the input ($1/2\pi RC$) should be approximately 70.98Hz/1.63. The optional (R2C2) at the output filters the clock feedthrough. The $1/2\pi R2C2$ should be 12-15 times the notch frequency. The major advantage of this notch is its wide bandwidth. The input frequency range is not limited by the clock frequency because the MAX280/LTC1062 by itself does not alias.

The circuit of Figure 8C is an extension of the previous notch filter. The input signal is summed with the lowpass filter output through A1, as previously described; then, the output of A1 is again summed with the input voltage through A2.

R6 = R2 = R3 = R7 and R4 = R5 = 0.5R7, the output of A2, at least theoretically, should look like the output of MAX280/LTC1062, the B_{OUT} pin. If the ratio of

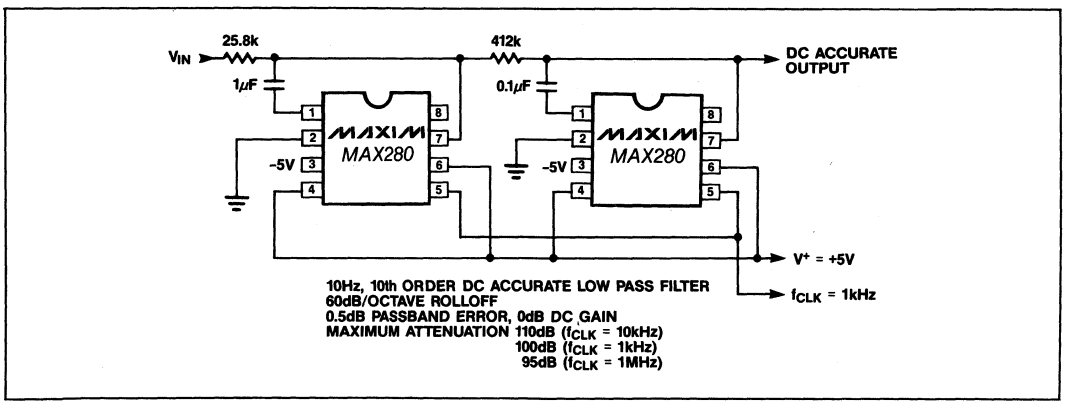


Figure 7A. Simple Cascading Technique

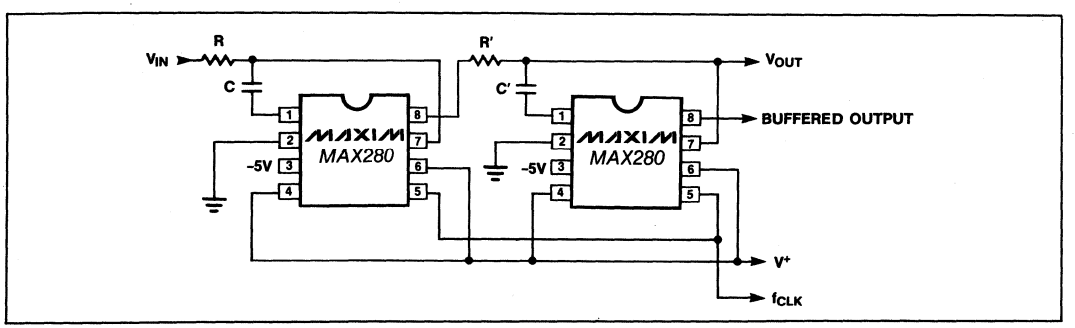


Figure 7B. Cascading Two MAX280/LTC1062s. The 2nd Stage is Driven by the Buffered Output of the First Stage.

(R6/R5) is slightly less than 2, a notch is introduced in the stopband of the filter as shown in Figure 8D. The overall filter response looks pseudoelliptic low-pass. The frequency of the notch is at $f_{CLK}/47.3$ and the value of the resistor ratio (R6/R5) should be equal to 1.935.

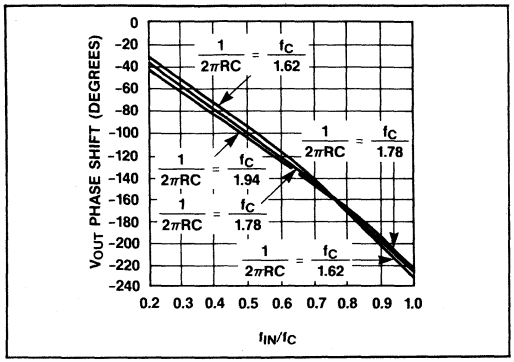


Figure 8A. Phase Response of the MAX280/LTC1062 for Various Input (R, C)s

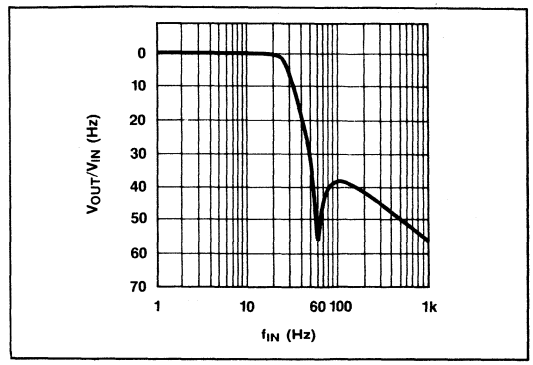


Figure 8D. Amplitude Response of the Filter

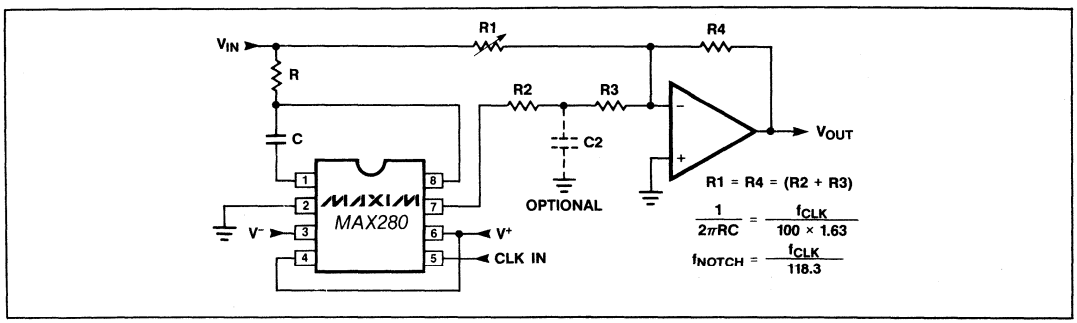


Figure 8B. Using the MAX280/LTC1062 to Create a Notch

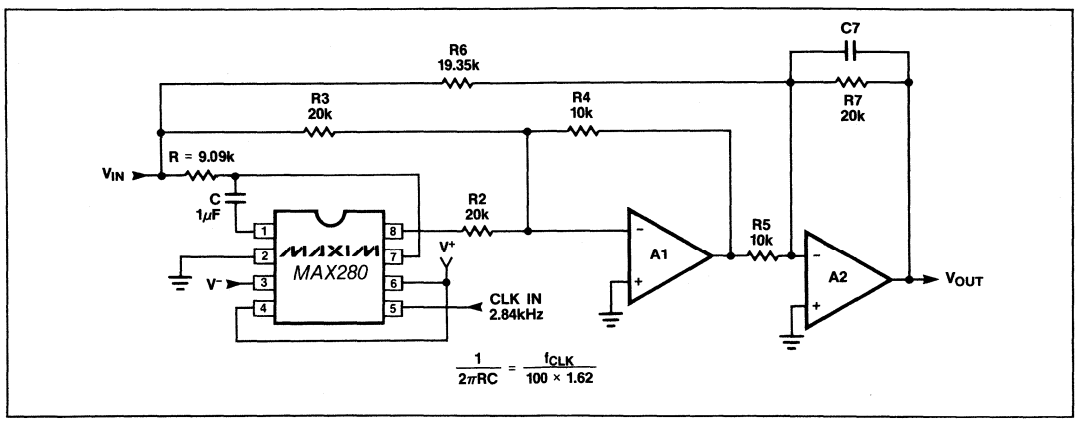
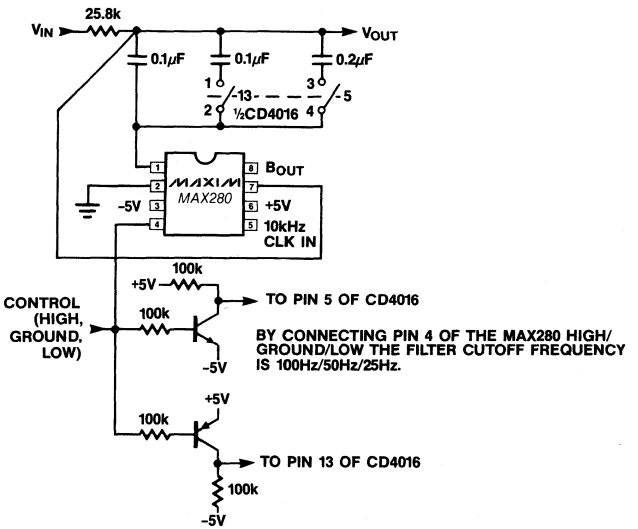


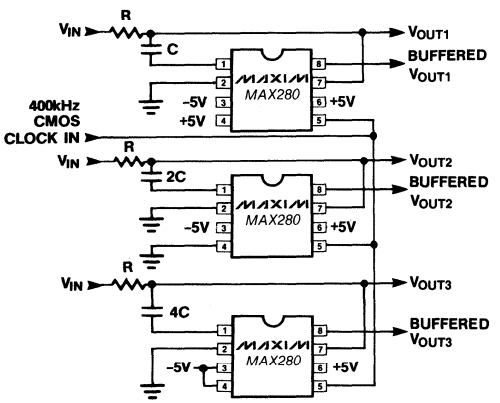
Figure 8C. A Lowpass Filter with a 60Hz Notch

5th Order, Zero DC Error, Lowpass Filter

Application Circuits

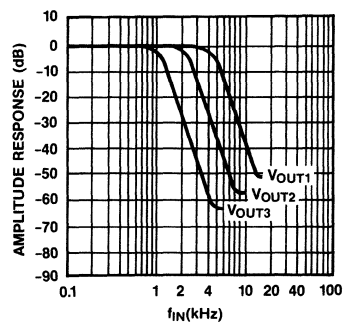


100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter



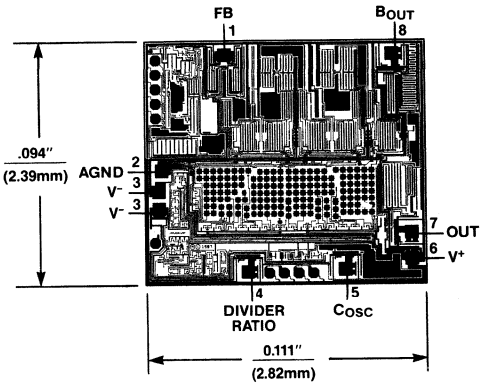
Octave Tuning with a Single Input Clock

Amplitude Response for the Octave Tuning Circuit



5th Order, Zero DC Error, Lowpass Filter

Chip Topography



MAXIM

5th-Order, Zero-Error, Bessel Lowpass Filter

General Description

The MAX281 is a 5th-order all-pole instrumentation lowpass filter with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing DC accuracy.

The external resistor and capacitor together with the on-chip 4th-order switched capacitor filter form a 5th-order Bessel lowpass filter. Bessel lowpass filters provide linear phase (constant group delay) response from DC to beyond the filter cutoff frequency, with some reduction in stopband attenuation.

The filter cutoff frequency is set by a clock which can be either internally generated or externally provided. The clock to cutoff frequency ratio of 101 allows easy removal of clock ripple.

MAX281A provides tighter specfications than the MAX281B for internal clock oscillator frequency and buffer amplifier offset voltage.

MAX280 is available for applications requiring a maximally flat (Butterworth) amplitude response.

Applications

Anti-Aliasing Filters

Data Loggers

Digital Voltmeters

Weigh Scales

Strain Gauges

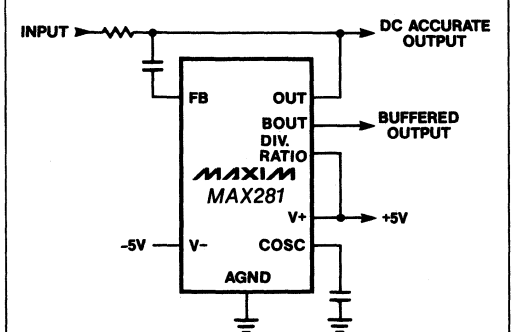
Features

- ♦ Bessel Lowpass Filter with No DC Error
- ♦ Low Passband Noise
- ♦ DC to 20kHz Cutoff Frequency
- ♦ 5th-Order All-Pole Bessel Response
- ♦ Internal or External Clock
- ♦ Cascadable for Higher Order Rolloff
- ♦ Buffered Output Available
- ♦ 8-Pin DIP or 16-Pin Wide SO Packages

Ordering Information

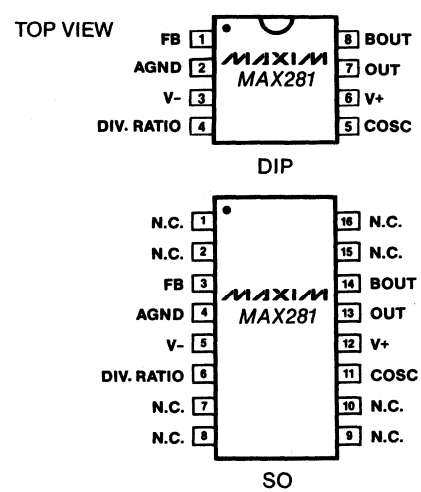
PART	TEMP. RANGE	PIN-PACKAGE
MAX281ACPA	0°C to +70°C	8 Plastic DIP
MAX281BCPA	0°C to +70°C	8 Plastic DIP
MAX281ACWE	0°C to +70°C	16 Wide SO
MAX281BCWE	0°C to +70°C	16 Wide SO
MAX281C/D	0°C to +70°C	Dice
MAX281AEPA	-40°C to +85°C	8 Plastic DIP
MAX281BEPA	-40°C to +85°C	8 Plastic DIP
MAX281AEWE	-40°C to +85°C	16 Wide SO
MAX281BEWE	-40°C to +85°C	16 Wide SO
MAX281AMJA	-55°C to +125°C	8 CERDIP
MAX281BMJA	-55°C to +125°C	8 CERDIP

Typical Operating Circuit



5TH-ORDER BESSEL LOWPASS FILTER

Pin Configurations



5th-Order, Zero-Error, Bessel Lowpass Filter

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 17V
Input Voltage at Any Pin .... V- (-0.3V) ≤ V_{IN} ≤ V+ (+0.3V)
Power Dissipation
Plastic DIP (derate at 6.25mW/°C above 70°C) ... 500mW
CERDIP (derate at 8.00mW/°C above 70°C) 640mW
SO (derate at 9.52mW/°C above 70°C) 762mW

Operating Temperature
MAX281_C___ ..... -0°C to +70°C
MAX281_E___ ..... -40°C to +85°C
MAX281_M___ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted, AC output measured at OUT pin, Figure 1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Dual Supply Single Supply			 ±2.375 4.75		 ±8 16	V
Power-Supply Current	COSC (Pin 5 to V-) = 100pF T_A = T_{MIN} to T_{MAX}			5	10	mA
Input Frequency Range				0-20		kHz
Filter Gain at f_{IN} = 0 f_{IN} = 0.5f_C (Note 1)	f_{CLK} = 100kHz Pin 4 at V+ C = 0.01µF R = 18.61kΩ	T_A = +25°C		0 -0.9	 -1.2	dB
f_{IN} = f_C f_{IN} = 2f_C f_{IN} = 4f_C		T_A = T_{MIN} to T_{MAX}	-2.5 -12 -35	-3.5 -14 -39		
Clock to Cutoff Frequency Ratio f_{CLK}/f_C	f_{CLK} = 100kHz, Pin 4 at V+ C = 0.01µF, R = 25.78kΩ			101		
Filter Gain at f_{IN} = 4fc	f_{CLK} = 400kHz, Pin 4 at V+ C = 0.01µF, R = 4.65kΩ T_A = T_{MIN} to T_{MAX}		-32	-37		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an ext op amp T_A = T_{MIN} to T_{MAX}		±3.5	±3.8		V
Clock Feedthrough				10		mV_{p-p}
INTERNAL BUFFER						
Bias Current	T_A = +25°C T_A = T_{MIN} to T_{MAX}			2 170	50 1000	pA
Offset Voltage	MAX281A MAX281B			0.2 2	2 20	mV
Voltage Swing	20kΩ; T_A = T_{MIN} to T_{MAX}		±3.5	±3.8		V
Short-Circuit Current Source/Sink				30/2		mA
CLOCK (NOTE 2)						
Internal Oscillator Frequency	COSC (Pin 5 to V-) = 100pF	MAX281A MAX281B	31 25	35 35	39 50	kHz
	T_A = T_{MIN} to T_{MAX} COSC (Pin 5 to V-) = 100pF	MAX281A MAX281B	29 15	35 35	43 65	
Max Clock Frequency				4		MHz
COSC Input Sink/Source Current	T_A = T_{MIN} to T_{MAX}			25	80	µA

Note 1: f_C is the corner frequency of the filter.
Note 2: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V+, f_{CLK}/f_C = 101; when pin 4 = GND, f_{CLK}/f_C = 202 when pin 4 = V-, f_{CLK}/f_C = 404.

5th-Order, Zero-Error, Bessel Lowpass Filter

Pin Description

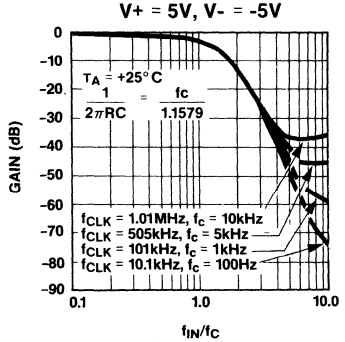
NAME	FUNCTION
FB	External capacitor couples to the chip through this pin.
AGND	Ground. Connect to system ground for dual-supply operation or mid-supply for single operation. This pin should be well bypassed using a large capacitor for single-supply operation.
V-	Negative Supply Voltage
DIVIDER RATIO	Strapped to select clock to cutoff ratio (external clock), or internal divider ratio (internal oscillator).

Voltage at pin 4	EXT fosc/fc	INT divisor
V+	101	1
GND	202	2
V-	404	4

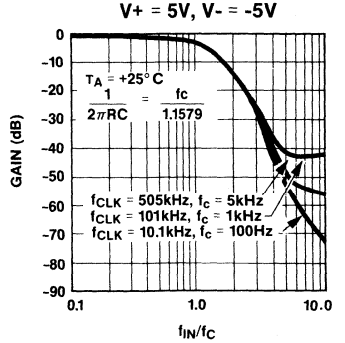
NAME	FUNCTION
COSC	Clock input pin for external clock applications. For internal clock operation, connect an external capacitor between this pin and V-.
V+	Positive Supply Voltage
OUT	Input to on-chip buffer amplifier
BOUT	Output of buffer amplifier

Typical Operating Characteristics

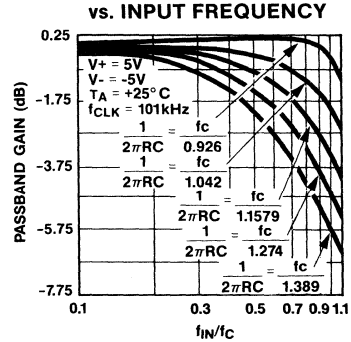
GAIN NORMALIZED TO CUTOFF FREQUENCY
V+ = 5V, V- = -5V



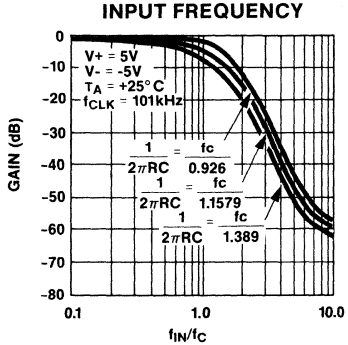
GAIN NORMALIZED TO CUTOFF FREQUENCY
V+ = 5V, V- = -5V



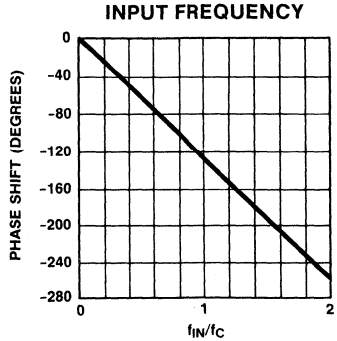
PASSBAND GAIN vs. INPUT FREQUENCY



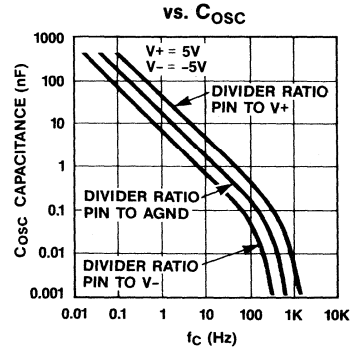
GAIN vs. INPUT FREQUENCY



PHASE SHIFT vs. INPUT FREQUENCY



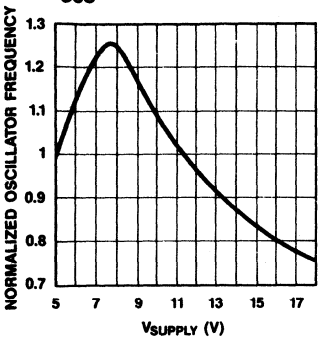
CUTOFF FREQUENCY vs. COSC



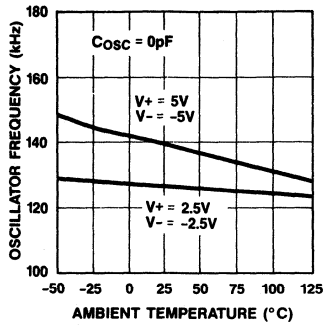
5th-Order, Zero-Error, Bessel Lowpass Filter

Typical Operating Characteristics (continued)

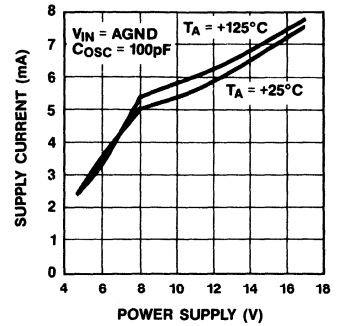
NORMALIZED OSCILLATOR FREQUENCY f_{OSC} vs. SUPPLY VOLTAGE



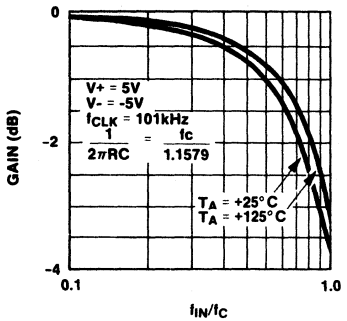
OSCILLATOR FREQUENCY f_{OSC} vs. AMBIENT TEMPERATURE



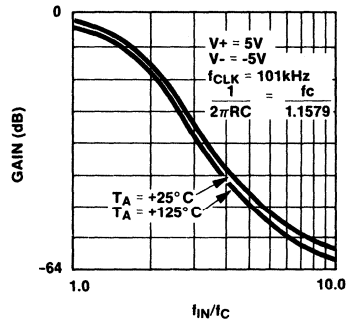
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



VARIATION OF PASSBAND GAIN WITH TEMPERATURE

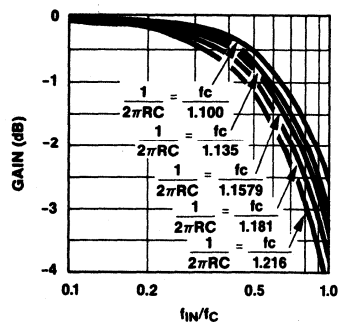


VARIATION OF GAIN WITH TEMPERATURE

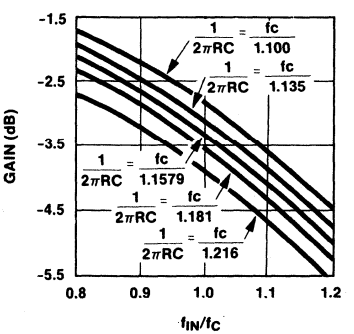


PASSBAND GAIN vs. INPUT FREQUENCY

V+ = 5V
V- = -5V
TA = +25°C
fCLK = 101kHz



GAIN vs. INPUT FREQUENCY



V+ = 5V
V- = -5V
TA = +25°C
fCLK = 101kHz

5th-Order, Zero-Error, Bessel Lowpass Filter

Introduction

Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form a 5th-order, lowpass filter. The input and output appear across an external resistor, and the IC part of the overall filter handles only the AC path of the signal. The DC offsets of the buffer and the switched-capacitor network are blocked by the capacitor and do not appear at the zero-offset output pin.

Use of this external resistor and capacitor also automatically provides the required anti-aliasing filtering for the sampled filter. Further, low-frequency noise in the filter IC is attenuated by the external capacitor since any noise at the FB pin goes through a highpass path to the filter output. The filter output pin is unbuffered. This signal can be buffered by the on-chip buffer or by a high-accuracy op amp (such as a chopper stabilized op amp) to obtain a buffered DC accurate system. The on-chip buffer has an offset voltage of 2mV for the MAX281A and 20mV for the MAX281B. The offset voltage for both devices have a typical tempco of 1µV/°C.

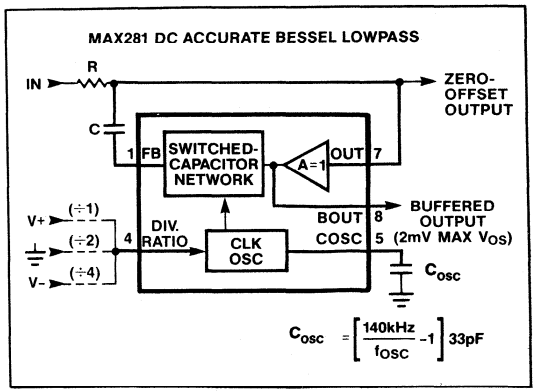


Figure 1. Block Diagram

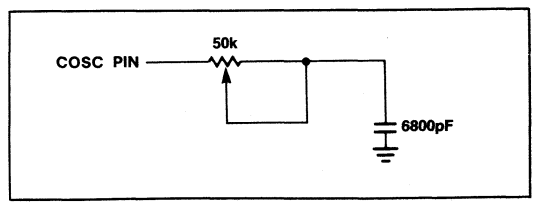


Figure 2. External Oscillator Trim

Detailed Description

Clock Requirements

The MAX281 operates either on its internal oscillator or an externally supplied clock.

Using an Internal Oscillator

The MAX281 contains an internal 140kHz (nominal) oscillator. This frequency can be modified by connecting an external capacitor in parallel with the on-chip 33pF capacitor; from the COSC pin to GND (or to V- if the capacitor is polarized).

When using the internal oscillator, connect the DIVIDER RATIO pin to V+ for 1/1, to GND for a 2/1, and to V- for a 4/1 f_{OSC}/f_{CLK} ratio.

The oscillator frequency can be calculated by:

$$f_{OSC} = 140kHz\ (33pF/(33pF+C_{OSC})\ ) \quad (1)$$

Due to process tolerances, f_{OSC} can vary by ±62.5% in the MAX281B. In the MAX281A, on-chip trimming reduces the f_{OSC} tolerance to ±19.5%. The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the COSC pin (Figure 2). The new frequency can be computed as:

$$f'_{OSC} = f_{OSC}/(1-4RC_{OSC}f_{OSC}) \quad (2)$$

where f_{OSC} is the value of the oscillator frequency when R = 0. When an external potentiometer is used, the new value of the oscillator frequency is always higher than the one calculated in (equation 1). To achieve a wide tuning range, calculate (equation 1) the ideal f_{OSC}, C_{OSC} pair, then double the value of C_{OSC} and use a 50k potentiometer to adjust f'_{OSC}. For example, to obtain a 1kHz oscillator frequency, C_{OSC} is 3900pF. By using 6800pF for C_{OSC} and a 50kΩ potentiometer, the clock frequency can be adjusted from 500Hz to 1.56kHz. The internal oscillation frequency can be measured directly at the COSC pin using a low-capacitance probe.

Using an External Clock

Depending upon the connection of the DIVIDER RATIO pin, the internal switched capacitor filter requires a clock 101, 202, or 404 times higher than the desired cutoff frequency. If an external clock is used, the input on the COSC pin must swing close to the power rails (V+,V-). Although standard 74HC00 series CMOS gates do not guarantee CMOS levels with the source and sink currents of the COSC pin, they will in reality drive the COSC pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and current to simultaneously drive several chips. The typical trip levels of the internal Schmitt trigger sensing COSC pin are:

POWER SUPPLY		TRIP LEVEL	
V+ = +2.5V	V- = -2.5V	V_{IH} = 0.9V	V_{IL} = -1.15V
V+ = +5V	V- = -5V	V_{IH} = 1.4V	V_{IL} = -2.1V
V+ = +6V	V- = -6V	V_{IH} = 1.7V	V_{IL} = -2.5V
V+ = +5V	V- = 0V	V_{IH} = 3.4V	V_{IL} = 1.35V
V+ = +10V	V- = 0V	V_{IH} = 6.4V	V_{IL} = 2.9V
V+ = +15V	V- = 0V	V_{IH} = 9.5V	V_{IL} = 4.1V

5th-Order, Zero-Error, Bessel Lowpass Filter

Choosing External Resistor and Capacitor Values

The external resistor and capacitor are used as part of a feedback loop for the filter and also forms one pole. The internal 4-pole switched-capacitor filter is driven by a clock which also determines the filter cutoff frequency. For a proper Bessel response, the clock and DIVIDER RATIO pin should be set to provide the desired cutoff frequency. Additionally, the resistor and capacitor should be chosen such that:

$$\frac{f_C}{1.1579} = \frac{1}{2\pi RC}$$

where f_C = filter cutoff frequency.

For example to implement a 10Hz cutoff filter, set:

$$1/2\pi RC = 10Hz/1.1579 = 8.6363Hz$$

R is typically ≈ 20kΩ. The minimum value of R depends upon the maximum input signal, and the current sinking capability of the FB pin (typically 1mA). So for a $1V_{p-p}$ signal, the minimum value of the resistor is 1kΩ.

The passband response for values of $1/(2\pi RC)$ around $(f_C/1.1579)$ can be seen on the Passband Gain vs. Input Frequency plots (see Typical Operating Characteristics). For optimum Bessel response, the RC product should be well controlled. Note that an inaccurate RC product can cause excessive peaking at the FB pin (Figure 3), which results in clipping and distortion of the output waveform.

For wide temperature range applications, NPO ceramic capacitors are recommended. Their tempcos are around ±20ppm and values are available to 0.1μF. Other ceramic capacitors are not recommended due to their large tempcos. Mylar, polystyrene and polypropylene capacitors all provide acceptable performance. Solid tantalum capacitors connected back-to-back and disc ceramic capacitors introduce additional passband errors (0.05-0.1dB).

Applications Information

Filter Input Voltage Range

Every node of the filter typically swings within 1V of both supplies. With the appropriate external resistor and capacitor values, the amplitude response of all the internal and external nodes should not exceed a gain of 0dB with the exception of the FB pin. The amplitude response of the FB pin, where some peaking may occur, is shown in Figure 3.

With ±5V supplies, the peak-to-peak input voltage should not exceed 6.5V. If the input voltage goes beyond this value, clipping and distortion of the output waveform may occur; however, the filter will not be damaged. The absolute maximum input voltage to any pin should not exceed the power supplies.

Internal Buffer

The internal output buffer of the FB pin and the OUT pin is part of the AC signal path. Hence, capacitive loading greater than 30pF can cause gain errors in the passband around the cutoff frequency. The internal buffer can also be used as the filter output, however, there will be a few millivolts of output offset.

Filter Attenuation

The rolloff is 30dB/octave. When the clock rate is increased and hence the cutoff frequency is increased, the filter's maximum attenuation decreases as shown in the Typical Operating Characteristics. This decrease is caused by rolloff at higher frequencies of the loop gains of the various internal feedback paths and is not due to any increase in noise floor.

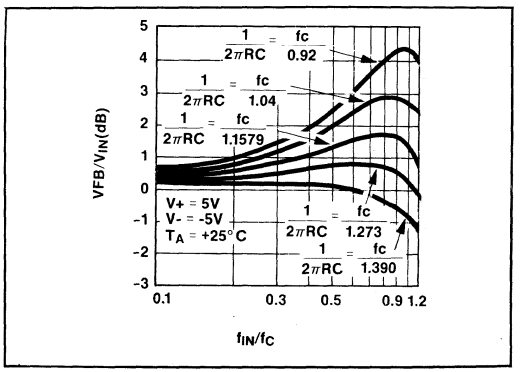


Figure 3. Amplitude Response of FB Pin

Filter Noise

The filter wideband noise is typically $90\mu V_{RMS}$ with ±5V supplies and typically $80\mu V_{RMS}$ for ±2.5V supplies or a +5V single supply. This value is nearly independent of the cutoff frequency. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below $0.1f_C$. Roughly 2/3 of the entire wideband noise is in the band DC to f_C.

Transient Response

Figure 4 shows the step response of the filter where f_C = 1kHz. This response approximates an ideal 5th-order Bessel filter. The absence of overshoot is characteristic of the Bessel response.

Anti-Aliasing

The internal 4th-order switched-capacitor filter is a sampled device, and as such will alias unless preceded by a band limited signal or a continuous non-sampled filter. The external resistor and capacitor used to form the 5th filter pole also automatically provides this function. Attenuation is greater than 35dB at the Nyquist frequency.

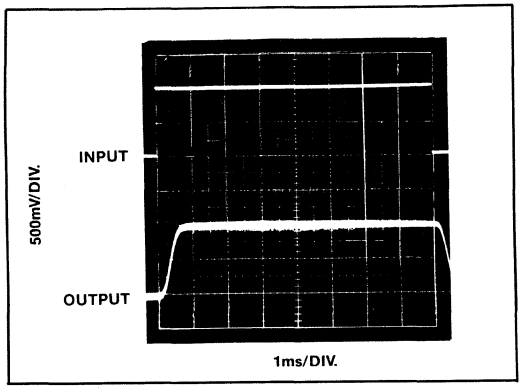


Figure 4. Step Response of MAX281 for f_C = 1kHz

Single-Supply Operation

Figure 5A shows a schematic for single-supply operation. The AGND pin and the OUT pin should be biased at 1/2 supply. The value of the resistors, R1 and R2, should be chosen to conduct 100μA or more. R' DC biases the buffer and C' isolates the buffer from the DC value of the output. Under these conditions, the external resistor and capacitor should be adjusted such that (1/2πRC) = 1.2737. This accounts for the extra loading of the R',C' combination. R' and C' are not required if the input voltage has a DC value around 1/2 supply. If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground. The AGND pin should also be bypassed by a decoupling capacitor.

Figures 5B and 5C illustrate the passband and stopband frequency response for both single- and dual-supply operation.

Clock Feedthrough

Clock feedthrough can be reduced by using a resistor and capacitor at the buffered output pin provided that this pin is used as an output. An active filter at the DC accurate output can act as a buffer and provide clock feedthrough filtering.

Cascading for Higher Order Filters

Two chips can be cascaded with or without intermediate buffers. Figure 6 shows a buffered arrangement which corrects for loading of the output when the first stage is used to drive the input of the next stage. This introduces a maximum DC error of 2mV over temperature at VOUT.

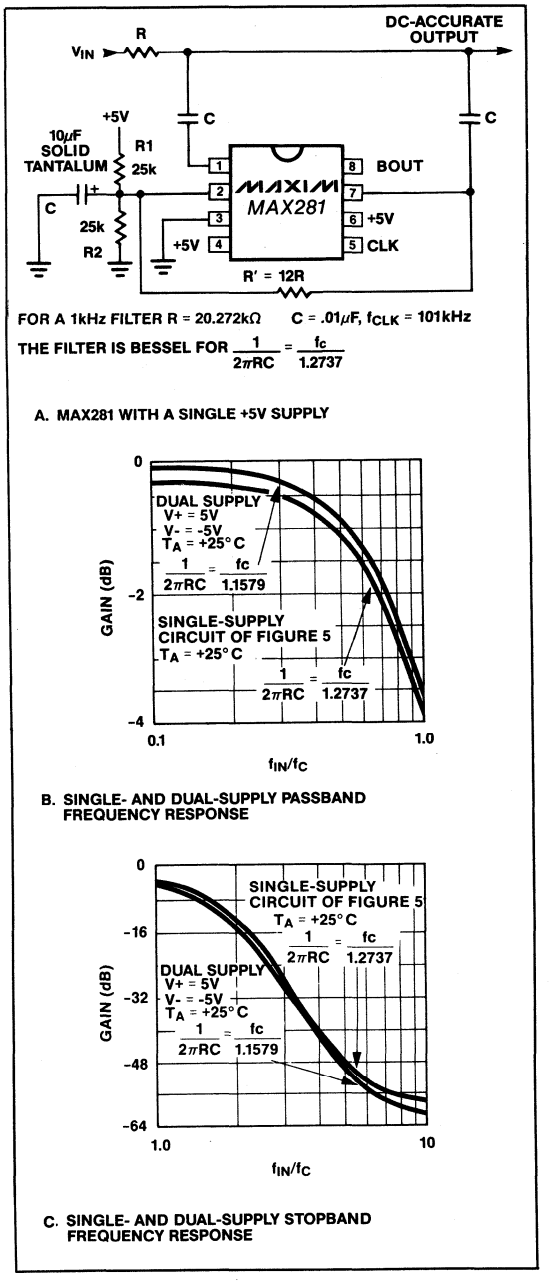


Figure 5. Operation from a Single +5V Supply

5th-Order, Zero-Error, Bessel Lowpass Filter

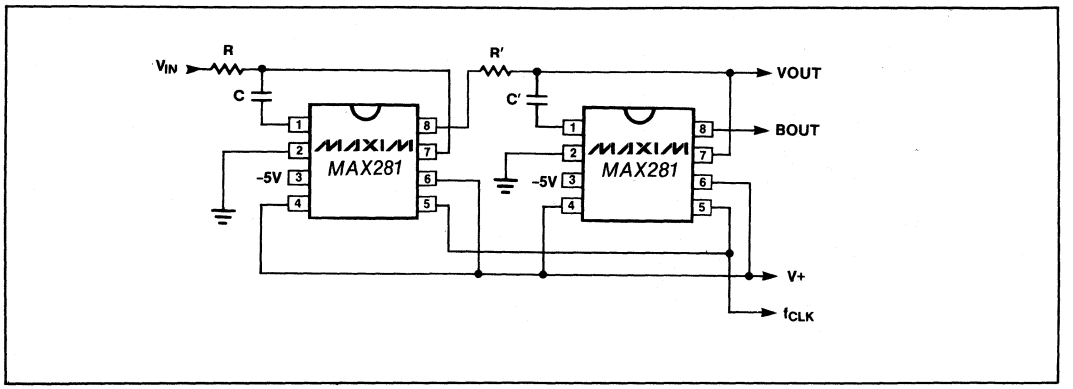


Figure 6. Cascading Two MAX281 filters. The 2nd Stage is Driven by the Buffered Output of the First Stage

Application Circuits

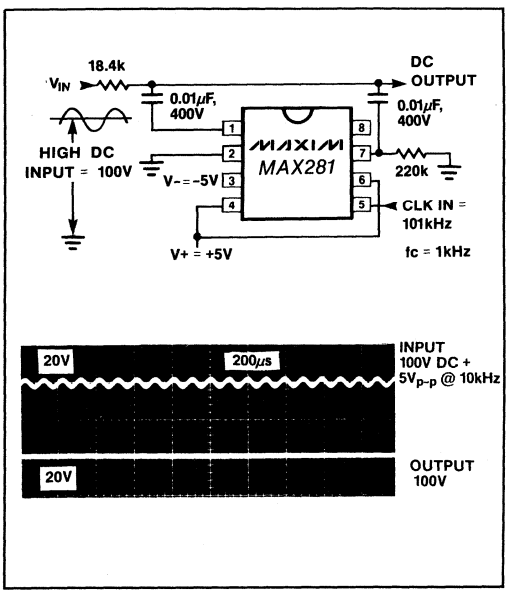
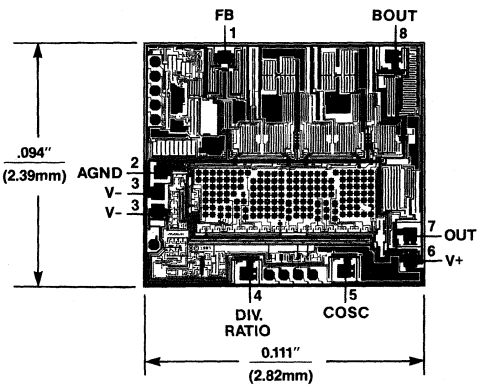


Figure 7. Filtering AC Signals from High DC Voltages

Filtering High DC Voltages

In Figure 7, a MAX281 removes undesired AC components from a DC voltage much higher than the operating voltage of the filter IC. This is possible due to the shunt architecture of these filters and is not generally possible with conventional active filter structures.

Chip Topography



ADVANCE INFORMATION
First Page of Data Sheet in Preparation

MAXIM

8th-Order, Clock-Tunable Lowpass Filters

General Description

The MAX291-MAX297 are a family of 8th-order lowpass filters. The filter responses are fixed Butterworth, Bessel, or elliptic, with corner frequencies that are set over a 0.1Hz to 50kHz range by adjusting the clock rate.

The Bessel filter is suited for low overshoot applications, while the Butterworth offers minimum passband amplitude ripple. Elliptic filters provide the steepest gain rolloff of the three types at the expense of passband ripple. The MAX292 features a typical spurious-free dynamic range of 72dB at 1kHz, making it ideal for dynamic applications such as analog-to-digital converter anti-aliasing and digital-to-analog converter output filtering.

Filters with either 100:1 or 50:1 clock-to-corner frequency ratios are available. 100:1 is recommended for corner frequencies up to 25kHz. Between 25kHz and 50kHz, the 50:1 ratio filters are recommended.

The MAX291-MAX297 operate with either an internal or external clock. The internal clock frequency is set by a single external capacitor. An uncommitted op amp (noninverting input grounded) is supplied to build a continuous-time lowpass filter for post-filtering or anti-aliasing.

Applications

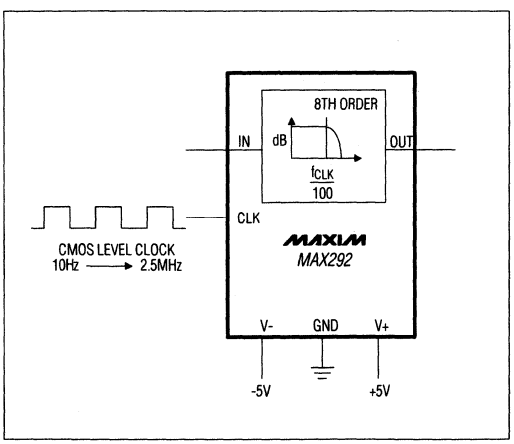
Anti-Aliasing Filters

DAC Post-Filtering

50Hz/60Hz Line-Noise Filtering

Noise Analysis

Functional Diagram



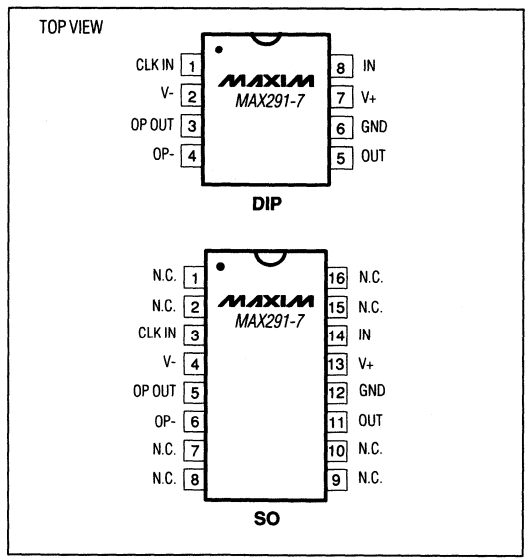
Features

- ♦ **Clock-Tunable Corner Frequency**
- ♦ **0.1Hz to 50kHz Corner-Frequency Range**
- ♦ **Cascadable for Higher-Order Rolloff**
- ♦ **Low Distortion - SFDR 72dB at 1kHz Typ**
- ♦ **Internal or External Clock**
- ♦ **Operate from Single +5V Supply or ±5V Supplies**
- ♦ **8-Pin DIP/16-Pin SO Packages**

Selection Table

PART	RESPONSE SHAPE	CLOCK: CORNER-FREQUENCY RATIO
MAX291	Butterwoth	100:1
MAX292	Bessel	100:1
MAX293	Elliptic (1.5 transition ratio)	100:1
MAX294	Elliptic (1.5 transition ratio)	100:1
MAX295	Butterworth	50:1
MAX296	Bessel	50:1
MAX297	Elliptic (1.5 transition ratio)	50:1

Pin Configurations



6

MAXIM

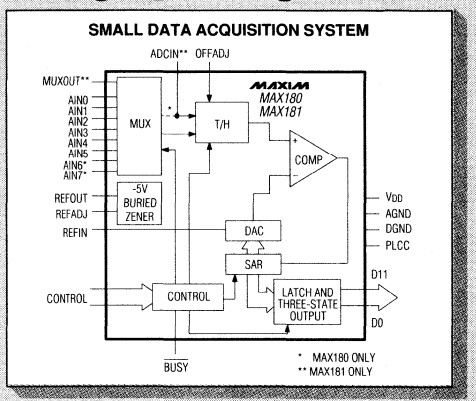
A/D Converters

Self-Contained 8-Ch 12-Bit System Simplifies "Analog In-to-Data Out"

Each 100kHz (10µs) Channel is µP Configurable for Differential/ Single-Ended and Unipolar/Bipolar Analog Input Ranges

You can now avoid interface problems like ground loops, noise coupling, voltage drops, and stray capacitances. Maxim's new MAX180 complete data-acquisition system contains all necessary analog and digital functions: 8-channel analog multiplexer, a wide-bandwidth track/hold, a 25ppm/°C voltage reference, and a 7.5µs A/D with a fast, parallel 8- or 16-bit microprocessor interface. The entire system fits in one standard 40-pin DIP or 44-pin PLCC package, and is fully tested and guaranteed for both DC and dynamic applications. In a typical system, Maxim's monolithic CMOS design reduces power consumption (110mW), component count, cost and significantly minimizes board space and design time.

For applications requiring a programmable-gain amplifier or a filter to follow the mux, Maxim's 6-channel MAX181 gives access to the mux output, which otherwise works the same as the MAX180.

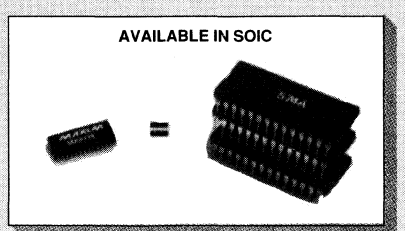


The MAX180/181 contain on-chip all necessary analog functions-including a low-drift, low-noise voltage reference.

New BiCMOS Design Makes a Better 574A : 8µs Fast & 3X Lower Power

MAX174 Drops-In 574A and 674A Applications, Improving Performance with No Design Effort

The new MAX174 provides a complete 12-bit A/D with 10ppm/°C voltage reference, a laser-trimmed internal clock, and +10V, +20V, ±10V and ±5V input ranges in the industry-standard 574A/674A pinout. Unlike older designs, Maxim's use of BiCMOS technology allows increasing speed from 25µs to 8µs while reducing power consumption from 450mW to 150mW. And Maxim supplies the MAX174 in the 0°C to +70°C and -40°C to +85°C temperature ranges in both DIP and space-saving SO packages for new designs. Maxim also has the 25µs MX574A and the 15µs MX674A for existing designs.



Three interleaved industry-standard 574As would be required to match the speed of a single low-power MAX174. And, in SO, it saves significant board area.

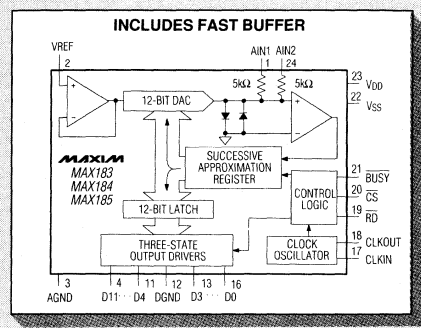
7

World's First 3µs 12-Bit A/D at $15*!

Simplify Design Effort with Flexible +5V, +10V, or ±5V Input Ranges and an Internal Ref Buffer

For applications demanding blazing speed without high cost, Maxim offers the MAX183 - the lowest-cost 3µs, 12-bit A/D ever. Designed with a proprietary BiCMOS process, the MAX183 provides high speed and low code-edge noise, while keeping power consumption at 90mW. Laser-trimmed resistors guarantee 12-bit, 1/2 LSB linearity and "no missing codes" performance from 0°C/+70°C to -55°C/+125°C temperature ranges. For slower and lower-cost applications, Maxim provides the MAX184 with 5µs and the MAX185 with 10µs conversion times, which are otherwise identical to the MAX183. All three parts support fast, parallel µP interfaces and are available in small-footprint 24-pin DIPs and SOs.

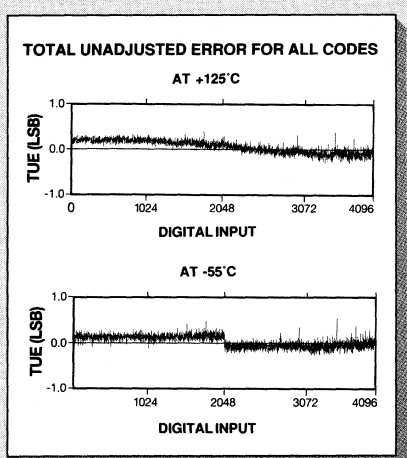
* 1000pc FOB USA, suggested resale price.



MAX183/4/5 have an on-chip high-performance voltage reference buffer that simplifies design efforts and saves cost.

Calibrated 12-Bit A/Ds Need No Adjustments to Maintain ±1 LSB Accuracy from -55°C to +125°C!

4- & 1-Ch A/Ds are Complete with T/H and 40ppm/°C Ref



With no gain, offset, or linearity adjustments, the total MAX178 error stays below ±1LSB from -55°C to +125°C for all codes.

Even the best trim pots drift over time and temperature, requiring costly calibration procedures. Maxim's MAX178 and MAX182 are automatically corrected at every conversion, eliminating adjustments and holding total error below ±1 LSB without trim pots. And these A/Ds include an internal T/H and DC and dynamic specifications for applications ranging from industrial control to signal processing, that demand minimal component count and stability over time and temperature.

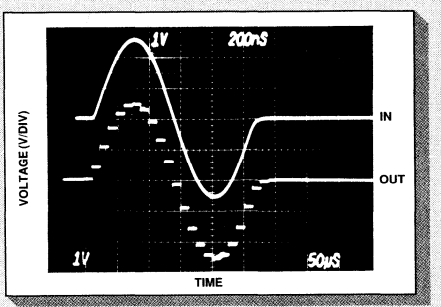
Both new A/Ds also include an internal 40ppm/°C voltage reference, an 8- or 16-bit µP interface, and an optional internal or external clock. For designs requiring conversion of multiple analog signals, the MAX182 combines a 4-channel analog mux with all the features of the single-input MAX178. The high-resistance analog inputs (500MΩ) permit driving the A/Ds with lower-cost, standard op amps.

If you are presently using a 7578 or 7582, Maxim's MAX178 and MAX182 upgrade existing designs pin-for-pin, reducing conversion time from 100µs to 60µs while eliminating external sample-and-hold, voltage reference, and *all* clock components at no additional cost!

100kHz 12-Bit Sampling A/Ds Have 6MHz T/H, DC and Dynamic Specs

+5V, ±5V, or ±2.5V High-Resistance Analog Inputs are Easy-to-Drive with Standard Lower-Cost Op Amps

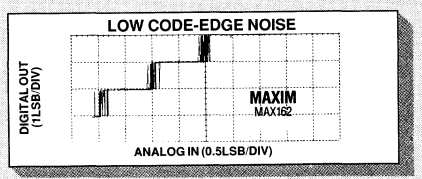
Maxim's MAX163/164/167 combine a 1µs acquisition-time T/H with a 7.8µs A/D on one CMOS circuit. The new A/Ds are plug-in replacements, with an on-chip T/H, for the AD7572, MAX162, and MAX172. Unlike other circuits, Maxim's proprietary sampling comparator used for these A/Ds doubles as a T/H and works with a very small, internal sampling capacitor. This results in a wide full-power sampling bandwidth (6MHz typ), low distortion (-80dB max), and a high analog input resistance (500MΩ). A 25ppm/°C internal voltage reference and three analog input ranges are provided for designs with +5V (MAX163), ±5V (MAX164), or ±2.5V (MAX167) signal ranges.



MAX167 has a high-bandwidth T/H, good enough to digitize a 1MHz sine wave using the undersampling technique.

3µs 12-Bit A/D with 25ppm/°C Ref Replaces Expensive Hybrids

Small 24-Pin DIP and SO Packages Save Space, Cost



MAX162 full-scale and zero-scale noises are better than most comparable devices, and are <1/8LSB.

Whether you want to replace a costly and bulky hybrid, or want a self-contained single-channel A/D, the MAX162 can significantly lower system cost and improve performance. The MAX162 has a 3µs A/D, an internal 25ppm/°C or 45ppm/°C voltage reference, an 8- or 16-bit µP interface, and an optional internal/external clock. The voltage reference uses a stable buried-zener diode, thin-film resistors, and high-quality amplifiers for optimum low-drift and low-noise performance for fast data-acquisition applications.

7

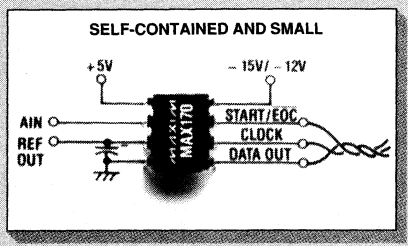
Complete 12-Bit 10µs A/D for $10!

MAX172 Includes an Internal 45ppm/°C Voltage Reference, and Plug-In Upgrades 12µs 7572s

For high-performance applications, the MAX172 provides an easy-to-use and low-cost alternative to earlier designs, such as the 574A. Maxim's A/D requires only a few external bypass capacitors to work in most 8- or 16-bit µP systems. Available in 24-pin SO and 0.3" DIPs in 0°C/+70°C to -55°C/+125°C temperature ranges, the MAX172 challenges all other A/Ds in price and performance - with 90ns access time, 215mW max power consumption, and "no missing codes" 12-bit linearity.

Un-Paralleled Converter: First 5.6µs 12-Bit A/D to Fit in 8-Pin MiniDIP!

The 3-Wire Serial-Interface A/D Saves Over 10 Traces on a Circuit Board - Fits Tight Spaces



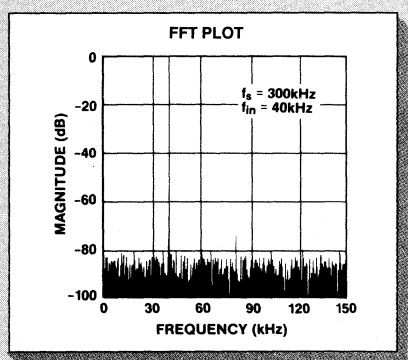
MAX170 needs only 3 wires to interface to a µP and saves space in small-footprint 8-pin DIP or 16-pin SOs.

Serial digital communication is preferred to parallel when long distances are involved. Digital interface provides better noise immunity from motors, heaters, and other industrial equipment compared to analog. Maxim's MAX170, with 3-wire interface, simplifies sending A/D outputs over long distances. And for breaking ground-loops, the 3-wire interface is easier and costs less to transformer- or opto-isolate than the 10 to 14 wires required for a 12-bit parallel interface. MAX170 is functionally complete for most "analog in/digital out" applications, including an internal 40ppm/°C voltage reference for additional board-space savings and design convenience.

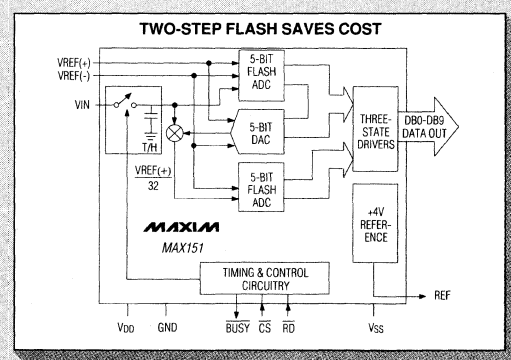
300kHz Samping 10-Bit A/D is Complete with 60ppm/°C Reference

±1LSB Accurate from -55°C to +125°C, DC and Dynamic Specified A/D Upgrades 8-Bit Designs

Maxim's MAX151 uses a proprietary half-flash technique to achieve "no missing codes" linearity and 1.9µs conversion time, while keeping power-consumption below 275mW - including the supply current of an internal voltage reference. Since the MAX151 internally tracks and holds the analog input signal, it eliminates the need for an external T/H when digitizing high-speed AC signals. For next generation designs that require better than 8-bits accuracy, the MAX151 offers an alternative to costlier high-speed 12-bit A/Ds, and is available in small-footprint 24-pin DIPs and SOs. MAX151 interfaces directly to most popular µPs by appearing as a memory location or input/output port.



MAX151 is 100% tested for DC and dynamic specifications and fits fast data-acquisition or DSP applications.



MAX151 uses a 2-step flash architecture. This minimizes the circuit complexity and saves cost while maintaining high performance.

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA) max (typ)	References	Comments	Price† 1000-up ($)
MAX130	3 1/2	±2000	LCD	+4.5 to 14	0.25 (0.1)	Bandgap	Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to 14	0.1 (0.06)	Bandgap	Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15 (0.06)	Bandgap	Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to 7	0.8 (0.2)	Bandgap	± inputs with single supply	6.88
ICL7106	3 1/2	±2000	LCD	+9	1.8 (0.6)	Zener	For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8 (0.8)	Zener	ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1 (0.6)	Zener	Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1 (0.06)	Zener	Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8 (0.2)	Bandgap	± inputs with single supply	6.08
MAX140	3 1/2	±2000	LED	+5	0.8 (0.2)	Bandgap	Low-segment current (2mA)	4.68
ICL7107	3 1/2	±2000	LED	+9	1.8 (0.6)	Zener	For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8 (0.8)	Zener	ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2 (0.06)	Zener	Low power when LED is off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2 (0.09)	External	20 conv/sec, ±10µV resolution	10.89
MAX134	3 3/4	±40,000	µP	±5	0.2 (0.09)	External	20 conv/sec, ±10µV resolution	10.89
ICL7109	12 bits + Sign	±4096	8/16 bit µP/UART	±5	1.5 (0.7)	Zener	3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4 (1.0)	External	Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2.0 (1.0)	External	For DMM, DPM, data loggers	5.48
MAX135	15 bits + Sign	±20,000	µP/8	±5	0.125	External	3-state two's complement outputs	††

1 E - external reference; I - internal reference.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products- contact factory for pricing and availability.

General-Purpose A/D Converters

Part Number	Resolution (bits)	Conversion Time (µs) max	Input Channels	Sample Rate (kHz) max	Reference Voltage (E / I [1]) (V)	Data-Bus Interface (bits)	Supply Voltages (V)	Input Ranges (V)	Comments	Price† 1000-up ($)
MAX153	8	0.400	1	2000	E	µP/8	+5 & ±5	+5V, ±2.5	High-speed with T/H	††
MX7821	8	0.660	1	1000	E	µP/8	+5 & ±5	+5V, ±2.5	With T/H	7.54
MAX150	8	1.34	1	500	E/I/+2.5	µP/8	+5	+5	With T/H and ref	7.96
MX7820	8	1.34	1	500	E	µP/8	+5	+5	Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5	With T/H	7.16
MAX154	8	2	4	300	E/I/+2.5	µP/8	+5	+5	4-ch with T/H and ref	8.36
MAX158	8	2	8	300	E/I/+2.5	µP/8	+5	+5	8-ch with T/H and ref	8.76
MX7824	8	2	4	300	E	µP/8	+5	+5	Plug-in replacement for AD7824	8.33
MX7828	8	2	8	300	E	µP/8	+5	+5	Plug-in replacement for AD7828	8.73
MAX155	8	3	8	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	8-ch simultaneous T/H and ref	††
MAX156	8	3	4	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	4-ch simultaneous T/H and ref	††
MAX160	8	4	1	-	E	µP/8	+5	+10, ±5	Ratiometric, single-supply	7.20
MAX165	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Sampling with ref	††
MAX166	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Differential input	4.91
MX7575	8	5	1	200	E/+1.23	µP/8	+5	+5	Plug-in replacement for AD7575	4.39
MX7576	8	10	1	-	E/+1.23	µP/8	+5	+5	Plug-in replacement for AD7576	3.78
MX7574	8	15	1	-	E	µP/8	+5	+10, ±5	Plug-in replacement for AD7574	4.80
MAX161	8	20	8	-	E	µP/8	+5	+10	8-ch with RAM buffer	11.12
MX7581	8	66.6	8	-	E	µP/8	+5	+10	Plug-in replacement for AD7581	11.08
MAX151	10	2.5	1	300	E/I/+4.0	µP/10	±5	+5	Sampling with reference	12.67
MAX173	10	5	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	Reference	7.01
MAX177	10	8.33	1	100	I/-5.25	µP/8/12	+5 & -12/-15	±2.5	Sampling with reference	7.96
MAX120	12	1.5	1	500	E/I/-5	µP/12	+5 & -12/-15	±5	With T/H	††
MX578	12	3	1	-	E/I/+10.0	Logic	+5 & ±15	±10	With parallel/serial outputs	88.71
MAX162	12	3.25	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	High-speed with internal ref	34.88
MAX183	12	3.25	1	-	E	µP/8/12	+5 & -12/-15	+5, ±5, +10	High-speed with external ref	15.00

1 E - external reference; I - internal reference.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products- contact factory for pricing and availability.

General-Purpose A/D Converters (continued)

Part Number	Resolution (bits)	Conversion Time (µs) max	Input Channels	Sample Rate (kHz) max	Reference Voltage (E / I[1]) (V)	Data-Bus Interface (bits)	Supply Voltages (V)	Input Ranges (V)	Comments	Price† 1000-up ($)
MX7672-03	12	3.25	1	-	E	µP/8/12	+5 &-12	+5, ±5, +10	Plug-in replacement for AD7672-03	57.38
MAX170	12	5	1	-	I/-5.25	Serial/12	+5 & -12/-15	+5	8-pin Mini DIP	11.96
MAX171	12	5	1	-	I/-5.25	Serial/12	+5 & -12/-15	+5	Opto-isolated	††
MAX184	12	5	1	-	E	µP/8/12	+5 & -12/-15	+5, ±5, +10	High-speed with external ref	13.75
MX7572-05	12	5	1	-	I/-5.25	µP/8/12	+5 & -15	+5	Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	-	E	µP/8/12	+5 & -12	+5, ±5, +10	Plug-in replacement for AD7672-05	33.66
MAX190	12	7.8	1	100	E/I/+4.096	µP/12/Serial	+5 & ±5	+5	Complete sampling with ref	††
MAX163	12	8.13	1	100	I/-5.0	µP/8/12	+5 & -12/-15	+5	Complete sampling with ref	17.00
MAX164	12	8.13	1	100	I--5.0	µP/8/12	+5 & -12/-15	±5	Complete sampling with ref	17.00
MAX167	12	8.13	1	100	I/-5.0	µP/8/12	+5 & -12/-15	±2.5	Complete sampling with ref	17.00
MAX174	12	8	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Upgrades for AD574A/AD674A	28.13
MAX180	12	8.125	8	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX181	12	8.125	6	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX172	12	10	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	First lowest-cost complete A/D	9.60
MAX185	12	10.4	1	-	E	µP/8/12	+5 & -12/-15	+5, ±5, +10	High-speed with external ref	12.00
MX7672-10	12	10.4	1	-	E	µP/8/12	+5 & -12	+5, ±5, +10	Plug-in replacement for AD7672-05	25.25
MX7572-12	12	12	1	-	I/-5.25	µP/8/12	+5 & -15	+5	Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Plug-in replacement for AD574A	23.44
MX574A	12	25	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Plug-in replacement for AD674A	11.97
MAX178	12	50	1	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	15.24
MAX182	12	50	4	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	17.55
MX7578	12	100	1	-	E	µP/8/16	+5 & +15 & -5	+5	Plug-in replacement for AD7578	16.96
MX7582	12	100	4	-	E	µP/8/16	+5 & +15 & -5	+5	Plug -in replacement for AD7582	19.50
MAX121	14	1.5	1	500	E/I/-5	µP/Serial	5 & -12/-15	±5	With ref	††
MAX168	14	3.5	1	250	E/I/+3	µP/8/Serial	±5	±3	Complete sampling with ref	††

1 E - external reference; I - internal reference.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products- contact factory for pricing and availability.

Don't Guess About A/D Converter Needs

This application note discusses characteristics that affect key A/D converter selection decisions and performance. It is not quite a general tutorial in that some important fine points are substituted for broader issues. (For a general A/D D/A primer, refer to Maxim's 1990 Applications Handbook, page 3-3). Subjects include input sampling, signal multiplexing, accuracy, noise problems, and other topics. If, after reading this, you have further questions about A/D converter (or other) applications, please feel free to contact Maxim's applications group at (408) 737-7600 extention 4000.

Resolution, Accuracy, Etc.

"Resolution" defines the smallest increment of signal amplitude an A/D can discern. A/D resolution differs from "accuracy," which is the absolute error incurred when measuring a signal. The different purposes of these specs are often clouded when A/Ds are specified; the fact that the specs sometimes have equal magnitude in A/Ds adds to the confusion. But in many other devices accuracy does not match resolution, so the value of both cases is worth examining.

A low-cost, 12-bit, 10µs A/D such as the MAX172 resolves a 5V full-scale input range to 5V/4096, or 1.2mV (1LSB), but is not accurate to this level. The untrimmed full-scale error limit of the "B grade" device is 15LSBs, while the offset limit is 6LSBs. These guarantees allow reduced cost without sacrificing linearity, which is guaranteed at 1/2 or 1LSB (A or B grade). 12-bit linearity is maintained (even on the lowest grade), because very few applications tolerate missing codes (see *Demystifying Linearity*), even when absolute accuracy is not needed. The A/D's unadjusted full-scale and offset errors are often moot. This is because they are constant, and errors in other parts of the signal path are frequently trimmed.

A/D accuracy and offset specs do not need 12-bit precision when:

1) measuring transducers or sensors that don't have precise accuracy specs (the MAX172B's 15LSB full-scale error = 0.37%),
2) only signal *changes* are of interest, not absolute voltage levels,
3) system calibration occurs elsewhere, either with manual trims or via a microprocessor or controller,
4) the A/D operates in a closed-loop control system where gain and offset errors only affect loop dynamics and not accuracy.

Untrimmed accuracy may still be worthwhile in high-resolution A/Ds if it eliminates adjustments. To effectively accomplish this, converter accuracies of 1LSB or better are needed, otherwise trims are not eliminated but only reduced in range. The MAX178 and MAX182 (with 4 input channels) reduce unadjusted total conversion error to ±1LSB over temperature with internal autocorrection circuitry.

Demystifying Linearity

A/D linearity has two common definitions, which can generate different specs for the same device and confuse comparisons between parts. This disparity is due to different A/D testing approaches. When comparing linearity specs, it pays to be familiar with both the "best-straight-line" testing approach and "endpoint" curve fitting (Figure 1).

The best-straight-line approach makes no claim about zero error, full-scale error, or transfer-function slope. It simply quantifies (in LSBs or percent) deviation from the straight line that best approximates the transfer

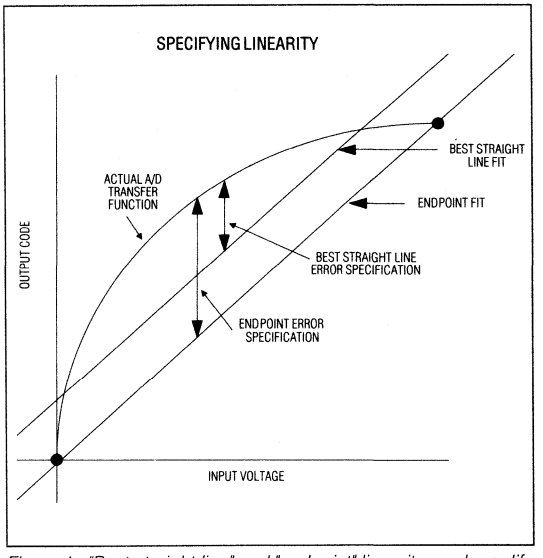


Figure 1. "Best-straight-line" and "endpoint" linearity produce different specifications for the same A/D.

Don't Guess About A/D Converter Needs

A/D PART NO.	RESOLUTION (BITS)	REF (%) TOLERANCE	REF VOLTAGE	REF DRIFT (ppm/°C) Typ	Max
MAX150/4/8	8	1.2	2.5	40	70
MAX165/6	8	1.63	1.23	40	70
MAX151	10	0.75	4.00	—	60
MAX173	10	0.95	-5.25	40	—
MAX177	10	0.4	-5.00	—	45
MAX162	12	0.95	-5.25	20	—
MAX163/4/7	12	0.4	-5.00	—	25
MAX170	12	0.95	-5.25	20	—
MAX171	12	0.95	-5.25	—	40
MAX172	12	0.95	-5.25	40	—
MAX174	12	0.2	10.00	—	—
MAX178/182	12	0.3	5.00	10	40
MAX180/181	12	0.4	-5.00	—	25

TABLE 1: A/D Converters With Internal References

function (and provides the lowest, i.e. "best looking", number). No points on this ideal line are defined before the test. The result is a pure linearity spec that includes no other errors.

Endpoint fit, on the other hand, presets the ideal line between the measured endpoints of the converter's transfer function. Deviations are measured without adjusting the line's position for any optimum fit. As a consequence, this linearity number is usually larger than that provided by the best-straight-line approach, but both are valid ways of representing linearity (also called integral nonlinearity or INL).

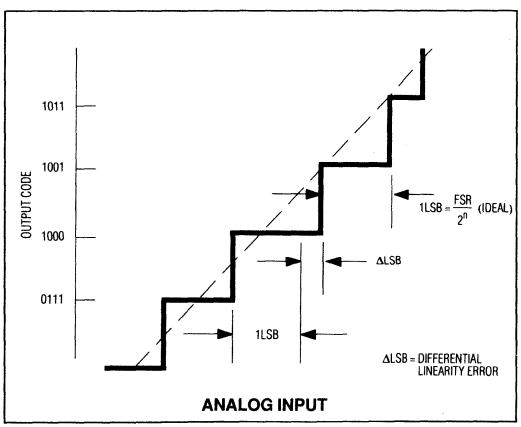


Figure 2. Differential Linearity Error

DNL and No Missing Codes

Differential nonlinearity (DNL) indicates if an A/D is monotonic or has no missing codes. DNL is the deviation of the analog span of each A/D output code from its ideal 1LSB value (Figure 2). A spec of 1/2LSB, for instance, means that a code is at least 1/2LSB but no more than 1.5LSB wide. If DNL is less than 1LSB, no missing codes is assured. Nearly all Maxim A/Ds also specify no missing codes as a separate (and somewhat redundant, but reassuring) guarantee.

Voltage References

What voltage reference is required for an A/D? A number of Maxim's A/Ds contain internal references and manage to eliminate this question for many applications. The internal reference's suitability for an application depends mostly on accuracy and drift requirements. As can be seen from Table 1, the initial reference accuracy ranges from 0.2% to 1.63% for different A/Ds. Examples of applications where initial untrimmed A/D and reference accuracy is not critical are listed in the *Resolution, Accuracy, Etc.* section.

Without adjustment or automatic calibration, reference accuracy and temperature drift relate directly to full-scale errors. If absolute accuracy is required, then a precision

Don't Guess About A/D Converter Needs

reference must be used. If the requirements are too demanding for the internal reference, many devices also accept external references. (Of course Maxim also makes A/Ds without internal references, which are not listed above). Keep in mind that references, much like A/Ds, do not provide untrimmed accuracy without some cost. If stability over temperature or repeatability are all you need, then look for low tempco only.

Ratiometric Systems

Some clever ways have been devised to cheat on reference requirements in certain types of high-accuracy designs. Although the most straightforward architecture may rely on a precisely trimmed reference, the most cost-effective design may not need trimming.

Analog measurements can be either absolute or relative in nature, depending on the input signal. A direct voltage measurement (as with a digital voltmeter) is absolute and relies heavily on absolute reference accuracy. On the other hand, the output signal from a bridge-type transducer (such as a load cell or pressure sensor) is a function of the measured quantity (weight, pressure, etc.) and the bridge's excitation voltage. In a ratiometric system, the same reference drives both the A/D and the bridge excitation, so the actual reference value (along with its error and drift) does not affect the result. The reference voltage need NOT exhibit stability over time and temperature. Either the A/D or an external source can provide the reference in a ratiometric system. In many applications even the power-supply voltage, if free from noise, can suffice.

Multi-Channel Data Acquisition

Single-Chip Solutions

When several analog inputs are measured, some form of signal multiplexing is usually used at the A/D input. A simple and direct way to economize is to expand the analog input using an A/D with an internal multiplexer. One-chip multi-input A/Ds, besides providing obvious component savings, also offer major performance advantages. Multiplexer error contributions and settling delays are eliminated from the system specs since they are included in the A/D's own error and timing limits. For example, the 7.5µs conversion time guaranteed for the MAX180 includes the time used by the multiplexer, track/hold, and A/D. In comparing the specs of the MAX164 (with one input) to the those of the MAX180 (8-channels, Figure 3), it is clear that no compromises are made for the benefit of eight channels; both parts sample at 100kHz.

Combining functions in one CMOS chip not only benefits accuracy but also simplifies the interface. Only one device needs to be addressed: On the MAX180, the same operation can select a channel and start a conversion. Simplifying the interface cuts down on decoding logic and saves power: The MAX180 uses only 110mW.

Separate Input Multiplexers - When?

Despite the convenience and performance that multi-input A/Ds provide, they do have limitations that a separate A/D and multiplexer(s) can sometimes overcome.

Fault Protection

To date, single-chip multiplexed A/Ds with high-voltage fault protection do not exist. Even with Maxim's latchup-proof A/D designs, the level of overdrive insensitivity provided by true fault-protected analog multiplexers cannot be economically added to monolithic A/D designs. The high-voltage protection structures are too large. This is not to say that devices like the MAX180 or MAX150 cannot withstand significant abuse–they can, especially with input-limiting resistors.

Maxim's latchup-proof designs prevent device damage under harsh input conditions; but even with input-limiting resistors and external-clamp diodes on each channel, some limitations cannot be avoided. Crosstalk errors,

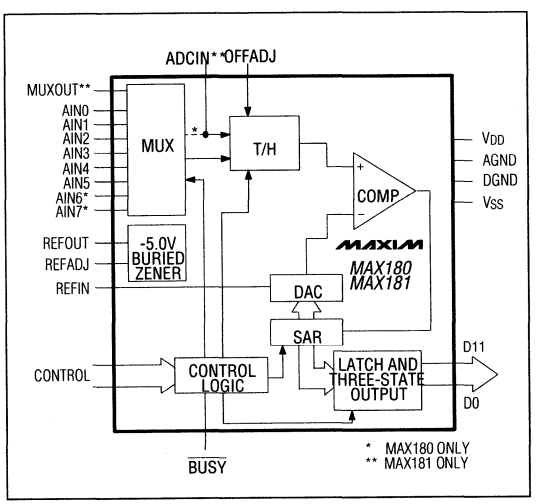


Figure 3. The MAX180 includes a 12-bit A/D, track/hold, reference, and 8-channel multiplexer on one chip. The MAX181 has 6 channels, but provides access to the mux output.

Don't Guess About A/D Converter Needs

caused when inactive channels are driven beyond the supply rails, can be a particular problem.

When such small, but significant, errors can't be tolerated, a true fault-protected analog multiplexer, such as a member of the MAX358 or MAX378 families, is the best choice. They withstand up to 70V overloads without spilling overdrive signals through to selected channels.

Adding Gain and Filtering

Multi-input A/Ds work best when all input signals have a similar dynamic range. If filtering or widely different channel gain is needed, the internal multiplexer usually requires each channel to have its own signal-conditioning circuitry. This can get repetitive and expensive.

Separate A/D and multiplexer components may win out if only one filter and programmable amplifier is needed between the multiplexer output and the A/D input. Maxim's 12-bit MAX181 (Figure 3) addresses this need by bringing out the output of its 6-channel mux and the input of its A/D on separate pins. This way, a companion device such as the MAX270 lowpass filter can provide selectable 4th-order corner frequencies between 1kHz and 20kHz for different channels.

Channel Sample Timing

In some cases, the relative timing of multiplexed signals is important. A typical ADC and multiplexer, whether a one-chip system or not, measure each channel in sequence, so channel 1 is read significantly before channel 8. In dynamic systems, this may add error if the signals of interest occur at the same time; the relative phase may contain information that the channel scanning will distort. One solution is to convert at a sufficiently fast rate so that the time delay between channels is reduced to insignificant levels. The problem with this is that the ADC speed, cost, and possibly power consumption soon reach prohibitive levels.

A better approach, which works well in CMOS, is to sample all input channels at the same time, then multiplex through the track/holds and convert the channel information. Scanning timing errors are eliminated by this approach, which is used in both the MAX155 (4-channel) and MAX156 (8-channel) 8-bit ADCs.

When to Track/Hold

Until recently, few A/D converters included internal track/hold circuits, and you had to determine whether you really needed to add one to the front of your A/D. The guideline for successive- approximation A/Ds limits input signal change during a conversion to 1/2LSB. If the change exceeds this, a track/hold is required to prevent the input from moving during the successive-approximation process.

Because 12-bit ADCs like the MAX162 and MAX183 are extremely fast (3.25µs), one is tempted to think that fairly high-frequency inputs can be converted accurately without using a sample/hold. However, a 12-bit converter with a 5V full-scale range resolves changes in inputs of less than a millivolt, and signals of well below 1kHz change by this amount in under the MAX162's 3.25µs conversion time. In fact, for frequencies as low as 11Hz, a hold function is required if 12-bit performance is to be maintained.

Other Track/Hold Advantages

Having given the textbook reason why track/holds are beneficial, there are others that may be more significant for practical applications with contemporary ADCs. A high-speed, un-sampled successive-approximation ADC places transient loads on the signal source during each bit test of the conversion. If the signal source doesn't settle in time for the bit decision, the ADC's comparator bases its decision on errant information, resulting in converter noise and nonlinearity. This is true even for low-frequency signals that don't violate the 1/2LSB rule discussed previously. The result is that many successive-approximation and some flash ADCs place high demands on the signal source, particularly with 12-bits and above. Wide-bandwidth amplifiers are needed to drive non-sampled ADCs, even for low-bandwidth signals.

Sampling A/D converters like the MAX164 and MAX180 12-bit families demand very little from the signal source in terms of dynamic capability, even though they are successive-approximation devices. Current is drawn from the input source, not on each bit test, but only once when the input is sampled. This accommodates a much wider variety of signal sources without buffering.

Interface Options

The best A/D interface is fast, requires minimal hardware, and uses compact or existing software. Unfortunately, the specific A/D interface architecture that accomplishes this varies widely with application. Common microprocessors use 8- and 16-bit busses. Microcontrollers use 4- and 8-bit busses. Both can use serial interfaces.

Don't Guess About A/D Converter Needs

Each Maxim A/D is designed for simple hardware and software connection to a wide range of processor types. Flexibility is enhanced by frequently allowing output formatting in different data widths where appropriate, as with the 12-bit MAX163/4/7, which connects to either 8- or 16-bit busses. In addition, several interface modes are selectable using only one or two control lines. For example, with the MAX163/4/7 the microprocessor can: 1) start a conversion, perform other tasks, and then come back to read data, or 2) start a conversion with a READ, and wait until the ADC supplies the answer. The microprocessor uses a BUSY output on the ADC to stretch the read cycle, making the ADC appear like a slow-memory device (Figure 4).

Serial Interfaces

In data-acquisition designs where size and board space are at a premium, serial interfaces can provide major advantages. For an equivalent 12-bit ADC, a serial device fits into an 8-pin package (MAX170) while a parallel part (MAX162/172) uses 24 pins. Also, the serial device's narrow data path does not impact the conversion time: The MAX170 has a 5.6µs conversion rate.

Besides saving space, a serial interface can cut the cost of taking electrically-isolated measurements. By using opto-couplers to isolate data lines, the ADC transmits information while severing electrical contact with the processor. The ADC and the analog signal are isolated. A serial device works best for this because only three interface lines require opto-couplers: Clock In, Data Out, and Convert Start. The 12-bit MAX171 (to be announced soon) simplifies isolated circuitry even further by including the opto-couplers with the A/D and reference in one package (Figure 5).

What is the value of isolation? Some operating environments do not allow the electrical connection between the signal source and the measuring system. This is a frequent safety requirement in industrial applications where it is possible for the input signal to be hot to the AC power line, either inadvertently or by design. Isolation also provides advantages for noise reduction by eliminating ground loops and by providing superior common-mode rejection to most differential input schemes. This is especially useful in large systems where signals from many remote locations are returned to one point. Each signal return line is likely to be at a slightly different potential, so ground-loop currents are almost certain.

Conversion Time vs. Conversions per Second

A/D converter speed can be specified in terms of conversion time (time required for one conversion) or in terms

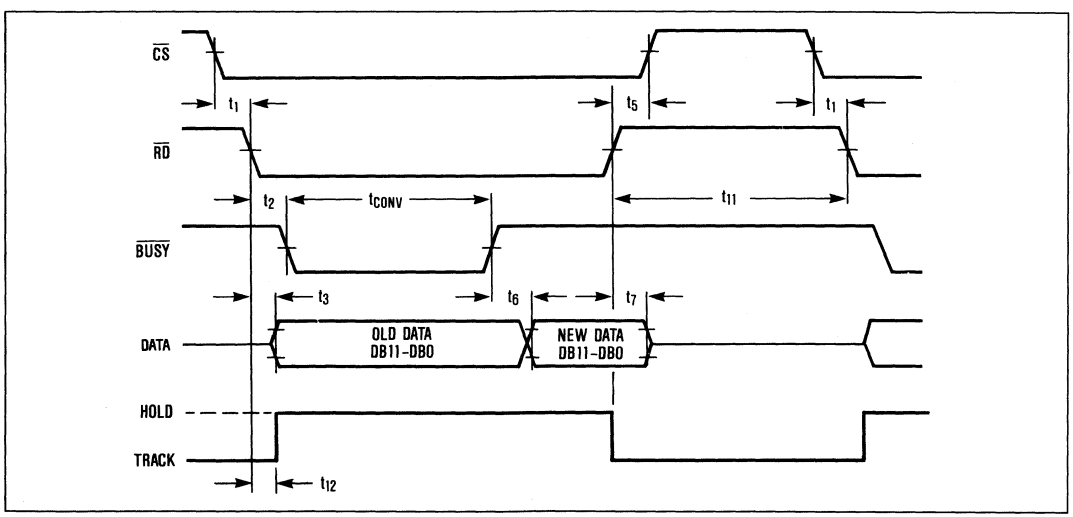


Figure 4. The A/D appears like a slow-memory device in this interface. The BUSY output stretches the microprocessor read cycle.

Don't Guess About A/D Converter Needs

of conversions (or samples) per second. These are closely related, but conversion rate doesn't always translate exactly to the inverse of conversion time. This is because ADCs often require some time between conversions.

The MAX167 performs a conversion in 7.81µs (12.5 clock cycles) if started in sync with a 1.6MHz clock. Data-access timing limits prevent the next conversion from starting immediately (Figure 6). Keeping these times as short as possible and guaranteeing data-bus timing specs over temperature minimizes dead time between conversions, allowing the MAX167 to continuously perform 100k samples per second. This rate includes the operating time of the ADC's internal track/hold.

Note also that the MAX167 (and most other Maxim ADCs) can "pipe line" the output data to increase interface speed. This means, as each new conversion is started by $\overline{RD}$, the results of the last conversion immediately appear on the data bus. The data is always one conversion old, but it can be accessed without waiting; separate read and write commands aren't needed. The MAX167 also implements more conventional interface, including those with 8-bit buses.

AC Signal Processing

When an ADC measures an AC signal, deviations from the ideal converter transfer function generate noise and distortion in the digital-output data. The severity of these

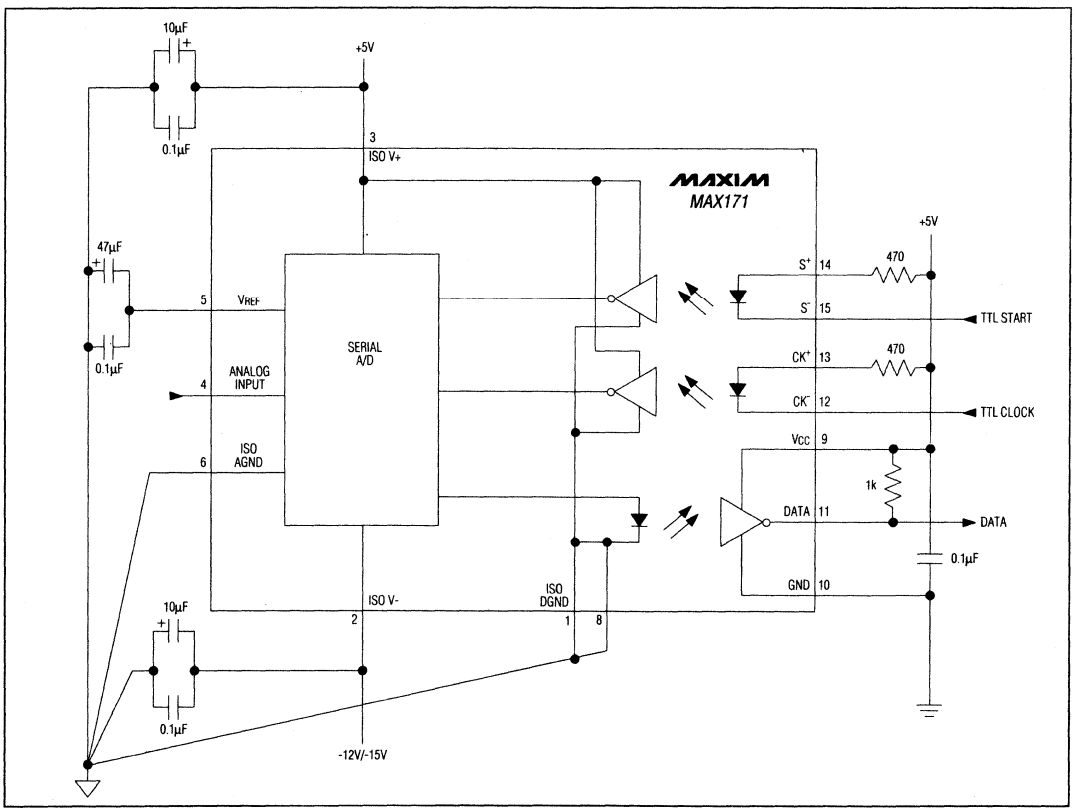


Figure 5. The MAX171 (to be announced soon) isolates measurements by including three high-speed optos in its 16-pin package.

Don't Guess About A/D Converter Needs

distortions may not correlate well to classic A/D converter specifications like offset, linearity, full-scale error, etc. In fact, large offset and full-scale errors do very little to harm AC performance, while the effect of linearity may depend more on the shape of the error rather than the amplitude. Also, converter noise expressed as a portion of an LSB does not indicate the effect on dynamic signals. What is important for DC-signal measurements may not be for AC-signal processing.

The dynamic performance of a number of Maxim's ADCs is tested and guaranteed independently of the classic DC-accuracy specs. Tested parameters include Total Harmonic Distortion, Signal-to-Noise-plus-Distortion, and Peak Harmonic (or Spurious) Noise. The tests are implemented by applying a low-distortion test signal to the ADC and analyzing the digital-conversion results with an FFT algorithm to determine distortion and noise. Nearly all of Maxim's sampling ADCs are tested in this manner.

Multiple Sources and "Standards" for A/Ds

As data-acquisition designers are acutely aware, not many A/D converters are second sourced. They are not like op amps, with a convenient universal pin out. Maxim has purposely adhered to popular pin outs where possible. Maxim has maintained compatibility with AD574 and AD674, The most common 12-bit ADC footprints, originally high-cost hybrid devices. Three Maxim BiCMOS monolithic devices improve the basic 574 design while reducing conversion time and power consumption 3 times. Compatible parts are:

MAX174
MX574A
MX674A

AD7572: 2nd generation 12-bit mini-standard with improved performance over 574 devices. A big advantage is its narrow DIP package compared to the 574 24-pin wide footprint. Compatible parts are:

MX7572
MAX162 - fastest conversion time, 3.25us
MAX172 - low cost
MAX163, **MAX164**, **MAX167** } track/hold included but still fully compatible

ADC0820/AD7820: High-speed, 8-bit footprints that operate on 5V. Compatible devices are:

MX7820
MAX150 - adds internal 2.5V voltage reference on an originally unused pin to maintain compatibility

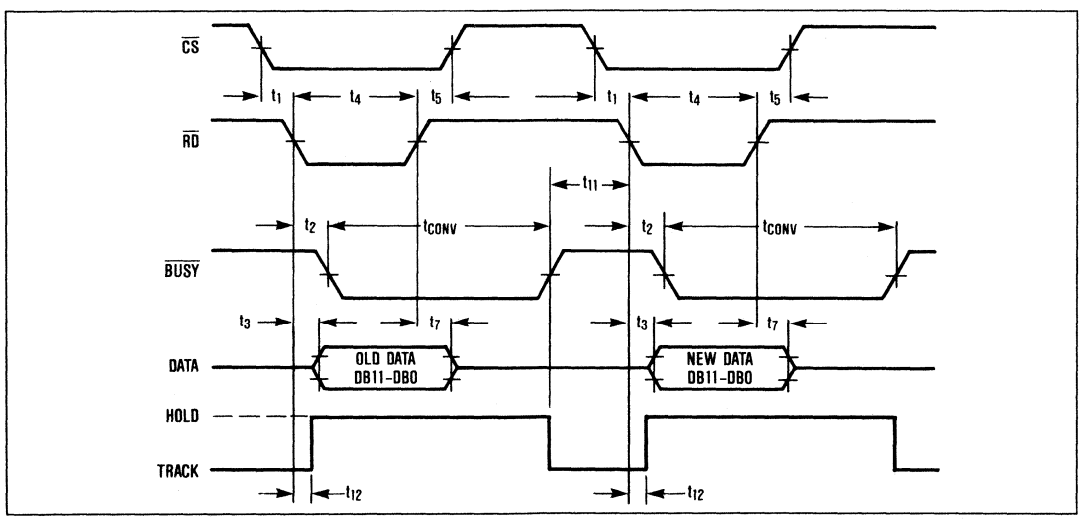


Figure 6. MAX163/164/167 ROM Mode, Parallel-Read Timing Diagram

Don't Guess About A/D Converter Needs

Performance Problems

Noise

Noise pick-up can be a problem when measuring any analog signal, but is particularly troublesome when the signal amplitudes are small (100mV or less). Low-level analog signals should be digitized as close to their source as possible (this is more easily done with small, serial-output ADCs like the MAX170), or should be amplified, again near the source, to the highest practical level. To minimize pick-up, route low-level signals away from clock lines, relays, and other noisy switching circuits.

In data acquisition, circuit nodes that are particularly susceptible to noise are: 1) A/D input pins when not driven from a buffered source, 2) the inverting inputs of op amps, 3) the center nodes on signal divider networks, and 4) the outputs of unbuffered filters. These should be made as physically small as possible to reduce coupling from noise sources. Separate analog and digital circuits on the board where possible. Very low-level signals may call for separately shielded sub-circuits.

If the system exhibits missing codes and noise when the source and layout are clean, the problem may be occurring at the A/D input. Many successive-approximation ADCs (those without internal track/holds) are difficult to drive (see *Other Track/Hold Advantages*). A good test to check the cause is to slow down the system clock. This allows the input source more time to settle after being loaded by the A/D. If the noise abates with a slower clock, the input signal may need a buffer.

The fact that an ADC's reference input doubles as an analog input may be lost in many acquisition designs. This is important because some ADC architectures are less effective than others in rejecting reference noise. If the reference settles poorly in response to current demands in the ADC, this may also be a noise source.

Grounds, Bypassing, Shielding

Success is never assured in a prototype--even in the best-designed data-acquisition systems. A problem's source can be obscure, but a verdict of "device failure," "poor accuracy," or "doesn't meet spec" often stems from a disregard for Ohm's Law and basic electro-magnetic principles. Solutions can range from compensating the scope probe to properly bypassing the power supply.

If you are unsure about grounding, try to connect all signal, ADC, and power grounds to a single point. This minimizes the ground loops that generate unwanted currents when intersected by stray magnetic fields. It also prevents the voltage drop in current-carrying lines from affecting the ground reference of more sensitive circuits. Simpler "chain" grounding, on the other hand, allows the feedback from such voltage drops to cause DC errors and oscillation.

Analog and digital circuitry for precision measurement should have separate power supplies, and ideally the analog and digital circuits should be completely isolated from one another. But full compliance with these ideals is seldom practical or cost effective. An effective power-supply compromise is to derive a separate, filtered supply for analog and A/D circuitry by adding an RC network to the system power supply. A/D and D/A converters necessarily commingle their internal digital and analog circuits; if a device offers separate analog and digital ground pins, it's best to connect both to the one best (quietest and usually analog) ground only.

Before cutting corners on grounding hardware and power-supply bypassing components you should carefully consider whether the system is likely to be expanded. Noise sources that aren't a problem with a few channels may grow geometrically as channels are added. Shields (if present) should be considered as water-tight extensions of the overall enclosure. Shielded cables should be grounded at one end only, preferably at the end nearest the single-point ground.

Murphy Meets Morrison

Finally, never trust blindly in emulators and development systems when troubleshooting and debugging analog systems. These are invaluable time savers, but beware any results that conflict with common sense. Because the instruments provide second-hand information about the state of your hardware, they can be fooled by the very problem you are chasing.

Once you know the problem's approximate location, it helps to remove, bypass, or clear away the buffers, interface ICs, and other devices that may mask the problem or confuse the issue. Then, there's no substitute for observation right at the pins of a suspect device. Condemning evidence should be witnessed first hand. Also, if a "fix" doesn't work, be sure to remove it before searching on.

A good text that takes much of the witchcraft out of grounding and other practical analog problems is *Grounding and Shielding Techniques in Instrumentation* by Ralph Morrison, published by Wiley and Sons, New York, NY. Though brief, it offers complete discussions without cumbersome levels of math.

MAXIM

±32,768 Count ADC with Serial Interface

General Description

The MAX132 is a CMOS ±32,768 serial-output analog-to-digital converter (ADC). Multi-slope integration provides high-resolution conversions in less time than standard integrating ADCs. The MAX132 converts up to 200 conversions per second. Low conversion noise allows specifying electrical characteristics with a full scale of only 400mV (12µV per count). A simple 4-wire serial interface connects easily to all common microprocessors. Twos complement output simplifies decoding of bipolar measurements.

Supply current is 65µA during normal operation and only 5µA in standby mode. Four serially programmed output bits can be used to control an external multiplexer or programmable gain amplifier. The MAX132 fits in a compact 24-pin DIP or small outline package. Both commercial and extended temperature ranges are available. High resolution and compact size make this device ideal for data loggers, weigh scales, data-acquisition systems, and panel meters.

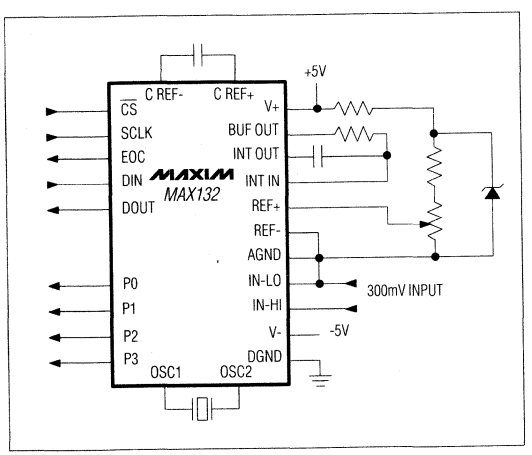
Applications

Data Acquisition

Control Applications

Measurement of Analog Signals
- Pressure
- Resistance
- Flow
- Temperature
- Voltage
- Power
- Current

Functional Diagram



Features

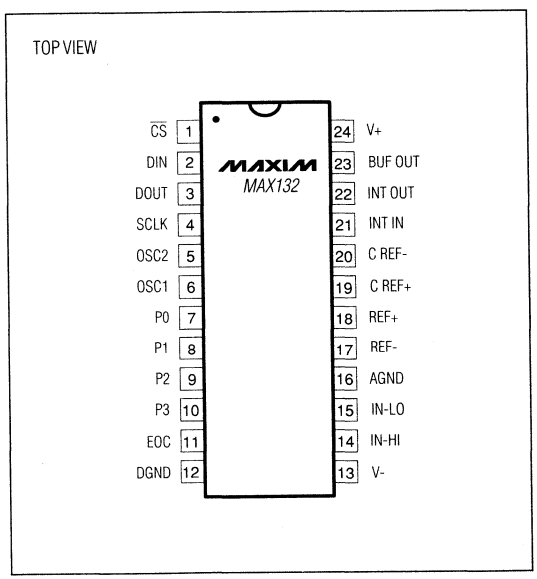
- ♦ ±32,768 Count Resolution
- ♦ Conversions up to 200 per Second
- ♦ Integrating ADC - Low Noise
- ♦ ±5V Supplies, 65 µA Operation Current
- ♦ 5µA Standby Current
- ♦ Digital Zero Reading on Command
- ♦ Serial I/O Interface
- ♦ Serial Programmed Logic Output for MUX and PGA

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX132CNG	0°C to +70°C	24 Plastic DIP
MAX132CWG	0°C to +70°C	24 SO
MAX132C/D	0°C to +70°C	Dice*
MAX132ENG	-40°C to +85°C	24 Plastic DIP
MAX132EWG	-40°C to +85°C	24 SO
MAX132ERG	-40°C to +85°C	24 CERDIP

Contact factory for dice specifications.

Pin Configuration



MAXIM

±20,000 Count ADC with Parallel Interface

General Description

The MAX135 is a CMOS, ±20,000 count parallel-output analog-to-digital converter (ADC). Multi-slope integration provides high-resolution conversions in less time than standard integrating ADCs. The MAX135 converts up to 200 conversions per second. Low conversion noise allows specifing electrical characteristics with a full scale of only 300mV (15µV per count). A simple 8-bit parallel data bus and three control lines easily interface to all common microprocessors. Twos complement output simplifies decoding of bipolar measurements.

Supply current is 65µA during normal operation and only 5µA in standby mode. The MAX135 fits in a 28-pin DIP or Small Outline package, both commercial and extended temperature ranges are available. High resolution and compact size make this device ideal for data loggers, weigh scales, data-acquisition systems, and panel meters.

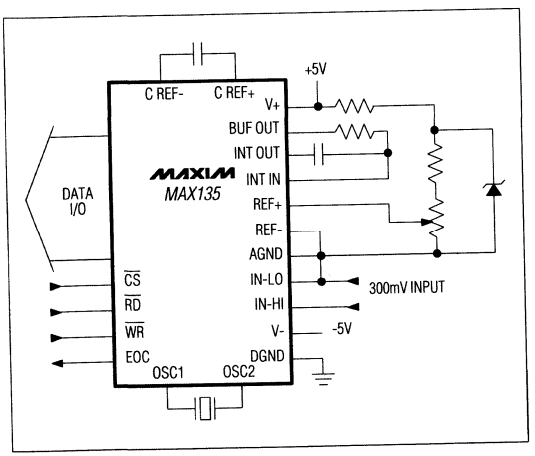
Applications

Data Acquisition

Control Applications

Measurement of Analog Signals
- Pressure
- Resistance
- Flow
- Temperature
- Voltage
- Power
- Current

Functional Diagram



Features

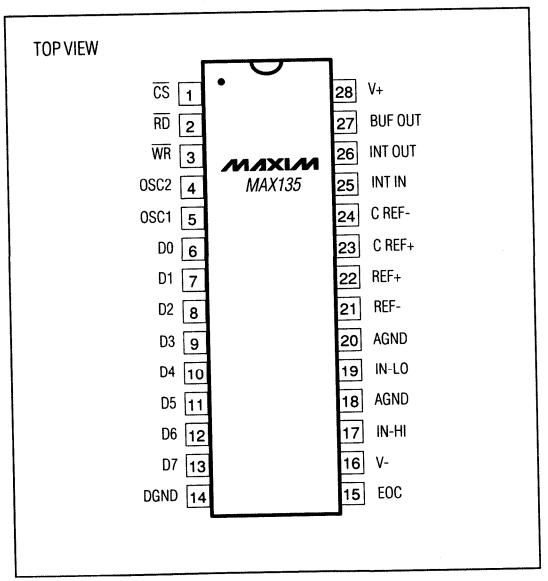
- ♦ **±20,000 Count Resolution**
- ♦ **Conversion Rate up to 200 per Second**
- ♦ **Integrating ADC - Low Noise**
- ♦ **±5V Supplies, 65µA Operation Current**
- ♦ **5µA Standby Current**
- ♦ **Digital Zero Reading on Command**
- ♦ **8-Bit Parallel Twos Complement Interface**
- ♦ **Three-State Logic Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX135CPI	0°C to +70°C	28 Plastic DIP
MAX135CWI	0°C to +70°C	28 Wide SO
MAX135C/D	0°C to +70°C	Dice*
MAX135EPI	-40°C to +85°C	28 Plastic DIP
MAX135EWI	-40°C to +85°C	28 Wide SO
MAX135EJI	-40°C to +85°C	28 CERDIP

** Contact factory for dice specifications.*

Pin Configuration



MAXIM

300kHz 10-Bit A/D Converter with Reference and T/H

General Description

The MAX151 is a high-speed, easy-to-use, microprocessor (μP) compatible 10-bit Analog-to-Digital Converter (ADC) with Track-and-Hold (T/H). Half-flash techniques allow a typical conversion time of 1.9μs with a Total Unadjusted Error (TUE) of ±1LSB (Max). The converter has a 0V to +5V analog input voltage range and uses ±5V supplies.

The MAX151 internally tracks and holds the analog input signal, eliminating the need for an external T/H when digitizing high-speed AC input signals. The MAX151 also contains an internal 4V reference, making the part a complete, low-cost ADC. Power consumption is typically 275mW.

The MAX151 interfaces directly to a μP by appearing as a memory location or Input/Output (I/O) port. Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) inputs control three-state outputs. Two interface modes ensure compatibility with most popular μPs. The MAX151 is available in both 0.3" DIP and Wide SO packages.

Applications

Digital Signal Processing

High-Speed Data Acquisition

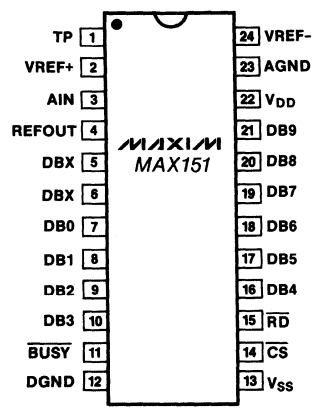
Telecommunications

High-Speed Servo Loops

Audio Systems

Pin Configuration

Top View



DIP/SO

Features

- ◆ **10-Bit Resolution and Accuracy**
- ◆ **±1LSB Total Unadjusted Error**
- ◆ **2.5μs Max Conversion Time (0.5μs Input Acquisition Time)**
- ◆ **300kHz Sampling Rate**
- ◆ **Internal 60ppm/°C Reference**
- ◆ **1ppm/°C Gain and Offset Drift**
- ◆ **Internal Clock**
- ◆ **±5V Supplies with 275mW Power Dissipation**
- ◆ **24-Pin 0.3" DIP and Wide SO Packages**
- ◆ **Tested for DC and Dynamic Specifications**

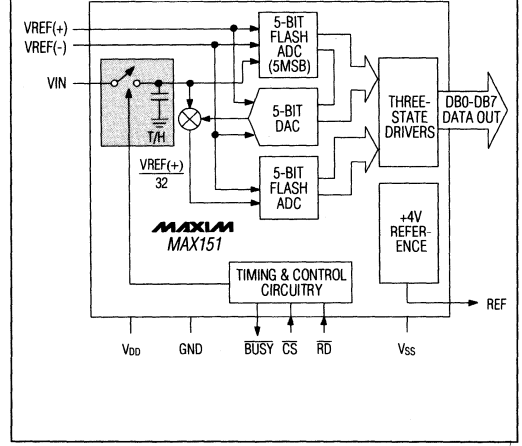
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX151ACNG	0°C to +70°C	24 Plastic DIP	1.0
MAX151BCNG	0°C to +70°C	24 Plastic DIP	1.5
MAX151ACWG	0°C to +70°C	24 Wide SO	1.0
MAX151BCWG	0°C to +70°C	24 Wide SO	1.5
MAX151BC/D	0°C to +70°C	Dice*	1.5

** Consult factory for dice specification.*

Ordering information continued on page 11.

Block Diagram



300kHz 10-Bit A/D Converter with Reference and T/H

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +6V
V_{DD} to V_{SS} ..... -0.3V, +12V
V_{DD} to AGND ..... -0.3V, +6V
Digital Outputs and Inputs to DGND ..... -0.3V, V_{DD} +0.3V
Analog Inputs to V_{SS} ..... -0.3V, V_{DD} +0.3V
REFOUT Current ..... Indefinite Short to V_{DD} or AGND
Power Dissipation (Any Package) to +75°C 1000mW
Derate Above 75°C by ..... 10mW/°C

Max Junction Temperature
MAX151C, MAX151E ..... 150°C
MAX151M ..... 175°C
Operating Temperature Ranges
MAX151C ..... 0°C to +70°C
MAX151E ..... -40°C to +85°C
MAX151M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ACCURACY						
Resolution			10			Bits
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Total Unadjusted Error	TUE	MAX151A MAX151B			±1 ±1.5	LSB
Power-Supply Rejection		V_{DD} = ±5% V_{SS} fixed V_{SS} = ±5% V_{DD} fixed			±1/4 ±1/4	LSB
DYNAMIC PERFORMANCE (f_S = 300kHz, V_{IN} = $5V_{P-P}$ at 40kHz)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)		55	58		dB
Total Harmonic Distortion	THD	First 5 harmonics		-70	-60	dB
Peak Harmonic or Spurious Noise				-70	-60	dB
Full-Power Input Bandwidth	FPBW			5		MHz
ANALOG INPUT						
Analog Input Range			VREF-		VREF+	V
Input Resistance	RIN			10		MΩ
Input Capacitance	CAIN	In series with 150Ω		150		pF
Input Current	IAIN	AIN = 0V to V_{DD}			±10	μA
REFERENCE INPUT						
Ladder Resistance		VREF+ to VREF-	0.5	1		kΩ
Negative Reference Voltage			V_{AGND}-0.1		V_{AGND}+0.1	V
Reference Voltage (Note 2)		VREF+ to VREF-	1		V_{DD}	V
INTERNAL REFERENCE						
Output Voltage		T_A = 25°C	3.970	4.000	4.030	V
Temperature Coefficient (Note 3)					60	ppm/°C
External Load Current		Must not change during conversion (In addition to ladder current)			2	mA
Power-Suppy Rejection		V_{DD} = ±5% V_{SS} fixed V_{SS} = ±5% V_{DD} fixed			±3 ±2	mV
Output Impedance				0.4	1.5	Ω

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$	2.4			V
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$			0.8	V
Input Current	IIN	$\overline{CS}$, $\overline{RD}$; V_{IN} = 0V to V_{DD}			±10	µA
Input Capacitance (Note 1)	CIN	$\overline{CS}$, $\overline{RD}$			10	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB9 I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB9 I_{SRC} = 200µA	4.0			V
Floating State Current	ILKG	DB0-DB9 VOUT = 0V to V_{DD}			±10	µA
Floating Capacitance (Note 1)	COUT				15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		4.75		5.25	V
Negative Supply Voltage	V_{SS}		-4.75		-5.25	V
Positive Supply Current	IV_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		30	45	mA
Negative Supply Current	IV_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		25	40	mA
Power Dissipation	PD	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V, Including Ladder; REFOUT connected to VREF+		275	425	mW

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V; Guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0		ns
Data Access Time (Notes 4, 5)	t_{RD}	C_L = 100pF		70	**120**		**180**	ns
Bus Relinquish Time (Notes 4, 5)	t_{DH}				**70**		**100**	ns
Conversion Time (Note 4)	t_{CONV}			1.9	**2.5**		**2.5**	µs
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 4)	t_{BUSY}	C_L = 100pF		70	**140**		**200**	ns
Data Setup Time After $\overline{BUSY}$ (Notes 4, 5)	t_B				**30**		**50**	ns
Delay Between Conversions	t_D	With $R_S < 50\Omega$	500			500		ns
		With $R_S < 1k\Omega$	1.5			1.5		µs
$\overline{RD}$ Pulse Width	t_{RPW}	To minimize digital coupling in ROM Mode			300		300	ns
Aperture Delay	t_{AP}			30				ns
Aperture Jitter				100				ps

Note 1: Guaranteed by design, not 100% tested.

Note 2: Reduce accuracy at low reference voltages. See Typical Operating Characteristics.

Note 3: VREF Tempco = ΔVREF/ΔT, where ΔVREF is the change in the reference voltage from T_A = 25°C to T_{MIN} or T_{MAX}.

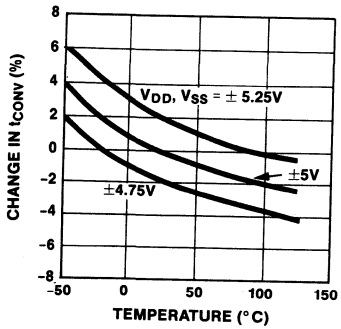
Note 4: 100% production tested.

Note 5: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. t_{RD} and t_B are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. t_{DH} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

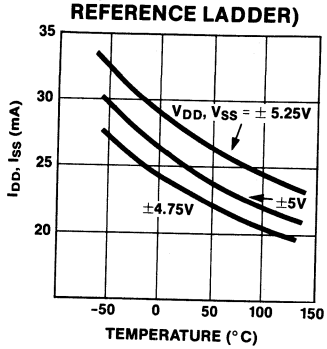
300kHz 10-Bit A/D Converter with Reference and T/H

Typical Operating Characteristics

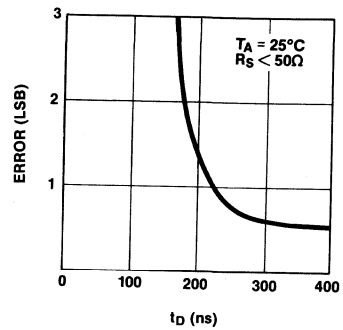
CONVERSION TIME vs. TEMPERATURE



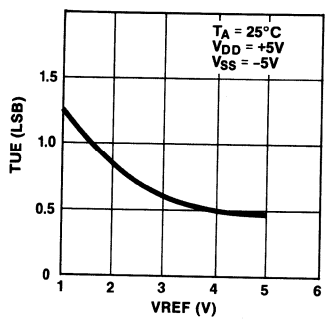
POWER-SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



ACCURACY vs. t_D



ACCURACY vs. VREF (VREF = VREF+ - VREF-)



300kHz 10-Bit A/D Converter with Reference and T/H

Pin Description

PIN	NAME	FUNCTION
1	TP	Test Pin, leave open.
2	VREF+	Positive Ladder Input, upper limit of reference span. Set the full-scale input voltage. Range: 1V to V_{DD}.
3	AIN	(Sampling) Analog Input
4	REFOUT	+4V Reference Output, usually connected to VREF+.
5-6	DBX	(Reserved for DB0-1, future 12-bit version, = LOW.)
7-10	DB0-DB3	Three-State Data Output, Bits 0-3
11	$\overline{BUSY}$	$\overline{Busy}$ Status Output, low when conversion is in progress.
12	DGND	Digital Ground.
13	V_{SS}	Negative Supply, -5V.
14	$\overline{CS}$	$\overline{Chip\ Select}$ Input, must be low for the ADC to recognize $\overline{RD}$.
15	$\overline{RD}$	Active Low $\overline{Read}$ Input, starts conversion when $\overline{CS}$ is low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
16-21	DB4-DB9	Three-State Data Output, Bits 4-9
22	V_{DD}	Positive Supply, +5V
23	AGND	Analog Ground
24	VREF-	Negative Voltage Ladder Input, lower limit of reference span. Set the zero-code voltage. Range: AGND ±0.1V.

Detailed Description

ADC Operation

The MAX151 half-flash A/D converter contains 31 comparators. The analog input is sampled by each comparator and compared to a resistive ladder DAC. A 5-bit coarse conversion result is then generated from the ladder DAC, subtracted from the analog input, and compared to a 2nd resistive ladder. 5 coarse and 5 fine bits are output in 10-bit wide parallel output format.

The voltage at the top and the bottom of the reference ladder determines the MAX151's zero-scale and full-scale input voltage. The analog input can range from 0V to +5V. An internal reference provides a 4.000V nominal output and is used by connecting REFOUT to VREF+ and VREF- to AGND. The reference provides up to 2mA of external load current in addition to the current it supplies to the internal ladder. Figure 3 shows the MAX151 in a typical application.

Analog Input - T/H

The MAX151 input can be modeled as a 150pF load in series with 150Ω (Figure 4). The comparator's input capacitance acts as a "hold" capacitor and must be completely charged by the input signal with every A/D conversion.

The input signal sees AIN as a capacitor which is switched between itself and AGND. Between conversions, the signal is tracked by connecting the capacitor to AIN. When a conversion begins, the capacitor disconnects from the analog input, and the A/D performs its conversion. At the end of the conversion, it reconnects to the input and charges to the input signal.

The MAX151 can digitize a variety of high-speed input signals without an external sample-and-hold. Although the conversion time for the MAX151 is 1.9μs, the time the input must be stable is much less.

The time needed for the T/H to acquire an input signal is a function of how quickly the input capacitance can be charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + 150\Omega)150pF$$
(but never less than 500ns)

Where R_S = source impedance of the input signal.

The MAX151 samples the analog input approximately 30ns after $\overline{RD}$ and $\overline{CS}$ (which are internally NANDed) are pulled low. This aperture delay is caused by the propagation delay of the internal logic. The variation in this delay from one conversion to the next is called aperture jitter, and it is typically less than 100ps.

The architecture of the MAX151 allows signals with high slew rates to be converted without error (Figure 4). The errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without sample-and-hold: a 1μs SAR converter would be unable to measure a 1kHz, 5V sine wave without using an external sample-and-hold. With no external sample-and-hold, the MAX151 can typically measure $5V_{p-p}$, 100kHz waveforms.

300kHz 10-Bit A/D Converter with Reference and T/H

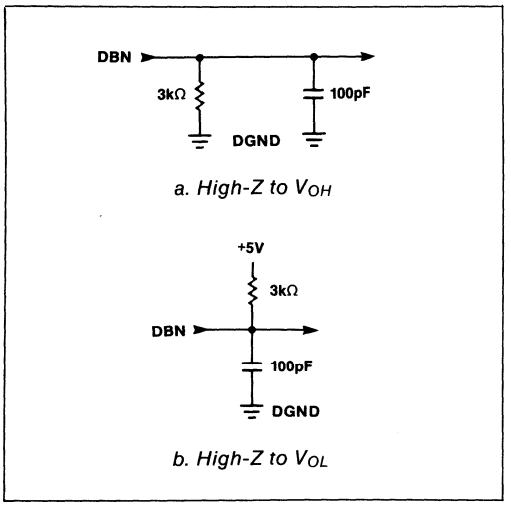


Figure 1. Load Circuits for Data Access Time Test

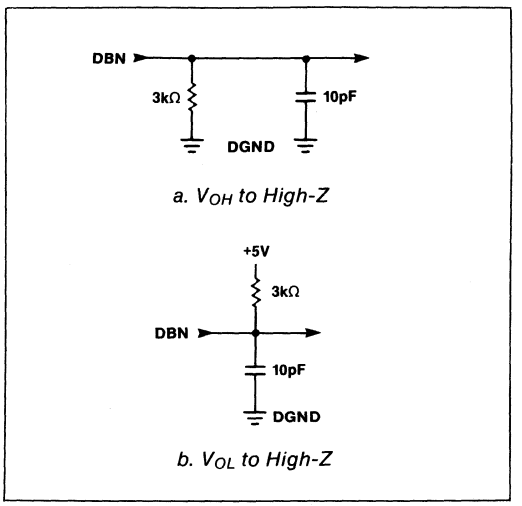


Figure 2. Load Circuits for Bus Relinquish Time Test

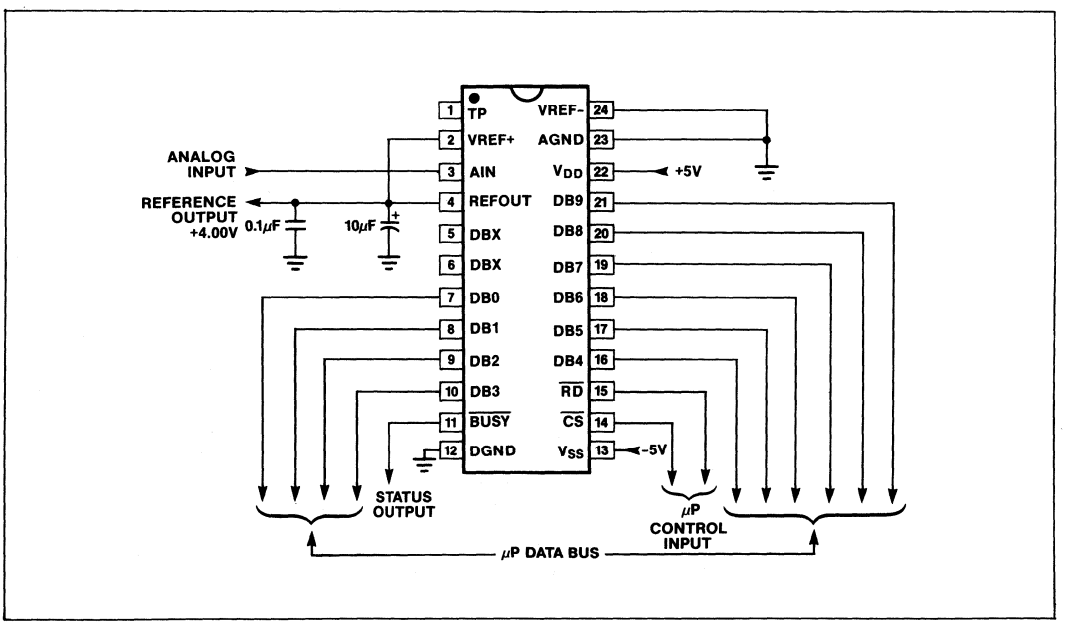


Figure 3. MAX151 Operational Diagram

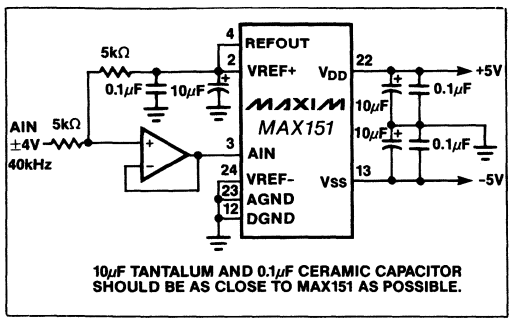


Figure 4. ±4V Bipolar Input with Driving Amplifier

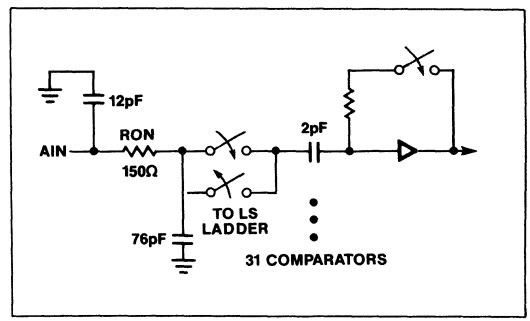


Figure 5. Equivalent Input Circuit

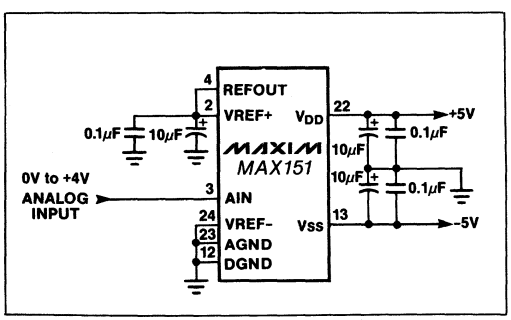


Figure 6. Internal Reference

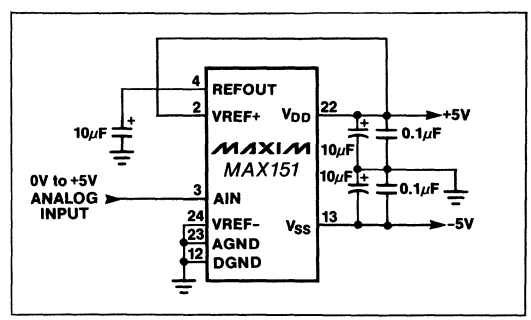


Figure 7. Power Supply as Reference

Input Drive Requirements

To fully utilize the speed advantages of the MAX151, the input should be driven by a fast settling op amp. The OP-42 and AD711 are 10-bit accurate op amps which can drive the MAX151. Both settle to 0.01% in less than 1μs.

On the other hand, since the acquisition time can be user controlled by adding delay between conversions, a slow amplifier or no amplifier can be used. For example, with a 1kΩ driving impedance, waiting 1.5μs between conversions ensures 10-bit accuracy. The MAX400 amplifier works well as an input buffer at these reduced conversion rates.

The analog input can be easily offset by the driving amplifier to obtain a ±4V bipolar input range for DSP applications (Figure 4).

Input Current

The MAX151 input behaves somewhat differently from conventional ADCs. Data-sampling comparators take varying amounts of current from the input. Figure 5 shows the equivalent input circuit. When the conversion starts, AIN is disconnected from the analog input signal. When BUSY goes high at the end of a conversion, AIN is connected to 31 2pF capacitors. During this tracking phase (BUSY = High), the input capacitors must be charged to the input voltage through the resistance of the internal analog switches (typically 150Ω). In addition, about 90pF of stray capacitance must be charged.

Internal Reference

The MAX151 has a +4.00V buried zener reference. The reference output is available at REFOUT and must be bypassed to AGND with a 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor. The capacitors minimize noise by providing a low impedance path to ground for high-frequency signals. These capacitors should be connected even if the internal reference is not used. A resistor must NOT be connected between the bypass capacitors and REFOUT. In addition to the current it supplies to the ladder, the internal reference output buffer can source up to 2mA for external circuitry.

To use the on-chip reference, connect REFOUT to VREF+ and VREF- to ground. The 4.00V output is referenced to AGND. For the majority of 10-bit measurement applications, use the internal reference. If desired, an external reference can be used as an alternative (Figures 6-8).

300kHz 10-Bit A/D Converter with Reference and T/H

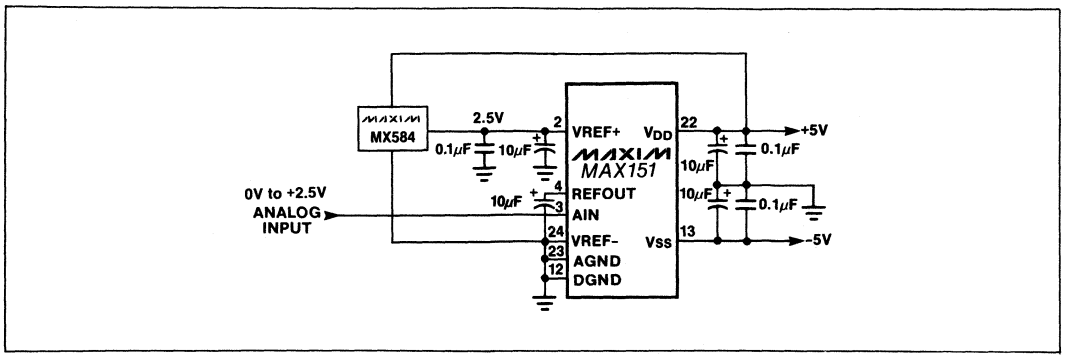


Figure 8. External Reference 2.5V Full-Scale

The VREF+ and VREF- inputs set the full-scale and zero-input voltages of the A/D. More precisely, the voltage at VREF- defines the input which produces an output code of all 0s, and the voltage at VREF+ defines the input which produces an output code of all 1s (Figure 9).

Gain and Offset Adjustment

Figure 9 shows the nominal unipolar transfer function of the MAX151. Code transitions occur at successive integer Least Significant Bit (LSB) values. Output coding is natural binary with 1LSB = 3.91mV (4V/1024) for a 4V reference.

End-point errors are very low. But, if the end points (offset and full scale) need to be adjusted to compensate for errors from other components in the system, use the following techniques. In applications where full-scale adjustment is required, the connection in Figure 10 provides ±0.5%, or ±5 LSBs of adjustment range. If both offset and full-scale range need adjustment, the circuit in Figure 11 is recommended. Offset should be adjusted before full-scale. For the MAX151 (0V to +4V input range), apply 1/2 LSB (2mV) to the analog input and adjust R12 so the digital output code changes between 00000 00000 and 00000 00001. To adjust full-scale, apply FS-3/2LSB (3.994mV) and adjust R8 until the output code changes between 11111 11110 and 11111 11111. There may be slight interaction between adjustments. If an input gain of 2 is acceptable, the connection in Figure 11 can be simplified by removing R5 and R6.

Starting a Conversion

The ADC is controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. The T/H holds the value of the input signal, and a conversion is triggered by the falling edge of $\overline{CS}$ and $\overline{RD}$. The $\overline{BUSY}$ output goes low as soon as the conversion starts. $\overline{BUSY}$ goes high at the end of the conversion, and the result is latched into three-state output buffers.

Digital Interface

The MAX151 has two basic interface modes: The Slow Memory Mode requires handshaking, but the ROM Mode does not. The length of the $\overline{RD}$ pulse tells the chip which mode is anticipated. In both modes, conversions are initiated by a falling $\overline{RD}$ and $\overline{CS}$ signal.

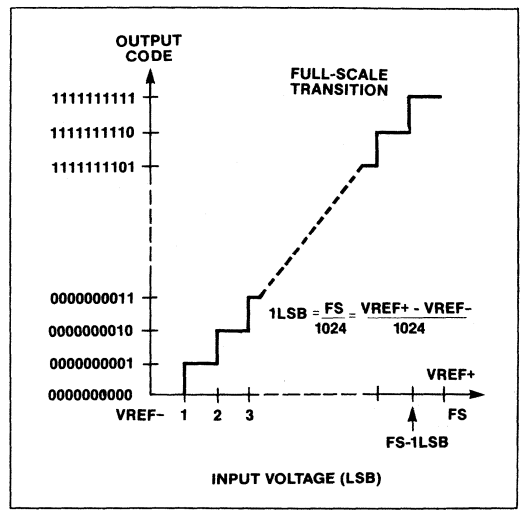


Figure 9. Ideal Transfer Function

In the Slow Memory Mode, the μP actively holds $\overline{RD}$ low until a complete conversion has been performed. During the conversion, the data outputs are active with the data from the previous conversion. After the conversion ends (t_{CONV}), the μP can read the result of the conversion. The $\overline{BUSY}$ signal is used as a handshake to tell the μP when a conversion ends.

In the ROM Mode, a short $\overline{RD}$ pulse starts a conversion and reads the result of the previous conversion. Note, the width of this pulse should not exceed 300ns.

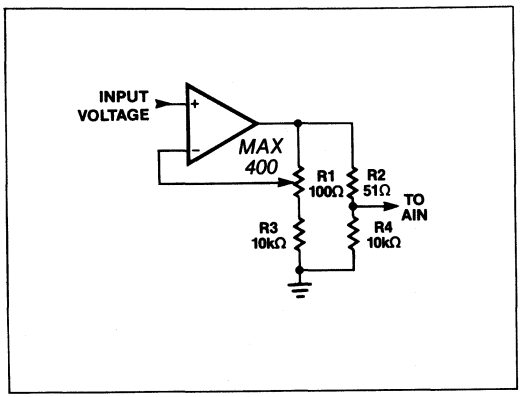


Figure 10. Trim Circuit for Full-Scale Only (±0.5%)

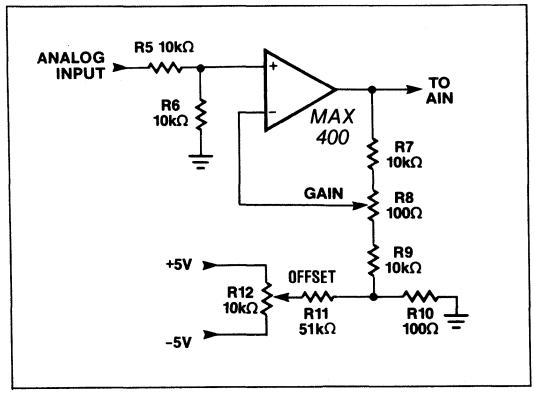


Figure 11. Offset (±20mV) and Gain (±0.5%) Trim Circuit

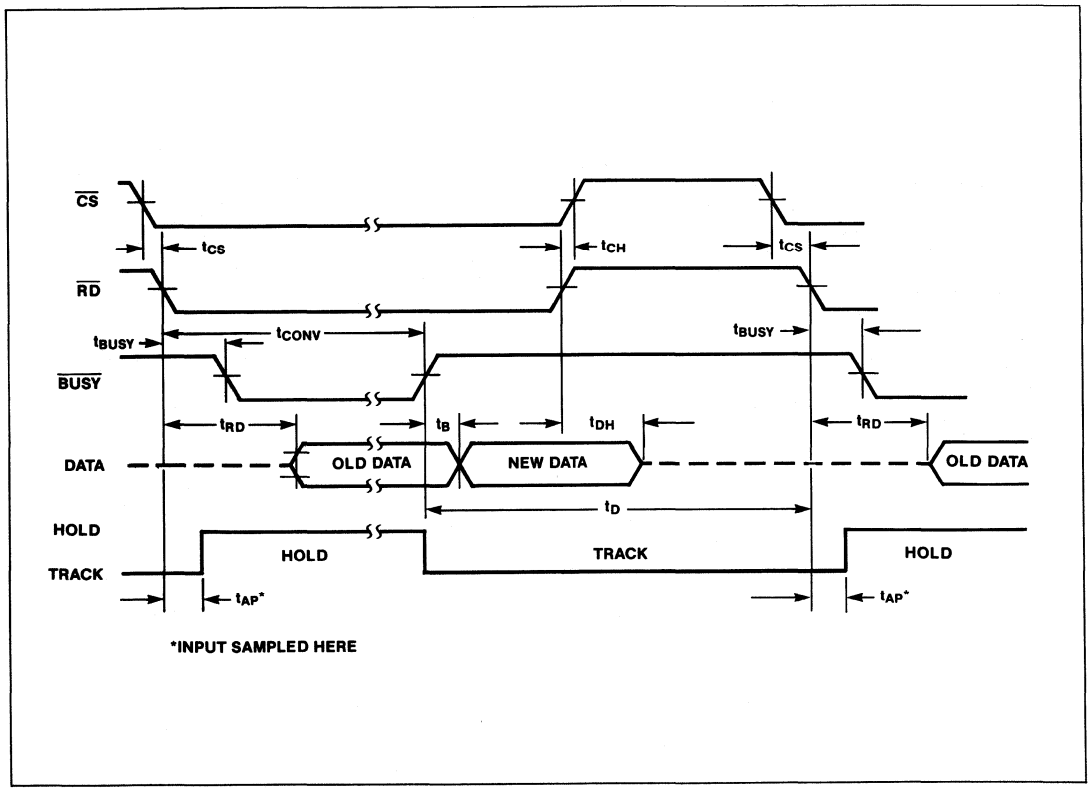


Figure 12. Timing Diagram—Slow Memory Mode

300kHz 10-Bit A/D Converter with Reference and T/H

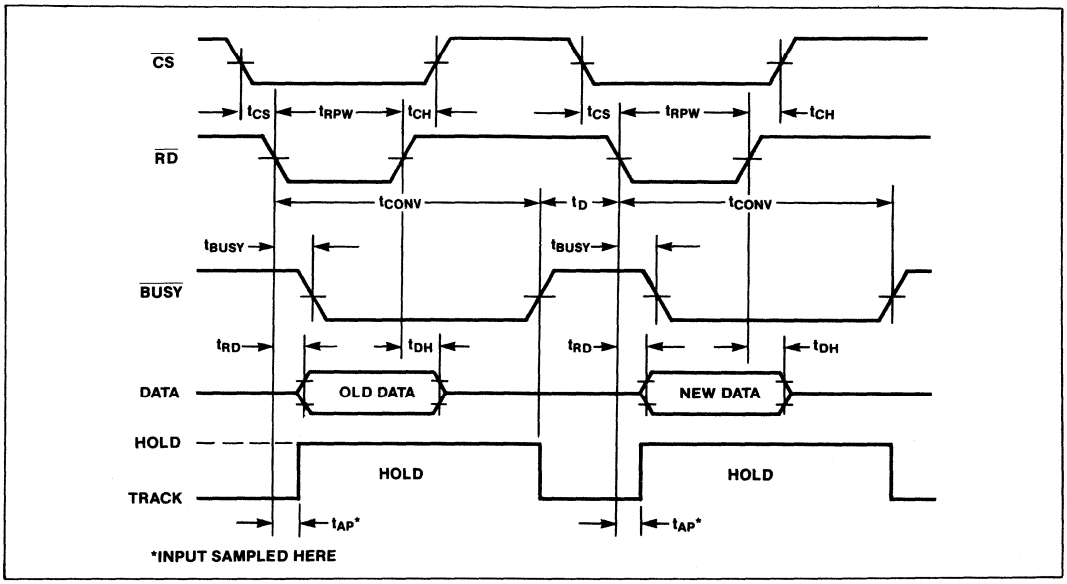


Figure 13. Timing Diagram—ROM Mode

Layout, Grounding and Bypassing

For best system performance, printed circuit boards should be used (wire-wrap boards are not recommended). In layout, separate the digital and analog signal lines as much as possible. Analog and digital lines should not run parallel, and digital lines should not run underneath the ADC package.

Figure 14 shows the recommended power-supply grounding connections. A single-point analog STAR ground should be established at AGND separate from the logic ground. All other analog grounds and DGND should be connected to this STAR ground. No other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

Power supplies should be bypassed to the analog STAR ground with 0.1μF and 10μF bypass capacitors. Capacitor leads should have minimum length for best noise rejection.

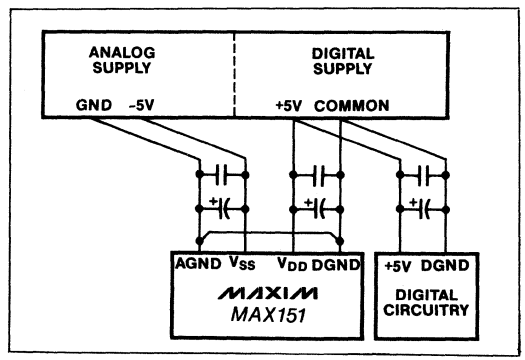


Figure 14. Power-Supply Grounding Practice

Dynamic Performance

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are accepted for specifying performance with DC and slowly varying signals, but less useful in signal processing where the A/D's impact on the system transfer is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

High-speed sampling capability and up to 333 ksamples/sec throughput make the MAX151 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the A/D's dynamic frequency response, distortion and noise at the rated throughput. This involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm to determine spectral content. Conversion errors are seen as spectral elements outside of the fundamental input frequency.

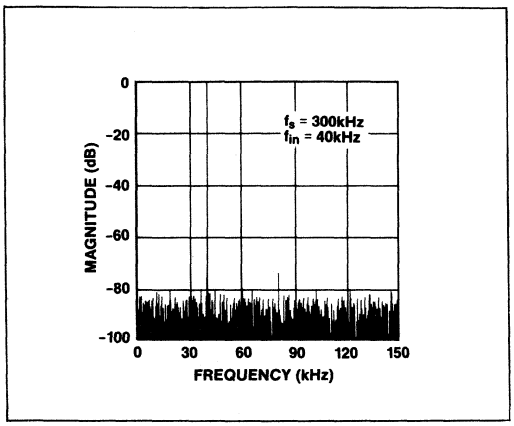


Figure 15. FFT Plot for the MAX151

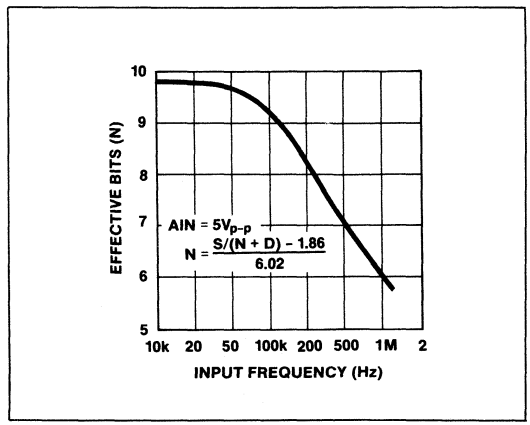


Figure 16. Effective Bits Curve

Signal-to-Noise Ratio and Effective Number of Bits

The ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). This includes distortion and noise components. For this reason, the ratio is also referred to as S/(N + D), or Signal-to-Noise plus Distortion.

The theoretical minimum A/D noise is caused by quantization error and a direct result of the A/D's resolution:

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits of resolution. A perfect 10-bit A/D can do no better than 62dB. Figure 15 shows the result of sampling a pure 40kHz sinusoid at a 300kHz rate. The FFT plot of the output shows the output level in various spectral bands (Figure 15).

By transposing the equation which converts resolution to SNR, the effective resolution or the "Effective Number of Bits" the A/D provides can be determined from the measured SNR:

$$N = (SNR-1.76)/6.02$$

Figure 16 shows the Effective Number of Bits as a function of the input frequency for the MAX151.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20Log[\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... + V_N^2)}/V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through nth harmonics.

Peak Harmonic or Spurious Noise

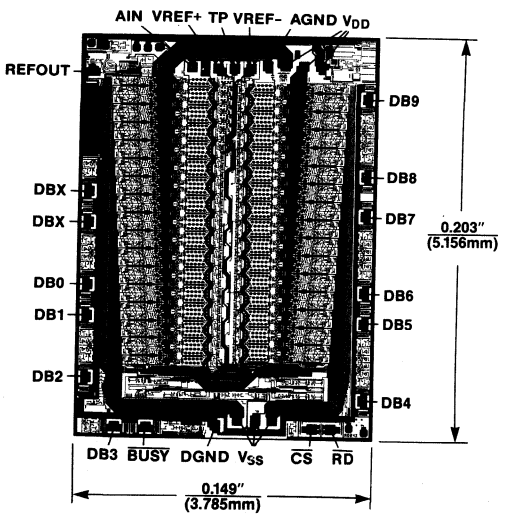
The ratio of the RMS amplitude of the fundamental input frequency to the amplitude of the next largest spectral component is referred to as the Peak Harmonic or Spurious Noise. Usually this peak occurs at some harmonic of the input frequency. But, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Ordering Information (continued)

PART	TEMP.RANGE	PIN-PACKAGE	TUE (LSB)
MAX151AENG	-40°C to +85°C	24 Plastic DIP	1.0
MAX151BENG	-40°C to +85°C	24 Plastic DIP	1.5
MAX151AEWG	-40°C to +85°C	24 Wide SO	1.0
MAX151BEWG	-40°C to +85°C	24 Wide SO	1.5
MAX151AMRG	-55°C to +125°C	24 CERDIP	1.0
MAX151BMRG	-55°C to +125°C	24 CERDIP	1.5

300kHz 10-Bit A/D Converter with Reference and T/H

Chip Topography



ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

400ns µP-Compatible, 8-Bit ADC with Track/Hold

General Description

The MAX153 high-speed, microprocessor-compatible (µP), 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 400ns conversion time. The device has a 100kHz input-signal bandwidth, and a V_{SS} pin supports dual power supplies and bipolar inputs. A $\overline{\text{POWER DOWN}}$ pin reduces current consumption to less than 100µA

The MAX153's track-and-hold (T/H) function capable of digitizing a 2MHz signal, and is static and dynamically tested. The converter-µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Features

- ♦ **400ns Conversion Time**
- ♦ **20-Pin Narrow DIP Package**
- ♦ **No External Clock**
- ♦ **100kHz Input Signal Bandwidth**
- ♦ **Bipolar/Unipolar Inputs**
- ♦ **Single/Dual +5V Supplies**
- ♦ **Ratiometric Reference Inputs**
- ♦ **Static and Dynamically Tested**
- ♦ **$\overline{\text{POWER DOWN}}$**
- ♦ **Internal Track/Hold**

Applications

Digital-Signal Processing

High-Speed Data Acquisition

Telecommunications

High-Speed Servo Loops

Audio Systems

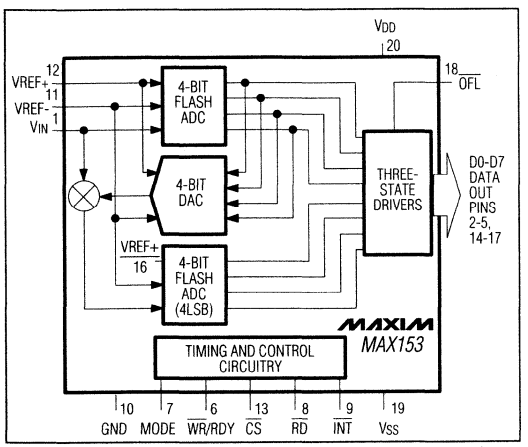
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX153CPP	0°C to +70°C	20 Plastic DIP
MAX153CWP	0°C to +70°C	20 Wide SO
MAX153CQP	0°C to +70°C	20 PLCC
MAX153C/D	0°C to +70°C	Dice*
MAX153EPP	-40°C to +85°C	20 Plastic DIP
MAX153EWP	-40°C to +85°C	20 Wide SO
MAX153MLP	-55°C to +125°C	20 LCC**
MAX153MJP	-55°C to +125°C	20 CERDIP**

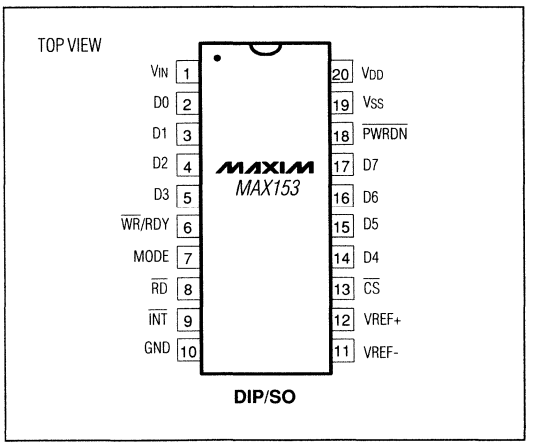
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Block Diagram



Pin Configurations



MAXIM

High-Speed, 8-Bit ADCs with 8/4 Simultaneous T/Hs and Reference

General Description

The MAX155/MAX156 are high-speed, multi-channel 8-bit analog-to-digital converters (ADC) with simultaneous Track-and-Hold (T/H) and 8 x 8 dual-port RAM. The MAX155 has 8 analog input channels, and the MAX156 has 4 analog input channels. Each channel has a separate T/H that holds the signal for the internal ADC. The ADC converts each channel in 3.6µs and stores the result in the RAM. The MAX155/MAX156 also feature a 2.5V on-chip reference, forming a complete high-speed data acquisition system.

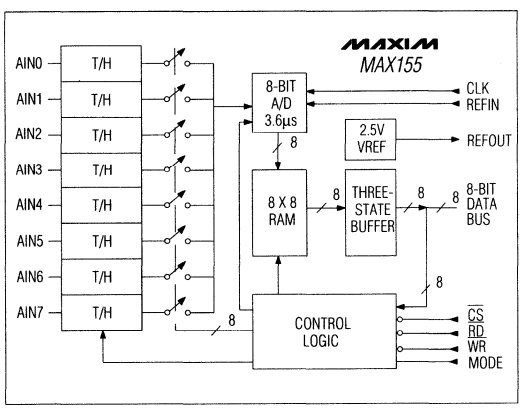
These devices can be used with a single 5V supply and perform unipolar or bipolar conversions with single-ended or differential inputs. For applications where an extended input range or bipolar conversion about ground is important, an optional negative supply pin (labeled V_{SS}) is provided.

Conversions are initiated with a $\overline{WR}$ pulse, and data is accessed with a $\overline{RD}$ pulse. Bidirectional Input/Output pins can be used to update the chip's command register. Hard-wired modes of operation, which bypass the command register, are also provided.

Applications

Digital Oscilloscope
Vibration Analysis
Input for DSP
Digital-Strip Chart Recorder
High-Speed Phase-Sensitive Data Acquisition

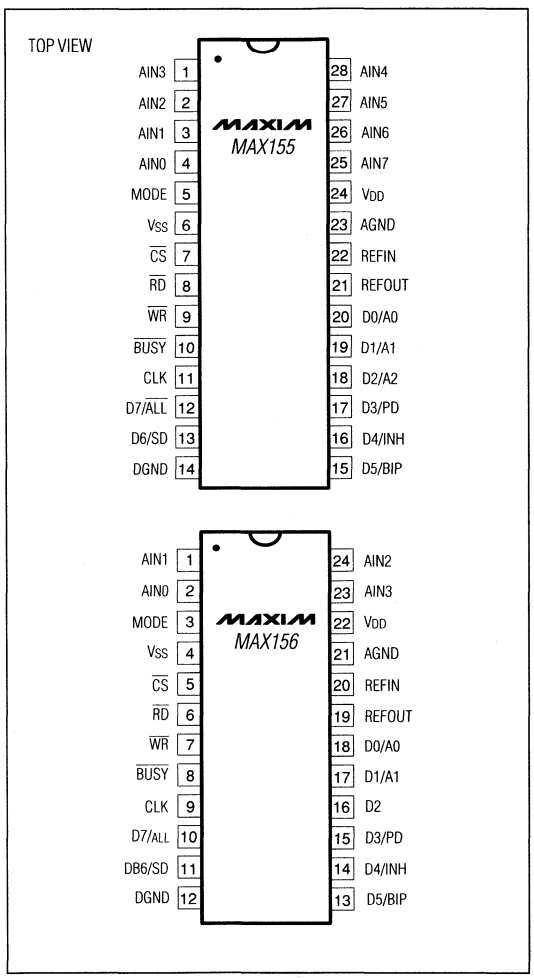
Functional Diagram



Features

- ♦ One-Chip Data Acquisition System
- ♦ 8 or 4 Analog Input Channels
- ♦ Single-Ended or Differential Inputs
- ♦ Simultaneous T/H
- ♦ 3.6µs Conversion Time per Channel
- ♦ On-Chip 8 x 8 Dual-Port RAM
- ♦ Internal 2.5V Reference
- ♦ Single +5V Supply Operation

Pin Configurations



7

Complete High-Speed CMOS 12-Bit ADC

General Description

The MAX162 and MX7572 are complete 12-Bit analog-to-digital converters (ADC's) that combine high speed, low power consumption, and an on-chip voltage reference. The conversion times are 3μs (MAX162) and 5 and 12μs (MX7572). The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX162/MX7572 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

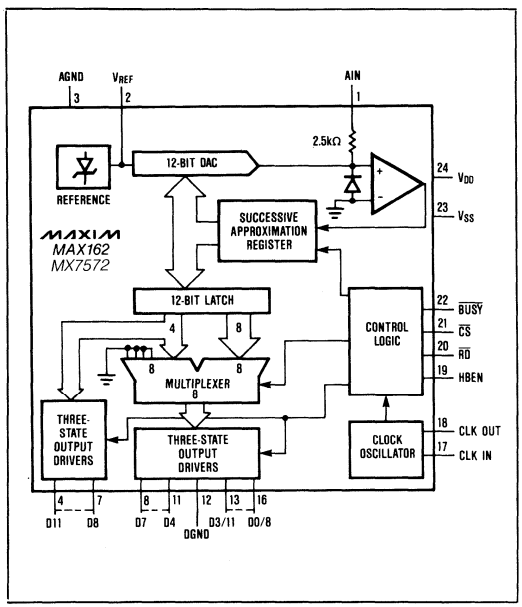
Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Functional Diagram



Features

- **12-Bit Resolution and Linearity**
- **3μs (MAX162), 5μs and 12μs (MX7572) Conversion Times**
- **No missing Codes**
- **On-Chip Voltage Reference**
- **90ns Access Time**
- **215mW Max Power Consumption**
- **24-Lead Narrow DIP Package**

Ordering Information

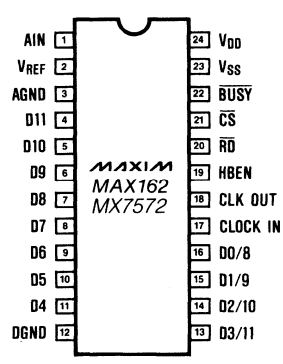
PART	TEMP. RANGE	PACKAGE*	ERROR
3μs CONVERSION TIME			
MAX162ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX162BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX162BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CC/D	0°C to +70°C	Dice**	±1 LSB
MAX162AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX162BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162CING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX162BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX162CMRG	-55°C to +125°C	CERDIP	±1 LSB

* *All devices — 24 lead packages*

** *Consult factory for dice specifications*

Ordering Information continued on last page.

Pin Configuration



Complete High-Speed CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX162XC, MX7572JN, KN, LN,
JCWG, KCWG, LCWG ..... 0°C to +70°C
MAX162XI, MX7572AQ, BQ, CQ ..... -25°C to +85°C
MAX162XM, MX7572SQ, TQ, UQ .... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -15V ±5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for MX7572XX05 and 1MHz for MX7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX162A, MX7572L/C/U	T_A = 25°C			±1/2	LSB
		MAX162AC, AI, MX7572L/C MAX162AM, MX7572U MAX162B/C, MX7572K/B/T/J/A/S				±1/2 ±3/4 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX162C, MX7572J/A/S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±6	LSB
		MAX162B, MX7572K/B/T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±3 ±5	LSB
		MAX162A, MX7572L/C/U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±3 ±4	LSB
Full Scale Error (Note 2)		MAX162C, MX7572J/A/S	T_A = 25°C			±15	LSB
		MAX162B, MX7572K/B/T	T_A = 25°C			±10	LSB
		MAX162A, MX7572L/C/U	T_A = 25°C			±10	LSB
Full Scale Tempco (Notes 3, 4)		MAX162C, MX7572J/A/S MAX162B/A, MX7572K/B/T, MX7572L/C/U				±45 ±25	ppm/°C
ANALOG INPUT							
Input Voltage Range		For Bipolar Input see Figures 19-21		0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)		MAX162C, MX7572J/A/S MAX162B/A, MX7572K/B/T, MX7572L/C/U			40 20		ppm/°C
Output Current Sink Capability		(Note 6)				500	µA

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ±5%, V_{SS} = -15V ±5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for MX7572XX05 and 1MHz for MX7572XX12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75 to 5.25V		±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V MAX162/MX7572 V_{SS} = -14.25V to -15.75V MAX162 V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB LSB
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN	2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN			10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN; VIN = 0 to V_{DD}			±10 ±20	µA
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200µA	4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}			±10	µA
Floating State Output Capacitance (Note 7)	C_{OUT}				15	pF
CONVERSION TIME						
MAX162	tCONV	f_{CLK} = 4MHz; Synchronous (13 clock cycles); Asynchronous (12 to 13 clock cycles)	3		3.25 3.25	µs
MX7572XX05	tCONV	f_{CLK} = 2.5MHz; Synchronous (12.5 clock cycles); Asynchronous (12 to 13 clock cycles)	4.8		5 5.2	µs
MX7572XX12	tCONV	f_{CLK} = 1MHz; Synchronous (12.5 clock cycles); Asynchronous (12 to 13 clock cycles)	12		12.5 13	µs
POWER REQUIREMENTS						
V_{DD}		±5% for Specified Performance	4.75	5	5.25	V
V_{SS} (Note 8)		±5% MAX162 ±5% MX7572		-12 or -15 -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1LSB
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS -3/2LSB
Note 3: Full Scale TC = $\Delta FS/\Delta T$, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: V_{SS} = -12V ±5% for the MAX162 only. Functional operation is guaranteed by testing offset error and full scale error.

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TIMING CHARACTERISTICS (Note 9)

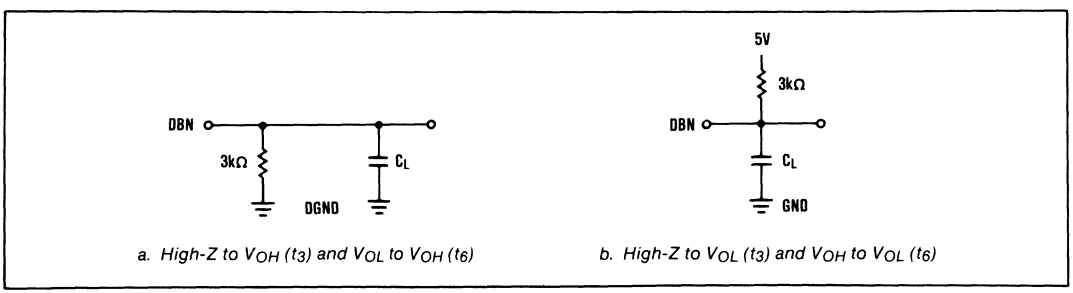
(V_{DD} = +5V, V_{SS} = -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX162C/I MX7572J/K/L MX7572A/B/C		MAX162M MX7572S/T/U		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

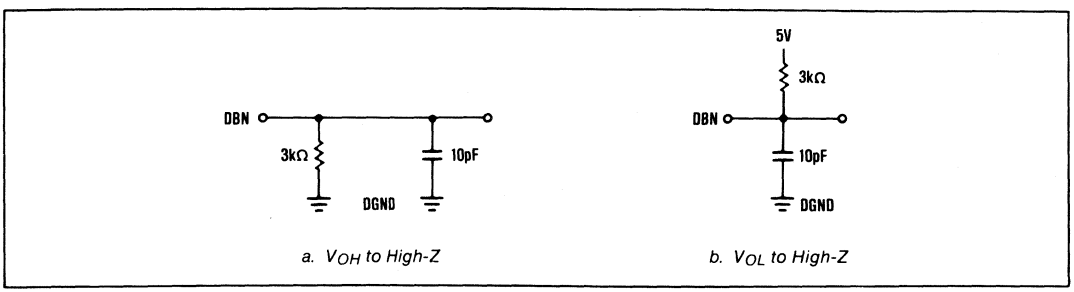
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

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Pin Description

PIN	NAME	FUNCTION
1	AIN	Analog Input, 0 to +5V unipolar input
2	V_{REF}	-5.25V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLKIN	Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. An inverted CLKIN signal appears at this pin.

PIN	NAME	FUNCTION
19	HBEN	High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.
22	$\overline{BUSY}$	The BUSY Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V for MX7572 and -15V or -12V for MAX162.
24	V_{DD}	Positive Supply, +5V.

Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note:
* D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

Converter Operation

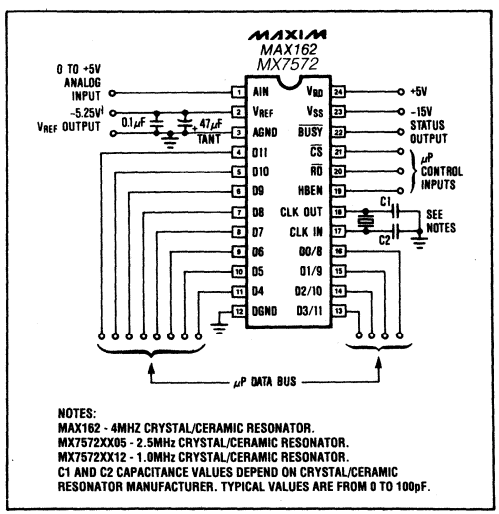

Figure 3. MAX162/MX7572 Operational Diagram

The MAX162 and MX7572 use a successive approximation technique to convert an unknown analog input to a 12 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 3 shows the MAX162/MX7572 in its simplest operational configuration.

Figure 4 shows the MAX162/MX7572analog equivalent circuit. The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero crossing detector and its output is fed back to the SAR input.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN digital inputs. A conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN is low. Once started, conversion cannot be stopped. The $\overline{BUSY}$ output goes low as soon as the conversion starts. $\overline{BUSY}$ may be used to control an external sample-and-hold when wide bandwidth input signals are being measured.

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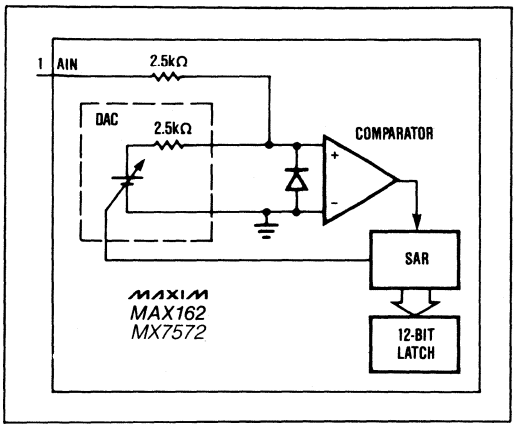


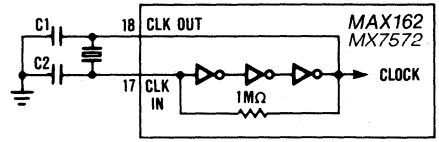
Figure 4. MAX162/MX7572 Analog Equivalent Circuit

The SAR is set to half scale as soon as the $\overline{CS}$ and $\overline{RD}$ inputs go low. This reset is asynchronous with the clock input. The analog input is then compared to one half of the full scale voltage. About 30ns after the second falling edge of CLKIN (or rising edge of CLKOUT), the output of the comparator is latched into the SAR MSB bit (see Figure 5). The bit is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (bit 11) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. Following a falling CLKIN signal, the BUSY output goes high and the SAR result is latched into the three-state output buffers.

Clock Operation

Clock Oscillator

Figure 6 shows the MAX162/MX7572 clock circuitry. The capacitive load on the CLKOUT pin must be minimized for low power dissipation and to avoid digital coupling of the CLKOUT buffer currents to the comparator. If an external clock source is being used to drive CLKIN, CLKOUT should be left open. The external clock source must have a 50% duty cycle. If the internal oscillator is being used, a crystal/ceramic resonator should be connected between CLKOUT and CLKIN as shown in Figure 6.



NOTES:
MAX162 - 4MHZ CRYSTAL/CERAMIC RESONATOR.
MX7572XX05 - 2.5MHz CRYSTAL/CERAMIC RESONATOR.
MX7572XX12 - 1.0MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 0 TO 100pF.

Figure 6. MAX162/MX7572 Internal Clock Circuit

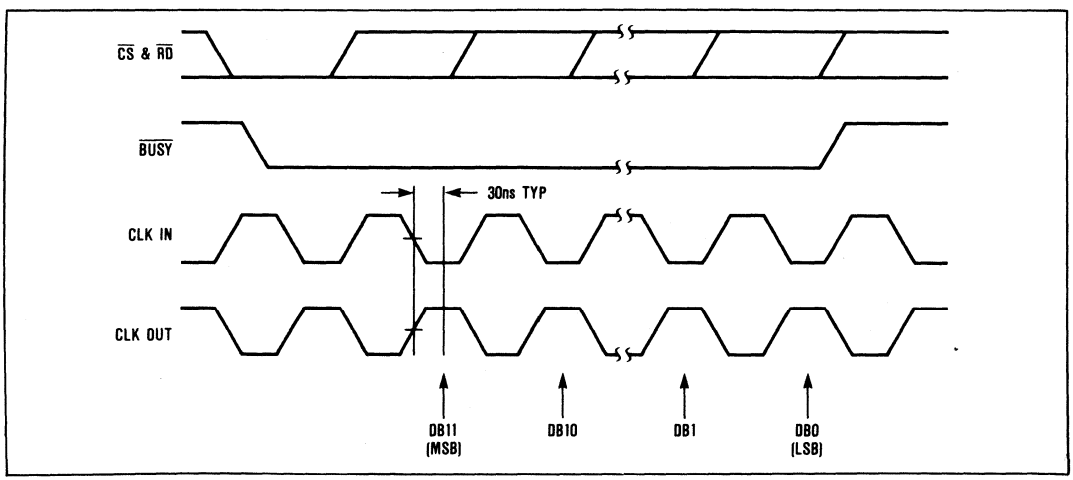


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN.

Control Input Synchronization

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). To ensure a fixed conversion time use the following guidelines for synchronization:

MAX162

For the MAX162 the $\overline{RD}$ input should go low at the falling edge of CLKIN. In this case the conversion lasts 13 clock cycles and the conversion time is 3.25μs when f_{CLK} = 4MHz. If the CLKIN and $\overline{RD}$ falling edges are skewed, the skew must not be more than 50ns to ensure the 13 period conversion time (See Figure 7). The MSB is tried at the second clock falling edge, leaving two clock cycles for the external sample-and-hold to settle from hold transients.

MX7572

The MX7572 $\overline{RD}$ input can go low at the rising edge of CLKIN. In this case the conversion lasts 12.5 clock cycles and the conversion time is 5μs when f_{CLK} = 2.5MHz and 12.5μs when f_{CLK} = 1MHz. The delay from the falling edge of $\overline{RD}$ to the falling edge of CLKIN must not be less than 180ns to ensure the 12.5 clock cycle conversion time (See Figure 8). This leaves the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional half clock cycle of settling can be allowed for driving the sample-and-hold by having $\overline{RD}$ go low at the falling edge of CLKIN, similar to the MAX162. This results in a 13 cycle conversion time (5.2μs when f_{CLK} = 2.5MHz, 13μs when f_{CLK} = 1MHz).

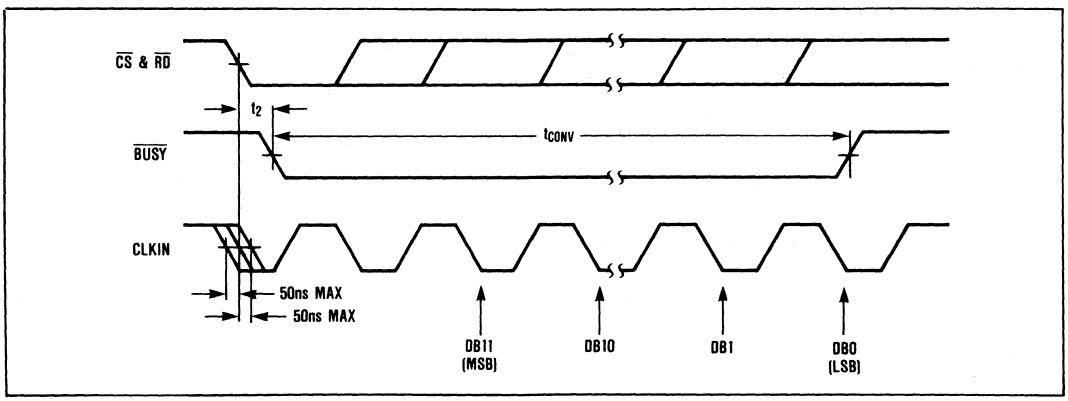


Figure 7. MAX162 $\overline{RD}$ and CLKIN For Synchronous Operation

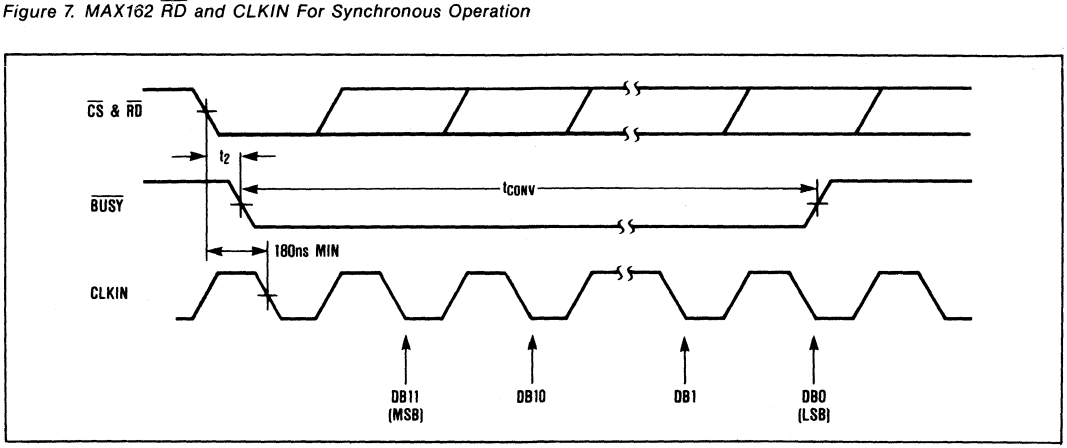


Figure 8. MX7572 $\overline{RD}$ and CLKIN For Synchronous Operation

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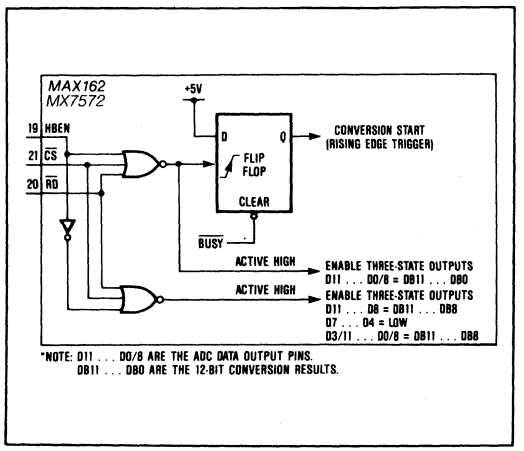

Figure 9. Logic Equivalent for $\overline{RD}$, $\overline{CS}$ and HBEN Inputs

Digital Interface

Output Data Format

The 12 output data bits can either be presented full parallel or in two 8 bit words. To obtain parallel output for 16 bit processors, HBEN should be kept low and the output data D11-D0 will be right justified.

For a two byte data read, outputs D7-D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented with the leading 4 bits being low for D7-D0/8.

Note that the 4 MSB's always appear at digital outputs D11-D8 whenever the digital drivers are enabled, regardless of the state of HBEN.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs; HBEN, CS and RD. Figure 9 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion. Once a conversion is in progress, it cannot be re-started. The BUSY output is low during the entire conversion cycle.

There are two modes of operation as outlined in the timing diagrams of Figures 10-13. Slow memory mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX162/MX7572 conversion time. ROM mode is for processors that cannot be forced into a wait state. In both operational modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation is required to access the conversion result.

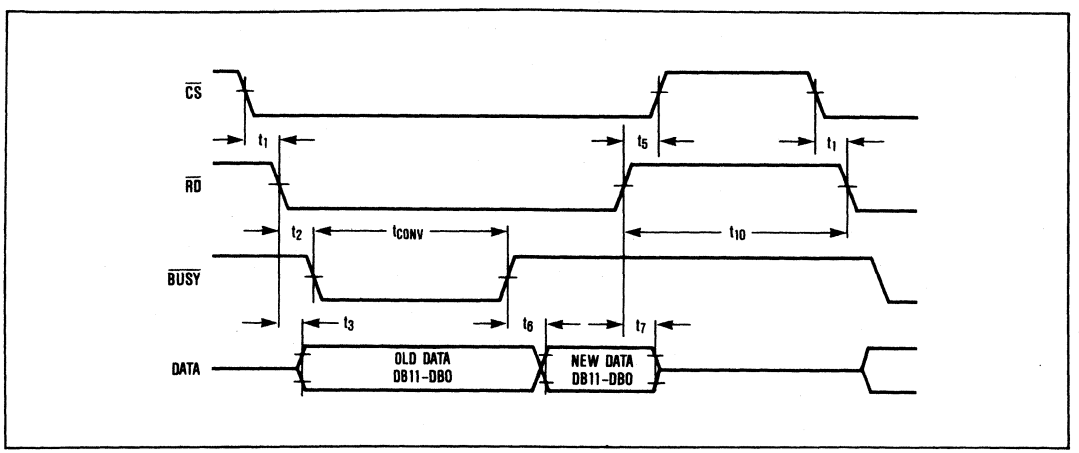

Figure 10. Slow Memory Mode, Parallel Read Timing Diagram

Table 1. Slow Memory Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

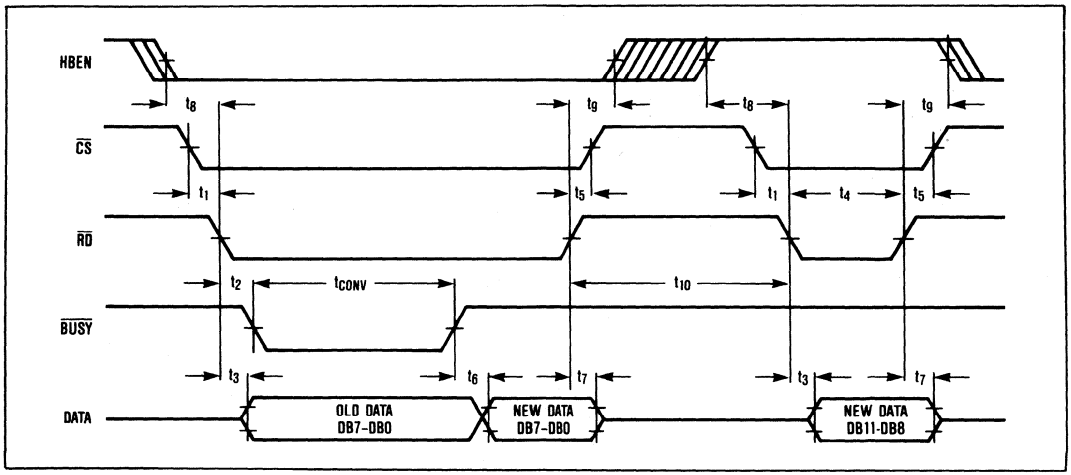

Figure 11. Slow Memory Mode, Two Byte Read Timing Diagram

Table 2. Slow Memory Mode, Two Byte Read Data Bus Status

MAX162/MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

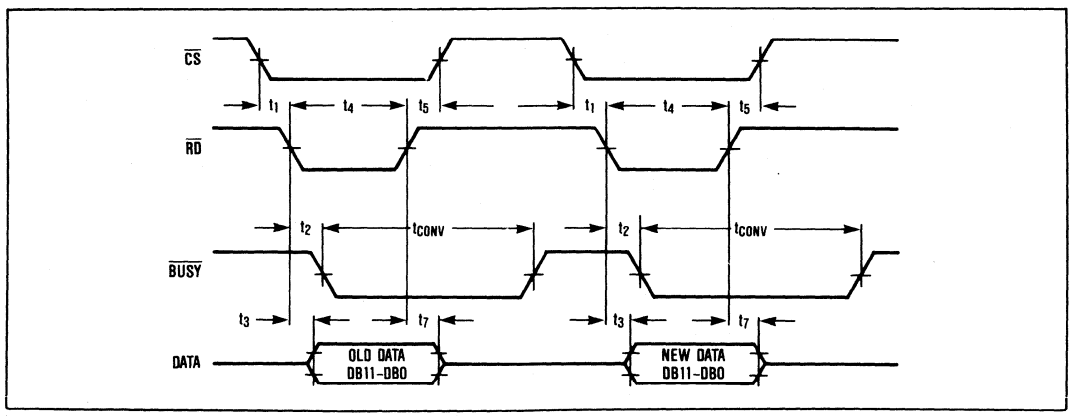

Figure 12. ROM Mode, Parallel Read Timing Diagram

Table 3. ROM Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

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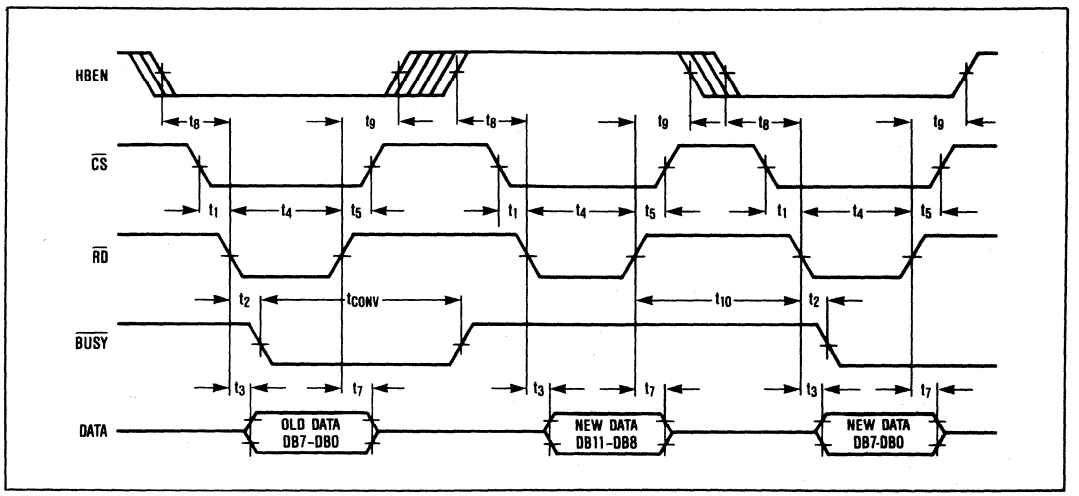

Figure 13. ROM Mode, Two Byte Read Timing Diagram

Table 4. ROM Mode, Two Byte Read Data Bus Status

MAX162/MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 10 and Table 1 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. CS and RD going low starts the conversion and BUSY goes low indicating that the conversion is in progress. Data from the previous conversion appears at the digital outputs. At the end of the conversion, BUSY returns high and the output latches are updated to place the digital conversion result on data outputs D11-D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only outputs D7-D0/8 are used. Starting the conversion and reading the 8 LSB's is identical to the Slow Memory Mode, Parallel Read. See Figure 11 and Table 2. A second READ operation with HBEN high places the 4 MSB's with 4 leading zeros on the data outputs D7-D0/8. The high byte read does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM mode avoids placing the processor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion appears at the data outputs D11-D0/8 (see Figure 12 and Table 3). This data may be disregarded if not needed. A second READ operation will access the results of the first operation and also start a new conversion. The delay between successive READ operations must be longer than the conversion time for the MAX162/MX7572.

ROM Mode, Two Byte Read

As in the Slow Memory Mode, only data outputs D7-D0/8 should be used for two byte reads. Figure 13 and Table 4 show the operation in this mode. A conversion is started with a READ operation with HBEN low. The data outputs present the 8 LSB's from the previous conversion and this data can be disregarded if not required. Two more READ operations are needed to access the conversion result. The first READ must be with HBEN high, where the 4 MSB's with 4 leading zero's are accessed. The second READ is with HBEN low, which reads in the 8 LSB's and starts a new conversion.

Interface Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, LSBs of error can be caused due to coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

ROM Mode

Considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a decision to keep or drop a bit. To avoid this problem, RD and CS should be active for less than one clock cycle. In other words, the RD and CS low pulse should be shorter than 250ns for the MAX162, 400ns for the MX7572XX05 and 1μs for the MX7572XX12. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN, since the comparator output is always latched at falling edges of CLKIN.

Analog Considerations

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX162/MX7572. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX162/MX7572 package.

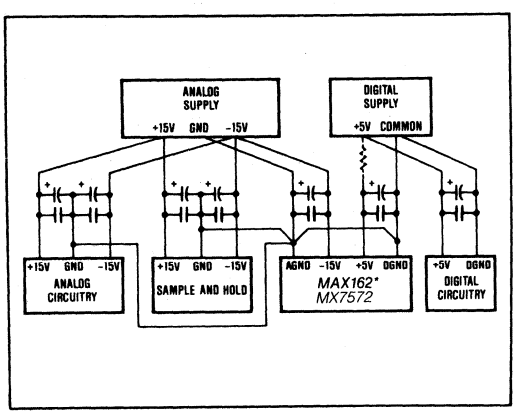

Figure 14. Power Supply Grounding Practice

Grounding

Figure 14 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 3 (AGND) of the MAX162/MX7572 separate from the logic ground. All other analog grounds and pin 12 (DGND) of the MAX162/MX7572 should be connected to this STAR ground and no other digital grounds should be connected to this STAR point. The ground return to the power supply from this STAR ground should be low impedance for noise free operation of the ADC.

Power Supply Bypassing

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1μF and 10μF by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10-20 ohms) resistor can be connected as shown in Figure 14 to filter external noise.

Internal Reference

The MAX162/MX7572 has an internal buried zener reference which provides the DAC reference voltage. The reference voltage is -5.25V ±1% and has a low temperature coefficient. The reference output is available at pin 2, and should be bypassed to analog ground (pin 3) with a 47μF tantalum capacitor in parallel with 0.1μF capacitor to minimize noise and provide low impedance at high frequencies. This by-pass capacitor must not be less than 4.7μF. The internal reference output buffer can sink upto 500μA.

Driving The Analog Input

The input signal leads to AGND and AIN should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion (4MHz for MAX162 and 2.5 or 1MHz for the MX7572). The output impedance of the driving amplifier is equal to its open loop output impedance divided by the loop gain at the frequency of interest.

MX7572 The MX7572 maximum clock rate of 2.5MHz makes it possible to drive it with amplifiers like the OP-42, AD711 or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

MAX162 The MAX162 with a maximum 4MHz clock rate might cause settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a OP-42, AD711 or OP-27 can be used to improve high frequency output impedance.

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MAX162/MX7572 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX162. For higher bandwidth signals a sample-and-hold should be used.

The $\overline{BUSY}$ output from the MAX162/MX7572 may be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the BUSY signal goes low, the switching transients at the output of the sample-and-hold caused by the DAC switching may result in code dependent errors due to the aperture delay of the sample-and-hold. A NAND gate may be used to ensure that the sample-and-hold switches to the hold mode BEFORE any disturbances as shown in Figures 15 & 16. The NAND gate solution works only if the width of the $\overline{RD}$ pulse is wider than the $\overline{RD}$ to BUSY delay in the MAX162/MX7572. If this is not the case, use a flip flop which is set by the falling edge of $\overline{RD}$ and reset by the rising edge of BUSY.

For synchronous $\overline{RD}$ and CLKIN as described above, the hold settling time allowed for the sample-and-hold is 500ns, 600ns and 1.5μs for the MAX162, MX7572XX05 and MX7572XX12 respectively.

To achieve the maximum sampling rate, the MAX162/MX7572 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

MX7572 Figure 15 shows an AD585 sample-and-hold to MX7572 interface. The MX7572 RD input and BUSY output are used to put the AD585 in hold mode when a conversion is in progress. In this example the analog input range is ±2.5V but other voltage ranges can be configured differently as explained later.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3μs sample-and-hold acquisition time.

Although this circuit works quite well for the 1MHz clock rate, at the 2.5MHz clock rate a faster sample-and-hold amplifier such as the HA-5320 is recommended.

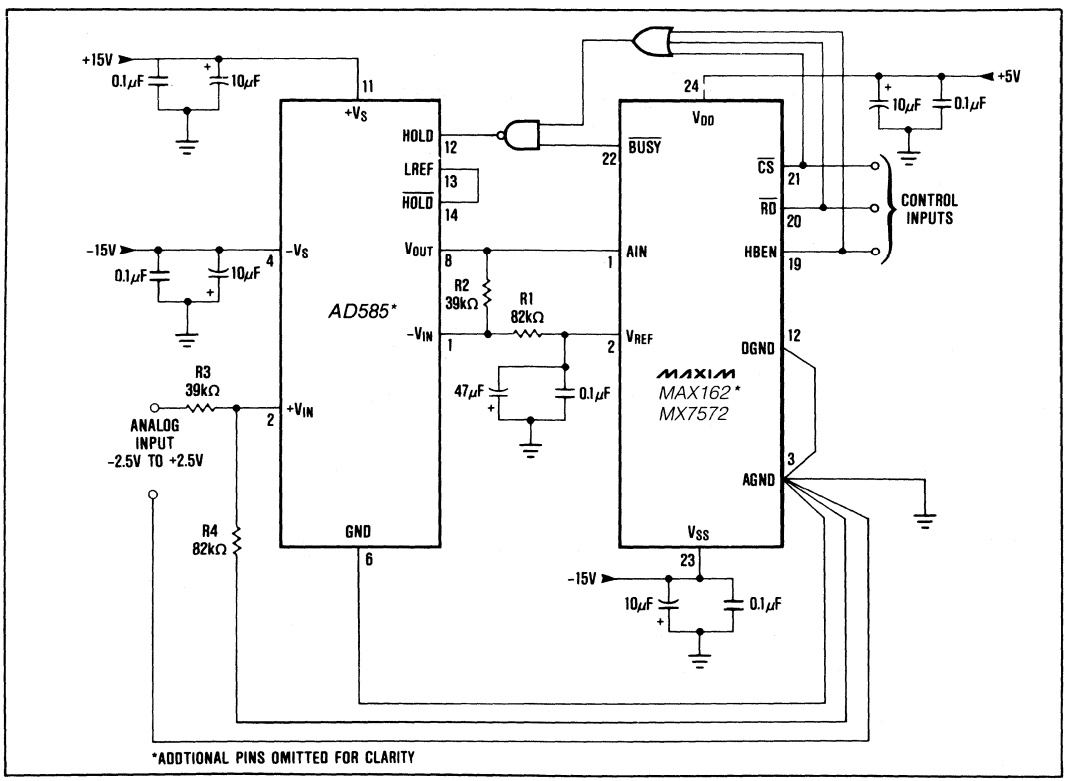


Figure 15. MX7572—AD585 Sample-and-Hold Interface

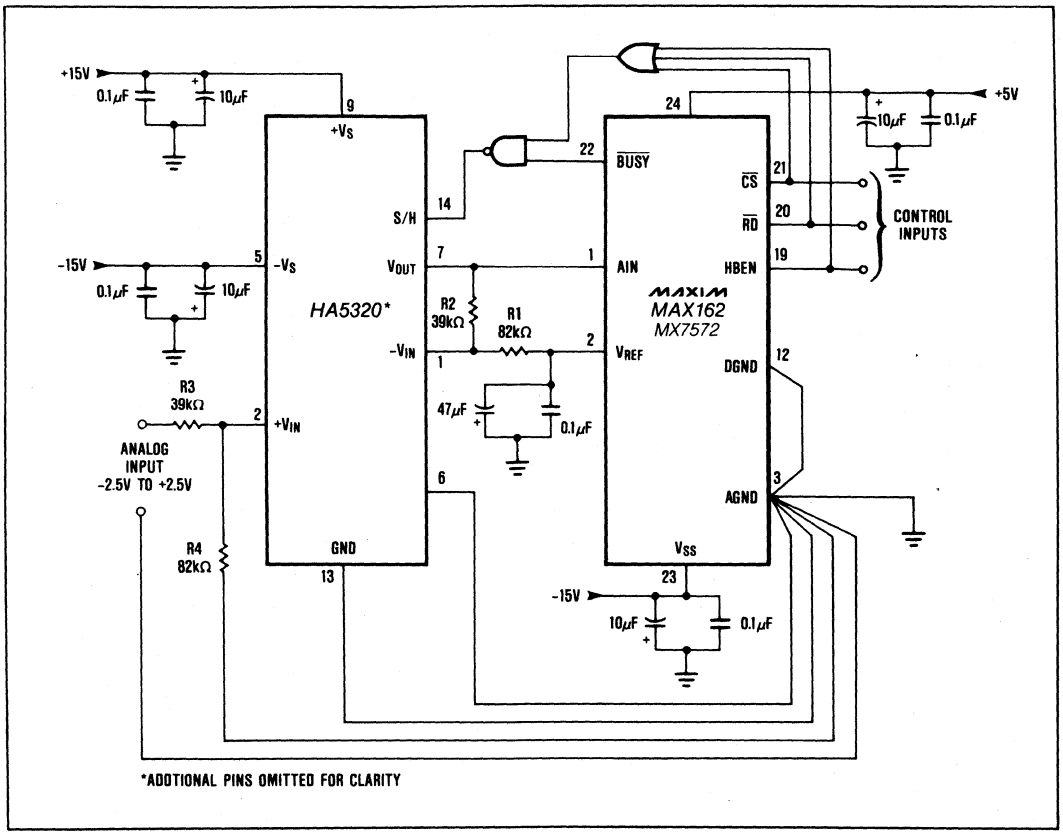


Figure 16. MAX162/MX7572—HA5320 Sample-and-Hold Interface

MAX162 Figure 16 shows the MAX162 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock which allows for a 1.5µs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Unipolar Input Operation

Figure 17 shows the nominal input/output transfer function of the MAX162/MX7572 Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 18. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS-3/2LSB (4.99817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 5 and 6.

Complete High-Speed CMOS 12-Bit ADC

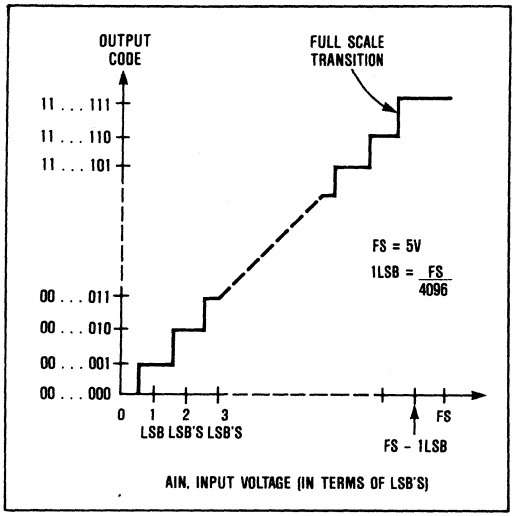


Figure 17. MAX162/MX7572 Transfer Function

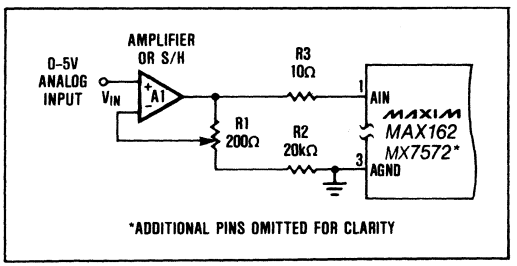


Figure 18. Full-Scale Adjustment

Figure 19 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 20 shows the ideal transfer function for this mode.

Figure 21 shows the bipolar operation in the inverting mode, where the output coding is complementary offset binary. Figure 20 shows the ideal transfer function for the circuit in Figure 21.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

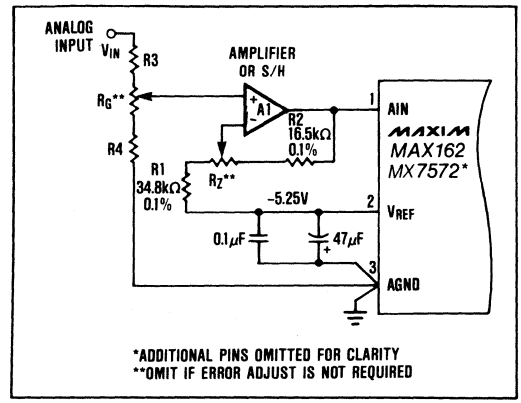


Figure 19. MAX162/MX7572 Non-inverting Bipolar Operation

Table 5. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 19

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

Notes:
* R3 and R4 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

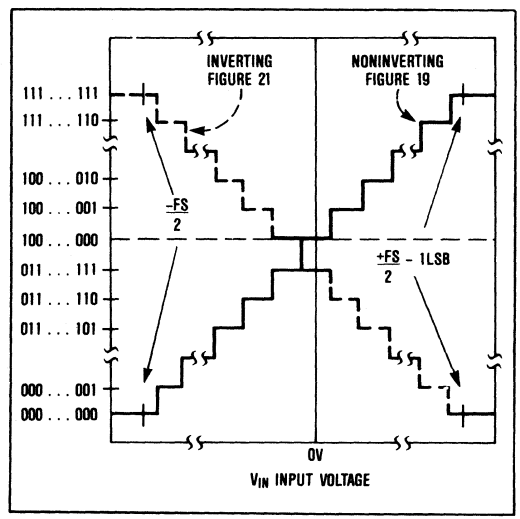


Figure 20. Ideal Input/Output Transfer Characteristic for the Bipolar circuits in Figures 19 and 21.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see tables 5 and 6) and adjust R_Z until the output code flickers between the following codes:

For Non-inverting (Figure 19)	1000 0000 0000 1000 0000 0001
For inverting (Figure 21)	0111 1111 1111 0111 1111 1110

Apply FS-3/2LSB (see tables 5 and 6) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 19)	1111 1111 1110 1111 1111 1111
For inverting (Figure 21)	0000 0000 0001 0000 0000 0000

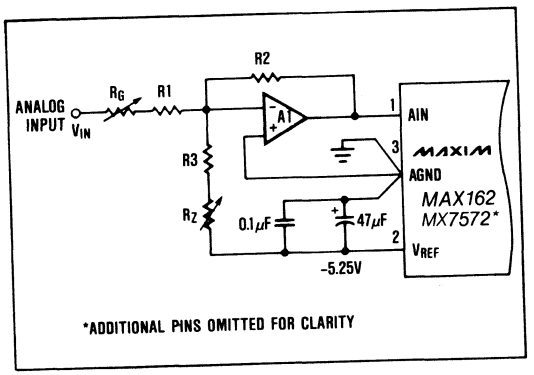


Figure 21. MAX162/MX7572 Inverting Bipolar Operation

Chip Topography

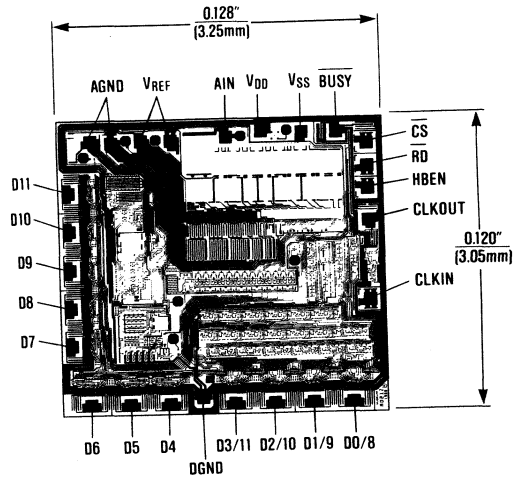


Table 6. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 21

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

Notes:
* R1, R2, and R3 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

Complete High-Speed CMOS 12-Bit ADC

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
5μs CONVERSION TIME			
MX7572JN05	0°C to +70°C	Plastic DIP	±1 LSB
MX7572KN05	0°C to +70°C	Plastic DIP	±1 LSB
MX7572LN05	0°C to +70°C	Plastic DIP	±½ LSB
MX7572JCWG05	0°C to +70°C	Wide S.O.	±1 LSB
MX7572KCWG05	0°C to +70°C	Wide S.O.	±1 LSB
MX7572LCWG05	0°C to +70°C	Wide S.O.	±½ LSB
MX7572AQ05	-25°C to +85°C	CERDIP	±1 LSB
MX7572BQ05	-25°C to +85°C	CERDIP	±1 LSB
MX7572CQ05	-25°C to +85°C	CERDIP	±½ LSB
MX7572SQ05	-55°C to +125°C	CERDIP	±1 LSB
MX7572TQ05	-55°C to +125°C	CERDIP	±1 LSB
MX7572UQ05	-55°C to +125°C	CERDIP	±½ LSB
12μs CONVERSION TIME			
MX7572JN12	0°C to +70°C	Plastic DIP	±1 LSB
MX7572KN12	0°C to +70°C	Plastic DIP	±1 LSB
MX7572LN12	0°C to +70°C	Plastic DIP	±½ LSB
MX7572JCWG12	0°C to +70°C	Wide S.O.	±1 LSB
MX7572KCWG12	0°C to +70°C	Wide S.O.	±1 LSB
MX7572LCWG12	0°C to +70°C	Wide S.O.	±½ LSB
MX7572AQ12	-25°C to +85°C	CERDIP	±1 LSB
MX7572BQ12	-25°C to +85°C	CERDIP	±1 LSB
MX7572CQ12	-25°C to +85°C	CERDIP	±½ LSB
MX7572SQ12	-55°C to +125°C	CERDIP	±1 LSB
MX7572TQ12	-55°C to +125°C	CERDIP	±1 LSB
MX7572UQ12	-55°C to +125°C	CERDIP	±½ LSB

** All devices — 24 lead packages*

MAXIM

CMOS 12-Bit A/D Converters With Track-and-Hold

General Description

The MAX163, MAX164, and MAX167 are complete CMOS sampling 12-bit analog-to-digital converters (ADCs) that combine an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33μs includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

The three A/Ds differ only in their analog input range. The MAX163 accepts 0V to +5V inputs, the MAX164 accepts -5V to +5V inputs, and the MAX167's input range is -2.5V to +2.5V. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX163/164/167 employ a standard microprocessor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

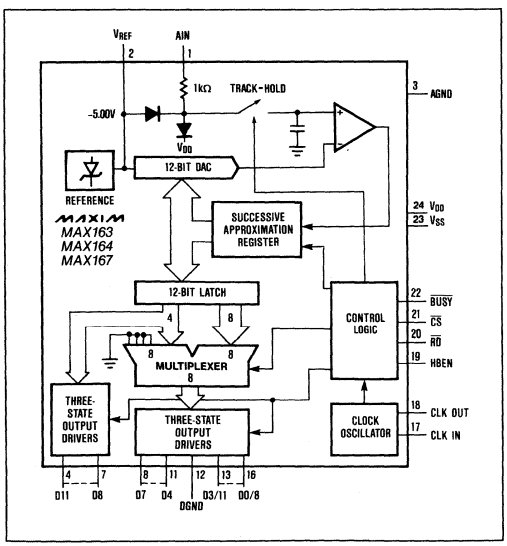
Digital Signal Processing (DSP)

Audio and Telecom Processing

High Accuracy Process Control

High Speed Data Acquisition

Functional Diagram



Features

- ♦ 12-Bit Resolution
- ♦ 8.33μs Conversion Time
- ♦ Internal Analog Track-Hold
- ♦ 6MHz Full Power Bandwidth
- ♦ On-Chip Voltage Reference
- ♦ High Input Resistance (500MΩ)
- ♦ 100ns Data Access Time
- ♦ 180mW (Max) Power Consumption
- ♦ AD7572/MAX162/MAX172 Plug-In Replacement
- ♦ 24 Lead Narrow DIP and SO Packages

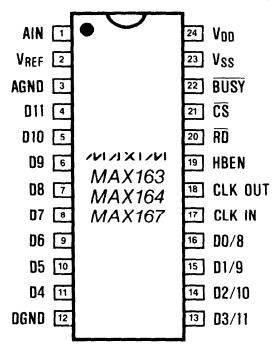
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX167BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX167CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX167ACWG	0°C to +70°C	Wide SO	±½ LSB
MAX167BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX167CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX167AEWG	-40°C to +85°C	Wide SO	±½ LSB
MAX167BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX167CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX167CC/D	0°C to +70°C	Dice**	±1 LSB
MAX167AENG	-40°C to +85°C	Plastic DIP	±½ LSB

** All devices—24 lead packages*
***Consult factory for dice specifications*
Ordering information continued on last page.

Pin Configuration

Top View



7

CMOS 12-Bit A/D Converters With Track-and-Hold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3 to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD} +0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V to V_{DD} +0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V to V_{DD} +0.3V
(Pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX16XXC ..... 0°C to +70°C
MAX16XXE ..... -40°C to +85°C
MAX16XXM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode (see text), T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.6MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX16XB, MAX16XC MAX167A				±1 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temperature				±1	LSB
Offset Error (Note 1)		MAX163 MAX164, MAX167				±4 ±6	LSB
Full Scale Error (Note 2)		T_A = 25°C, Includes Reference Error				±10	LSB
Full Scale Tempco (Notes 3, 5)		Excludes Internal Reference Drift				±5	ppm/°C
Conversion Time	t_{CONV}	Synchronous (12.5 Clock Cycles) (13 Clock Cycles)				7.81 8.13	µs
Clock Frequency	f_{CLK}			0.1		1.6	MHz
DYNAMIC ACCURACY (Sample Rate = 100kHz)							
Signal to Noise plus Distortion Ratio	S/(N+D)	10kHz Input Signal, T_A = 25°C		70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz Input Signal, T_A = 25°C	MAX167			-80	dB
			MAX163, MAX164			-76	
Peak Harmonic or Spurious Noise		10kHz Input Signal, T_A = 25°C	MAX167			-80	dB
			MAX163, MAX164			-76	
Full Power Sampling Bandwidth		In Track Mode, Under Sampled Waveform			6		MHz
ANALOG INPUT							
Input Voltage Range (Note 4)		MAX163 MAX164 MAX167		0 -5 -2.5		+5 +5 +2.5	V
Input Leakage Current						±1	µA
Input Capacitance (Note 5)						20	pF
Track-Hold Acquisition Time				1			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode (see text), T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.6MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF} Output Voltage		T_A = 25°C	-4.98	-5.00	-5.02	V
V_{REF} Output Tempco (Note 6)		MAX16XB, MAX16XA MAX16XC			25 45	ppm/°C
Reference Load Sensitivity		$\Delta FS/\Delta I_{REF}$, I_{REF} Load Change: 0 to 5mA		0.2	1	LSB/mA
Output Sink Current					5	mA
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN	2.4			V
Input Capacitance (Note 5)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			10	pF
Input Current	I_{IN}	V_{IN} = 0V to V_{DD} — $\overline{CS}$, $\overline{RD}$, HBEN V_{IN} = 0V to V_{DD} — CLK IN			10 20	µA
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SOURCE} = 200µA	4			V
Three-State Leakage Current	I_L	D11-D0/8, V_{OUT} = 0V to V_{DD}			±10	µA
Three-State Output Capacitance	C_O	(Note 5)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	±5% For Specified Performance		5		V
Negative Supply Voltage	V_{SS}	±5% For Specified Performance	-12		-15	V
Positive Supply Rejection		FS Change, V_{SS} = -15V or -12V V_{DD} = 4.75V to 5.25V		±1/2		LSB
Negative Supply Rejection		FS Change, V_{DD} = 5V V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		7	10	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -12V		104	150	mW

Note 1: Typical change over temp is ±1 LSB.
Note 2: Ideal last code transition = FS - 3/2 LSB, adjusted for offset.
Note 3: Full Scale Tempco = $\Delta FS/\Delta T$, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: V_{IN} must not exceed V_{DD} for specified accuracy.
Note 5: Guaranteed by design, not subject to test.
Note 6: V_{REF} Tempco = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.

CMOS 12-Bit A/D Converters With Track-and-Hold

TIMING CHARACTERISTICS (See Figures 9-12)

(V_{DD} = +5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, Note 7, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted).

PARAMETER	SYMBOL (Figures 9-12)	CONDITIONS	T_A = 25°C MIN	TYP	MAX	MAX16XXC/E MIN	MAX	MAX16XXM MIN	MAX	UNITS
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 8)	t_2	CL = 50pF		**80**	**170**		**220**		**260**	ns
Data Access Time (Notes 8, 9)	t_3	CL = 100pF		**50**	**100**		**130**		**150**	ns
$\overline{RD}$ Pulse Width	t_4		100			130		150		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ (Notes 8, 9)	t_6			**40**	**80**		**105**		**120**	ns
Bus Relinquish Time (Notes 8, 10)	t_7			**30**	**50**		**65**		**75**	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between READ Operations	t_{10}		200			200		200		ns
Delay Between Conversions	t_{11}		1			1		1		µs
Aperture Delay	t_{12}	Jitter < 50ps		25						ns
CLK to $\overline{BUSY}$ Delay	t_{13}			80	170		220		260	ns

Note 7: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 8: This specification is 100% production tested.
Note 9: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 10: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

CMOS 12-Bit A/D Converters With Track-and-Hold

Pin Description

PIN	NAME	FUNCTION
1	AIN	Sampling Analog Input, MAX163: 0V to +5V Unipolar MAX164: ±5V Bipolar MAX167: ±2.5V Bipolar
2	V_{REF}	-5.00V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLK IN	Clock Input. An external TTL compatible clock may be connected, or a crystal may be connected between CLK IN and CLK OUT.
18	CLK OUT	Clock Output. An inverted CLK IN signal appears at this pin.
19	HBEN	High Byte Enable Input. Used to multiplex the internal 12-bit conversion result into the lower order outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low input starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.
22	$\overline{BUSY}$	The $\overline{BUSY}$ Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V or -12V
24	V_{DD}	Positive Supply, +5V

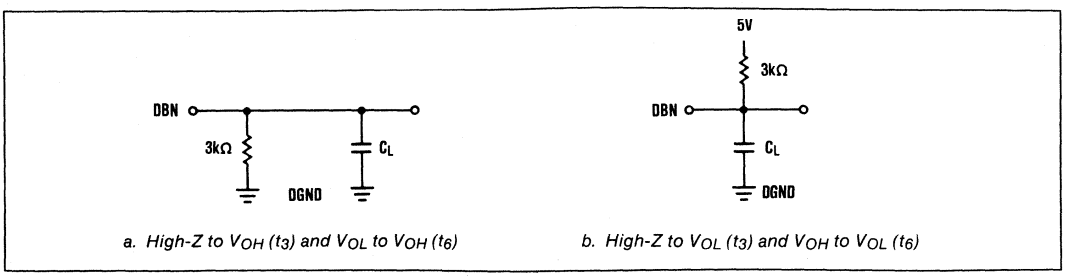
A/D Converter Operation

The MAX163/164/167 use successive approximation and input track-and-hold circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic provides easy interface to microprocessors so that most applications require only passive components to perform analog-to-digital conversions. No "hold" capacitor is required. Figure 3 shows the MAX163/164/167 in their simplest operational configuration.

Analog Input—Track-and-Hold

In Figure 4, the equivalent input circuit illustrates the sampling architecture of the ADC's analog comparator. The comparator's input capacitance acts as the "hold" capacitor and must be completely charged by the input signal with every A/D conversion (but NOT every clock cycle). The capacitance is charged through an internal 1kΩ protection resistor in series with the input.

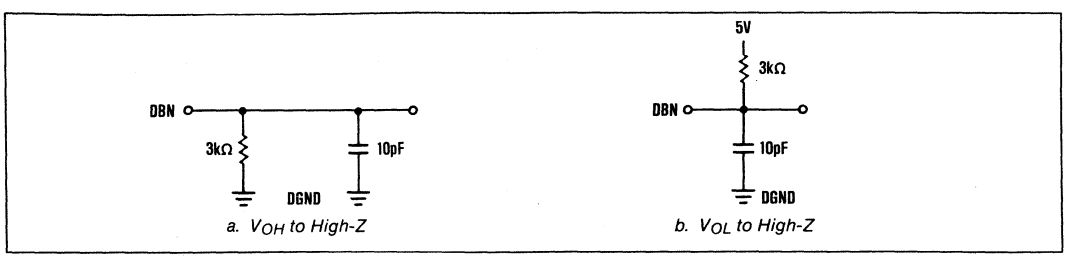
To an input signal, AIN appears as a capacitor switching between analog ground and the input signal. Between conversions (BUSY high and RD or CS or HBEN high) the capacitor is connected to AIN. When a conversion starts, the capacitor disconnects from AIN, thus sampling the input, and is internally discharged. At the end of the conversion it reconnects to the input and charges to the input signal. The loading effect of AIN on the analog signal is such that a high speed input buffer is usually NOT needed. This is because the A/D disconnects from the input during the actual conversion.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time

CMOS 12-Bit A/D Converters With Track-and-Hold

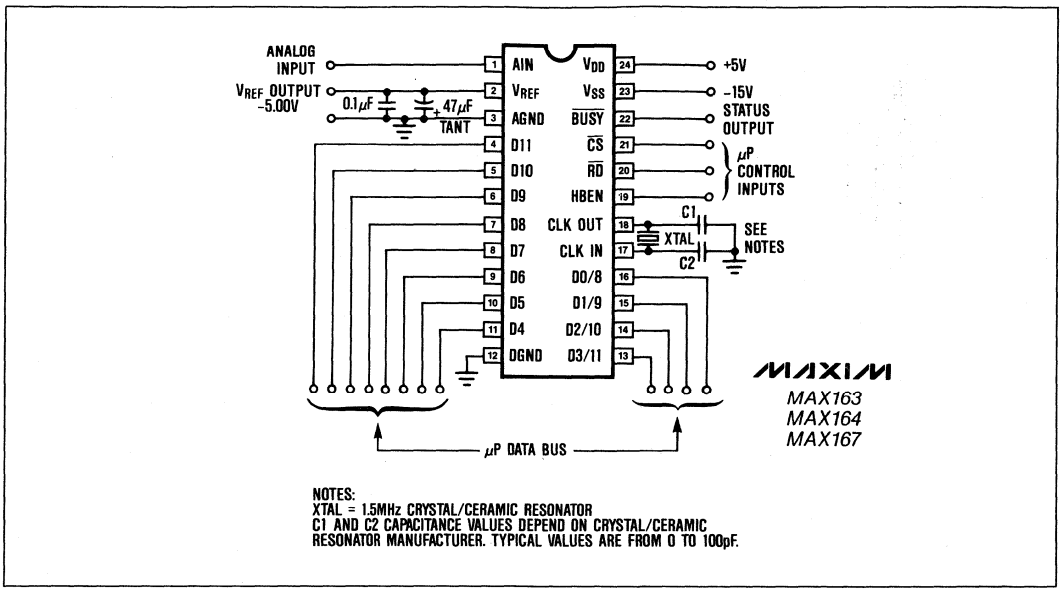


Figure 3. MAX163/164/167 Operational Diagram

The track-and-hold enters its "tracking" mode when the ADC is deselected (CS high) and BUSY is high. "Hold" mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is less than 50ps. Figures 9 through 12 detail the track-and-hold and interface timing for the various interface modes. The internal track-and-hold control logic is shown in Figure 5.

The time required for the track-and-hold to acquire an input signal is a function of how quickly the input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + R_{IN})20pF \text{ (but never less than } 1\mu s)$$

Where R_{IN} = 1kΩ, and R_S = source impedance of the ADC's input signal.

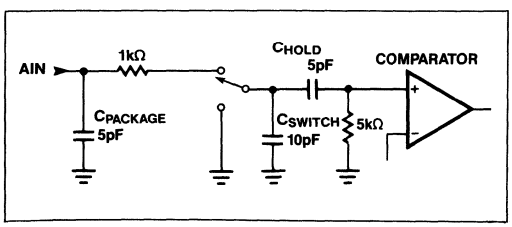


Figure 4. Equivalent Input Circuit

Input Bandwidth

The A/D's input tracking circuitry has excellent large signal and wide bandwidth behavior. It is not slew limited like many other ADC track-and-holds. Remarkably, the MAX163/164/167 track-and-hold's full power bandwith is typically 6MHz. This makes it possible to digitize high speed transient events and to measure periodic signals whose bandwidth exceeds the ADC's sample rate (>100kHz) by using under sampling techniques. It is important to note here that if under sampling is used to measure high frequency signals, special care must be taken to avoid aliasing errors. Without adequate input filtering, high frequency noise may be aliased into the measurement band.

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{REF}, work with an internal series resistance to allow over drives of up to ±15V at AIN

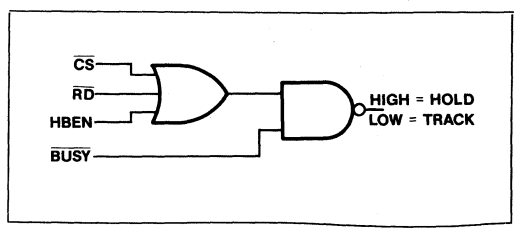


Figure 5. Track-Hold Internal Control Logic

with no risk of damage to the A/D. However, for accurate conversions near full scale (MAX163 and MAX164 only), AIN should not exceed V_{DD} because A/D accuracy is affected while the protection diodes are even slightly turned on.

Starting a Conversion

The ADC is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. The track-and-hold enters Hold Mode and a conversion starts at the falling edge of CS and RD while HBEN is low. The BUSY output goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, BUSY goes high and the conversion result is latched into three-state output buffers.

Internal/External Clock

Figure 6 shows the MAX163/164/167 clock circuitry. The capacitive load on the CLK OUT pin must be minimized to avoid digital coupling of the CLK OUT buffer currents to the ADC's analog comparator. If an external clock source drives CLK IN, then CLK OUT should be left open. Acceptable external clock duty cycles are between 20% and 80%, so a precise square wave is not required. If the internal oscillator is used, a crystal or ceramic resonator is connected between CLK OUT and CLK IN as shown in Figure 6.

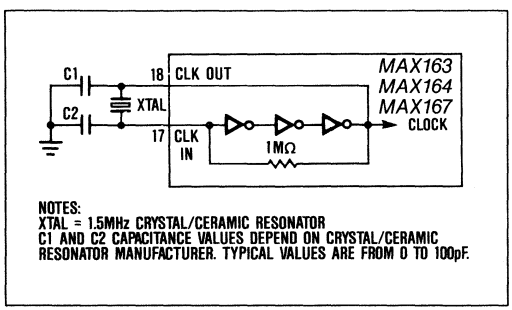


Figure 6. Internal Clock Circuit

Internal Reference

The MAX163/164/167 have a -5.00V buried zener reference which biases the internal DAC. The reference output is available at V_{REF} (Pin 2) and should be bypassed to AGND (Pin 3) with a 47µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor. This minimizes noise and maintains a low impedance at high frequencies. A resistor should NOT be connected between the bypass capacitors and Pin 2. The internal reference output buffer can sink up to 5mA.

Digital Interface

Clock and Control Synchronization

For best analog performance, the MAX163/164/167 clock should be synchronized to the RD and CS control inputs as shown in Figure 7, with at least 100ns separating convert start from the nearest clock edge. This ensures that transitions at CLK IN and CLK OUT do not couple to the analog input and get sampled by the track-and-hold. The magnitude of this feedthrough is only a few millivolts, but if CLK and convert start (CS and RD) are asynchronous, frequency components caused by mixing of the clock and convert signals may increase the apparent input noise.

When the clock and convert signals are synchronized, small endpoint errors (offset and full scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be eliminated by ensuring that the start of a conversion (RD and CS falling edge) does not occur within 100ns of a clock transition, as in Figure 7. Nevertheless, even without observing this guideline, the MAX163/164/167 are still compatible with either the MAX162/172 or the MX7572 synchronization modes, with no increase in linearity error. This means that either the falling or rising edge of CLK IN may be near $\overline{RD}$'s falling edge.

Output Data Format

The 12 data bits can be output either in full parallel or as two 8-bit bytes. The data bus output format is shown in Table 1. To obtain parallel output for 16-bit processors, HBEN is permanently tied low. The output data, DB11-DB0, is then right justified, i.e., DB0, the LSB, is the right most bit in the 16-bit word.

For a two byte read, outputs D7 through D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented at DB0-DB3 with the leading 4 bits low in locations D4-D7. Note that the 4 MSBs always appear at D11-D8 whenever the outputs are enabled, regardless of the state of HBEN.

Timing And Control

Conversion start and data read operations are controlled by three digital inputs, HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 8 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion and once the conversion is in progress, it cannot be re-started. BUSY remains low during the entire conversion cycle.

Two modes of operation are outlined in the timing diagrams of Figures 9-12. Slow Memory Mode is intended for processors that can be forced into a WAIT state during the ADC's conversion time. ROM Mode is for processors that cannot be forced into a wait state. In both modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation accesses the conversion result.

CMOS 12-Bit A/D Converters With Track-and-Hold

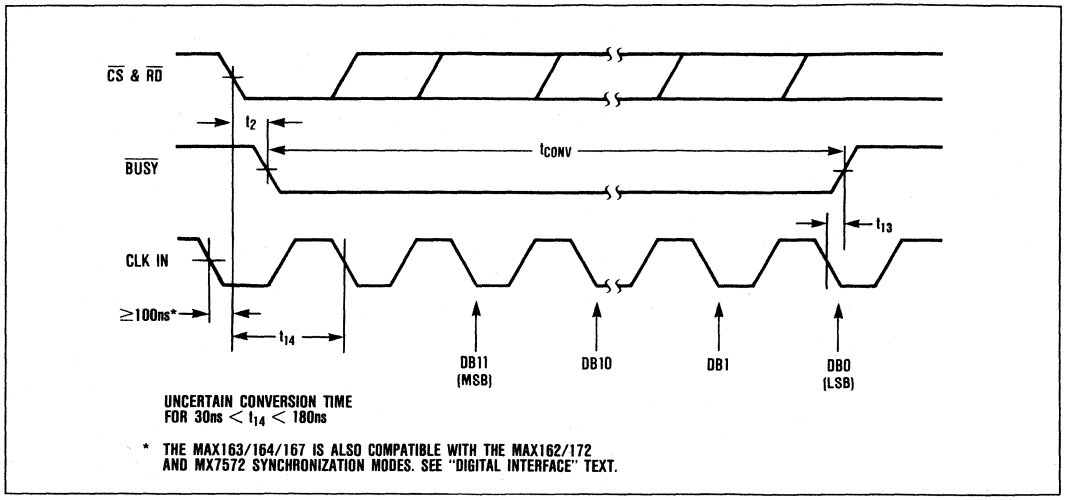


Figure 7. $\overline{RD}$ and CLK IN for Synchronous Operation

Table 1. Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note: *D11 ... D0/8 are the ADC data output pins.
DB11 ... DB0 are the 12-bit conversion results, DB11 is the MSB.

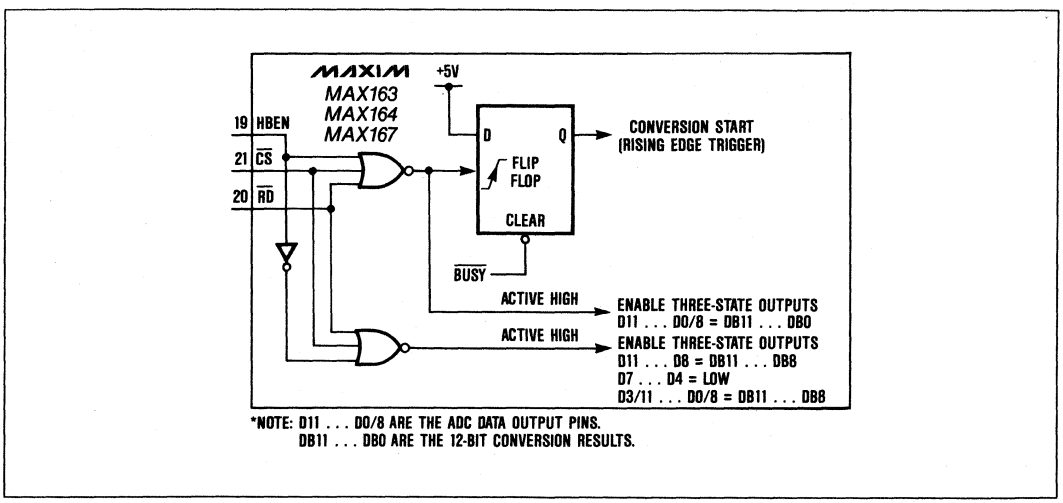


Figure 8. Logic Equivalent for $\overline{RD}$, $\overline{CS}$ and HBEN Inputs

Slow Memory Mode, Parallel Read (HBEN = LOW)

See Figure 9 and Table 2. Taking $\overline{CS}$ and $\overline{RD}$ low starts the conversion. $\overline{BUSY}$ remains low while the conversion is in progress. The PREVIOUS (old) result appears at the digital outputs until the end of the conversion when $\overline{BUSY}$ returns high. The output latches are then updated with the newest result on D11-D0/8.

Slow Memory Mode, Two Byte Read

See Figure 10 and Table 3. Outputs D7-D0/8 are used for a two byte read. The start and read operations for the 8 LSBs are identical to the Slow Memory Mode, Parallel Read. A second read operation with HBEN high places the 4 MSBs, with 4 leading zeros, on data outputs D7-D0/8. This second read operation does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

See Figure 11 and Table 4. ROM Mode avoids using processor wait states. A conversion starts with a read operation and the 12 data bits from the PREVIOUS conversion appear at D11-D0/8. The data from the first read in a sequence is often disregarded when this interface mode is used. A second read accesses the results of the first conversion and also starts a new conversion. The time between successive READs must be longer than the MAX163/164/167 conversion times.

ROM Mode, Two Byte Read

See Figure 12 and Table 5. As in the Slow Memory Mode, only D7-D0/8 are used for two byte reads. A conversion starts with a read operation with HBEN low. At this point the data outputs contain the 8 LSBs from the PREVIOUS conversion. Two more read operations are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading zeros are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Application Hints

Initialization After Power Up

In some applications it may be desirable to remove power from the ADC during periods of inactivity. This is increasingly common in battery powered systems. To initialize the MAX163/164/167 at power up, perform a read operation with HBEN low and ignore the data outputs.

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, errors can be caused by coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM Mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

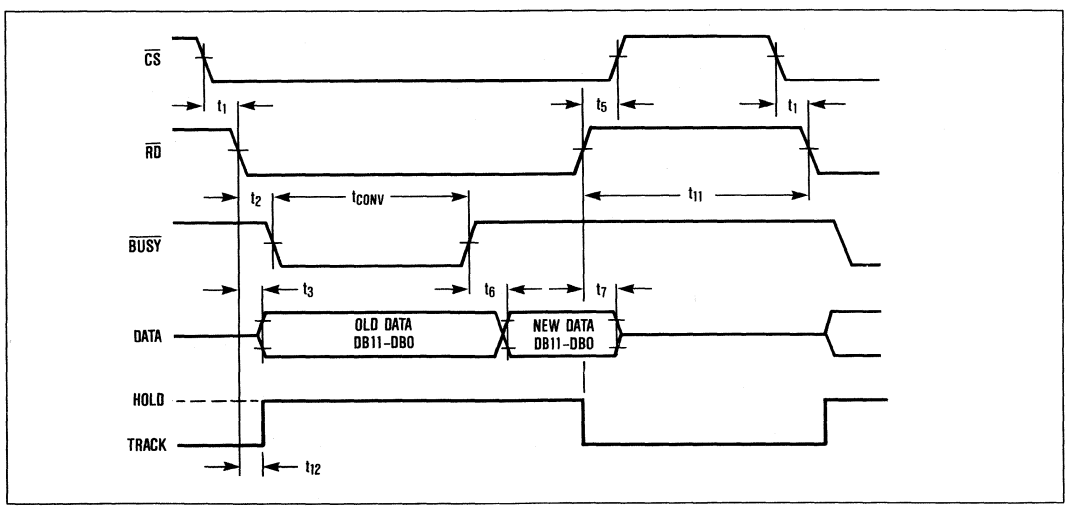


Figure 9. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

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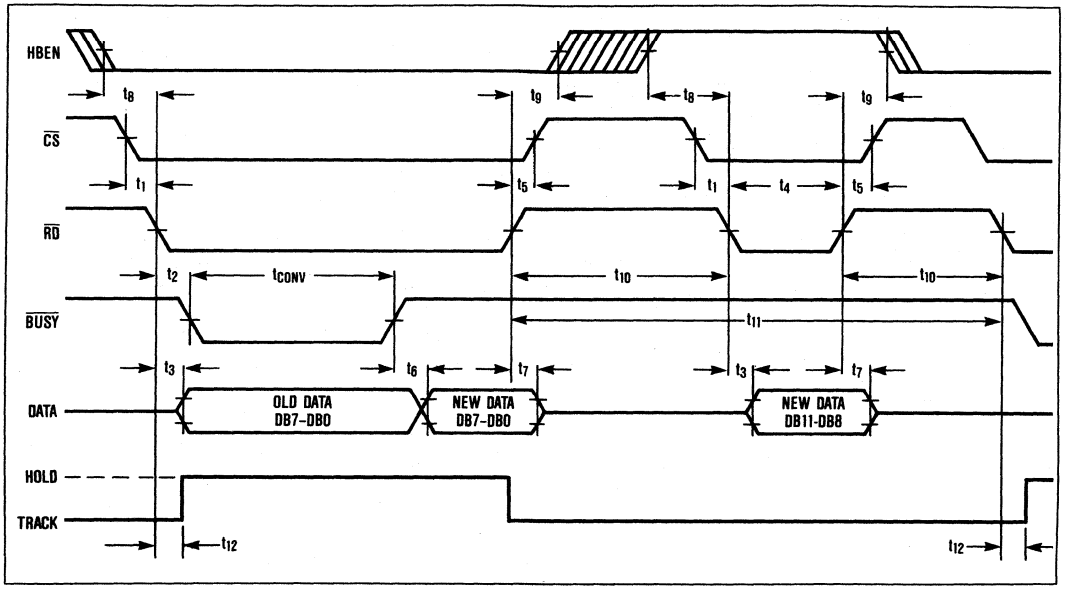

Figure 10. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

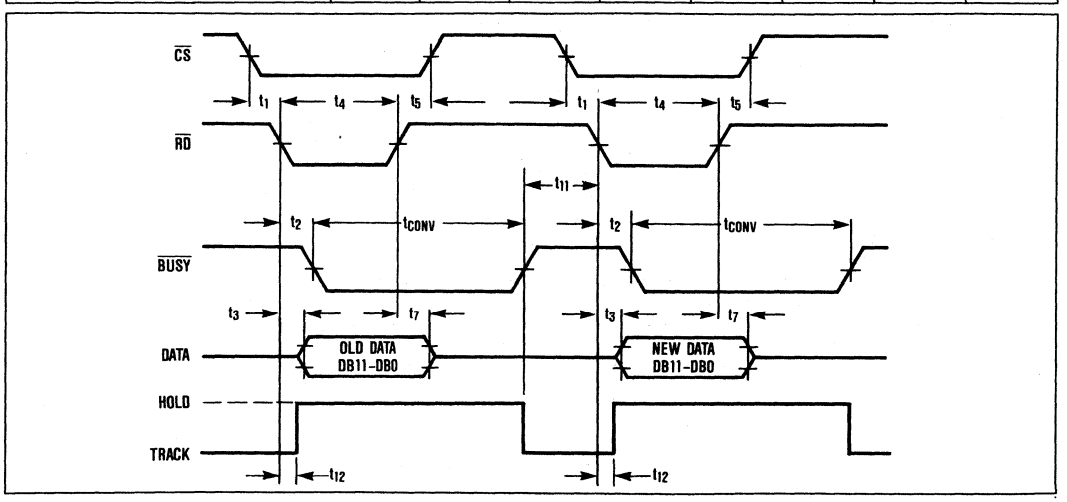

Figure 11. ROM Mode, Parallel Read Timing Diagram

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

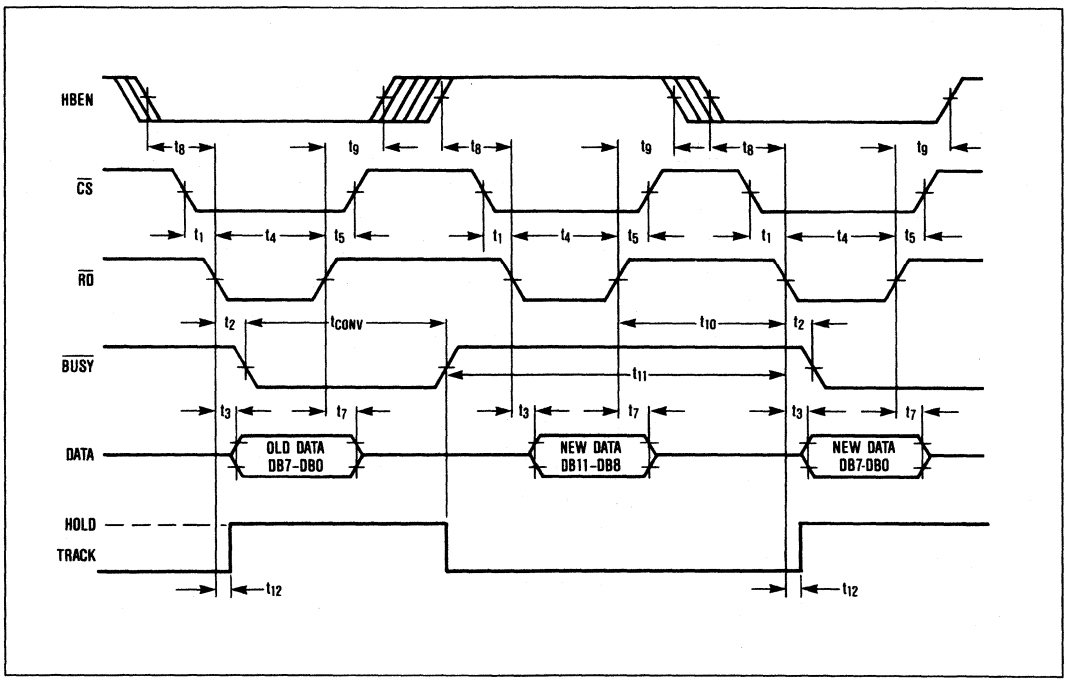

Figure 12. ROM Mode, Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

In ROM Mode, considerable digital noise is generated in the ADC when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after a conversion is started. This noise can affect the ADC comparator and cause large errors if it coincides with the time the SAR is latching a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ must go high at a rising edge of CLK IN, since the comparator output is always latched at falling edges of CLK IN.

Layout, Grounding, Bypassing

For best system performance printed circuit boards should be used. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

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Figure 13 shows the recommended system ground connections. A single point analog STAR ground should be established at Pin 3 (AGND) separate from the logic ground. All other analog grounds and Pin 12 (DGND) should be connected to this STAR ground and no other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog STAR ground with 0.1μF and 10μF bypass capacitors. Capacitor leads should have minimum length for best supply noise rejection. If the +5V power supply is very noisy, a small (4.7Ω-20Ω) resistor can be connected as shown in Figure 13 to filter this noise.

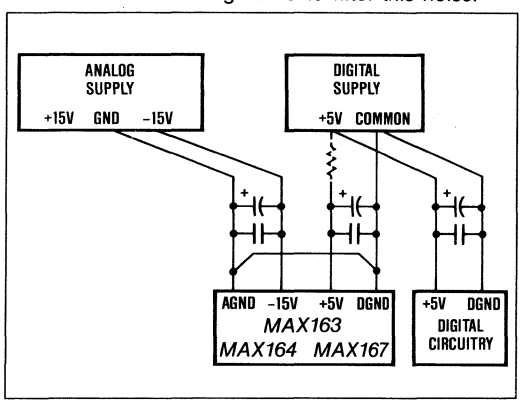

Figure 13. Power Supply Grounding Practice

Gain and Offset Adjustment

The plot in Figure 14 graphs the nominal unipolar input/output transfer function of the MAX163. Code transitions occur half way between successive integer LSB values. Output coding is natural binary with 1 LSB = 1.22mV (5V/4096). Figure 15 shows the bipolar input transfer function for the MAX164/167, where output coding is offset binary.

In applications where gain (full scale range) adjustment is required, the connection shown in Figure 16 provides ±0.5%, or ±20 LSBs, of adjustment range. If both offset and full scale range need adjustment, the circuit in Figure 17 is recommended. Offset should be adjusted before gain. For the MAX163 (0V to +5V input range), apply +1/2 LSB (0.61mV) to the analog input and adjust R12 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply FS - 1-1/2 LSB (4.99817V) and adjust R8 until the output code changes between 1111 1111 1110 and 1111 1111 1111. There may be slight interaction between adjustments. If an input gain of two is acceptable, the connection in Figure 17 can be simplified by removing R5 and R6.

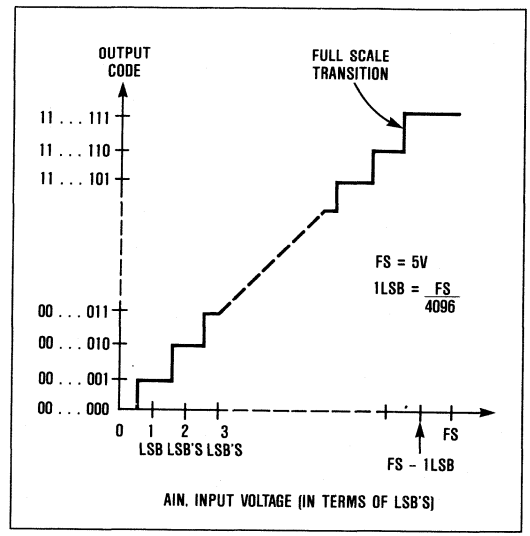

Figure 14. MAX163 Unipolar Transfer Function

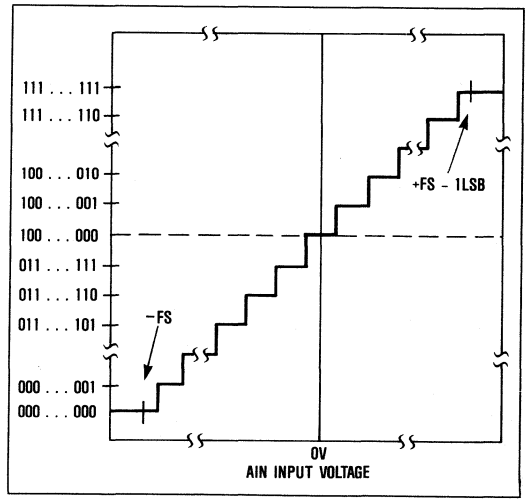

Figure 15. MAX164/167 Bipolar Transfer Function

To adjust bipolar offset (MAX164 ±5V, MAX167 ±2.5V), apply +1/2 LSB (1.22mV for MAX164, 0.61mV for MAX167) to the analog input and adjust R12 for output code flicker between 1000 0000 0000 and 1000 0000 0001. For full scale, apply FS - 1-1/2 LSB (+4.99634V for the MAX164, 2.49817V for the MAX167) to the input and adjust R8 so the output code flickers between 1111 1111 1110 and 1111 1111 1111. There may be some interaction between these adjustments.

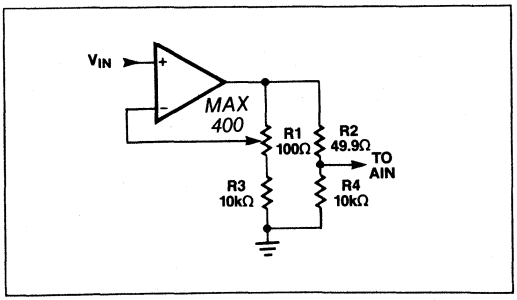

Figure 16. Trim Circuit for Gain Only (±0.5%)

Dynamic Performance

High speed sampling capability and 100kHz throughput make the MAX163/164/167 ideal for wideband signal processing. To support these and other related applications, FFT (Fast Fourier Transform) test techniques are used to guarantee the A/D's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

A-to-D converters have traditionally been evaluated by specifications such as Zero and Full Scale Error, Integral Non-linearity (INL), and Differential Non-linearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals but are less useful in signal processing applications where the A/D's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

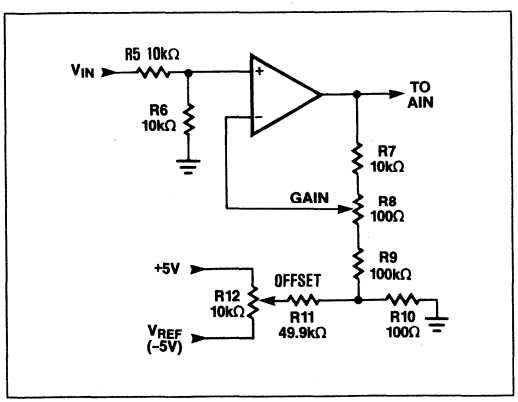

Figure 17. Offset (±20mV) and Gain (±0.5%) Trim Circuit

Signal-to-Noise Ratio and Effective Number of Bits

The ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). The output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason the ratio is sometimes referred to as "Signal-to-Noise + Distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the A/D's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit A/D can, therefore, do no better than 74dB. Figure 18 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX167. An FFT plot of the output shows the output level in various spectral bands.

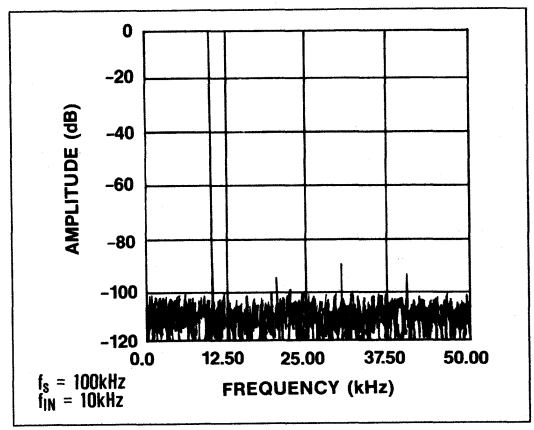

Figure 18. FFT Plot for the MAX167

By transposing the equation which converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "Effective Number of Bits" that the A/D provides: N = (SNR - 1.76)/6.02. Figure 19 shows the effective number of bits as a function of the input frequency for the MAX167.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20Log\left[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_4^2 + ... + V_N^2)/V_1}\right]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

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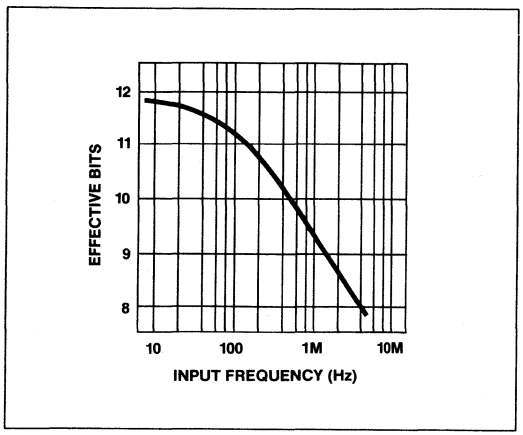
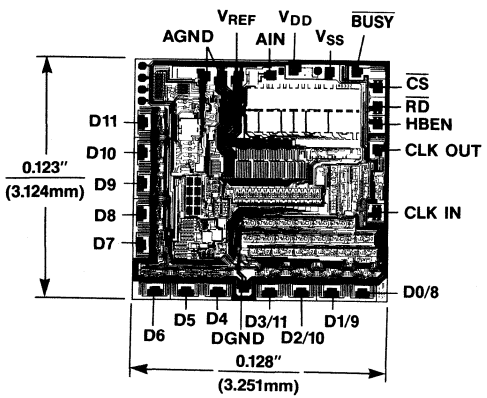


Figure 19. MAX167 Effective Bits vs. Input Frequency

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the Peak Harmonic (or Spurious) Noise. Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX167BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX167CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CC/D	0°C to +70°C	Dice**	±1 LSB
MAX163BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CC/D	0°C to +70°C	Dice**	±1 LSB
MAX164BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164CMRG	-55°C to +125°C	CERDIP	±1 LSB

** All devices—24 lead packages*
***Consult factory for dice specifications*

MAXIM

Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

General Description

The MAX171 is a complete 5.8µs, 12-bit analog-to-digital converter (ADC) that provides over 1,500V_{RMS} electrical isolation between its analog input and the digital interface pins. It combines a serial output 12-bit ADC, three opto-couplers, and a low-drift buried-zener voltage reference in a standard 16-lead plastic DIP package (0.3").

Required external components are limited to supply and reference decoupling capacitors and three resistors. The 2.5MHz clock input can be driven from an external clock source such as a divided microprocessor clock. The MAX171 works with +5V and -12V to -15V supply voltages and typically dissipates 265mW.

The MAX171 is useful in applications where an analog signal must be electrically isolated from control electronics to avoid hazardous electrical conditions, provide noise immunity, or bridge large differences in ground potential. These situations have traditionally required an instrumentation or isolation amplifier with suitably high common mode rejection. If the analog signal must be digitized at some point in the signal chain, the MAX171 can replace these isolating amplifiers while providing high performance and lower cost.

Applications

Ground-Loop Interruption

Process Control

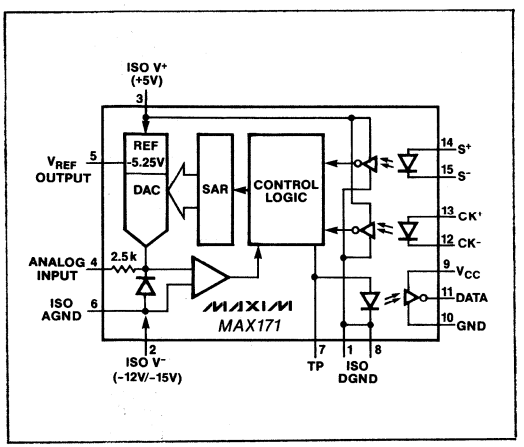
Isolated Industrial Data Acquisition

Electro-Mechanical Systems

Robotics

Automatic Test Equipment

Functional Diagram



Features

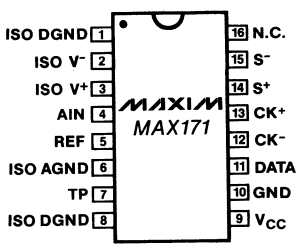
- ♦ **Optical Isolation to Over 1,500V_{RMS}**
- ♦ **UL Recognized in File E118032 to UL1577**
- ♦ **12-Bit Resolution and Linearity**
- ♦ **5.8µs Conversion Time**
- ♦ **No Missing Codes Over Temperature**
- ♦ **Serial Output**
- ♦ **Complete with On-Chip Reference**
- ♦ **Standard 16-Lead Plastic DIP Package**

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX171ACPE	0°C to +70°C	Plastic DIP	±½ LSB
MAX171BCPE	0°C to +70°C	Plastic DIP	±1 LSB
MAX171AEPE	-40°C to +85°C	Plastic DIP	±½ LSB
MAX171BEPE	-40°C to +85°C	Plastic DIP	±1 LSB

Pin Configuration

TOP VIEW



Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

$V_{ISO\ V+}$ to ISO GND ..... -0.3V to +7V
$V_{ISO\ V-}$ to ISO GND ..... +0.3V to -17V
AIN to ISO GND ..... ±15V
V_{CC} to GND ..... -0.3V to +7V
DATA Output Current 60mA
DATA Output Voltage 5.5V
Digital Inputs: S^+ to S^- and CK^+ to CK^-:
LED Current 15mA
LED Reverse Voltage 5V

Isolation Voltage
1 second ..... 1,500 V_{RMS}
1 minute ..... 1,200 V_{RMS}
Continuous ..... 130 V_{RMS}
Operating Temperature Ranges
MAX171XC ..... 0°C to +70°C
MAX171XE ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, $V_{ISO\ V+}$ = +5V ±5%, $V_{ISO\ V-}$ = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ISOLATION (T_A = +25°C, Note 1)							
Test Voltage	V_{ISO}	1 second withstand 1 minute withstand (Note 2)		1500 1200			V_{RMS} V_{RMS}
Leakage Current	I_{ISO}	V_{ISO} = 130V_{RMS}, 60Hz			2	50	μA_{RMS}
Resistance	R_{ISO}	V_{ISO} = 500VDC			10^{10}		Ω
Capacitance	C_{ISO}				5		pF
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL		MAX171AC MAX171AE MAX171B			±1/2 ±3/4 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Specified Temperature Range				±1	LSB
Offset Error (Note 3)			MAX171A MAX171B			±3 ±5	LSB
Full Scale Error (Note 4)		T_A = 25°C				±10	LSB
Full Scale Tempco (Notes 5, 6)						±45	ppm/°C
Conversion Time	t_{CONV}	14 Clock Cycles + Opto-Coupler Delay				5.8	µs
ANALOG INPUT							
Input Voltage Range				0		+5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 7)						±40	ppm/°C
Output Current Sink Capability		(Note 8)				5	mA
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS Change, V_{SS} = -15V or -12V	V_{DD} = 4.75V to 5.25V		±1/2		LSB
Negative Supply Rejection	V_{SS}	FS Change, V_{DD} = +5V	V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, $V_{ISO\ V+}$ = +5V ±5%, $V_{ISO\ V-}$ = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (S^+ to S^- and CK^+ to CK^-)						
LED Operating Current	I_{IN}		8	10	15	mA
LED Forward Operating Voltage	V_{IN}	I_{IN} = 10mA		1.55	1.75	V
LED Capacitance (Note 9)	C_{IN}			60		pF
LOGIC OUTPUT (DATA)						
Output Low Voltage	V_{OL} V_{OL}	I_{SINK} = 1.6mA I_{SINK} = 13mA	 0.25		0.4 0.6	V
Output High Current	I_{OH}	V_{DATA} = 5.5 V		0.02	250	µA
POWER REQUIREMENTS						
Analog Positive Supply Voltage	$V_{ISO\ V+}$	±5% for Specified Performance	4.75		5.25	V
Analog Negative Supply Voltage (Note 10)	$V_{ISO\ V-}$	±5% for Specified Performance	-15.75		-11.4	V
Analog Positive Supply Current	$I_{ISO\ V+}$	START = V_{DD}, AIN = 0V		25	44	mA
Analog Negative Supply Current	$I_{ISO\ V-}$	START = V_{DD}, AIN = 0V		-6	-12	mA
Digital Positive Supply Voltage	V_{CC}		4.75		5.25	V
Digital Positive Supply Current	I_{CC}			10	18	mA
Power Dissipation		$V_{ISO\ V+}$ = +5V, $V_{ISO\ V-}$ = -15V, V_{CC} = +5V		265	495	mW
TIMING CHARACTERISTICS (Note 11)						
CLOCK Pulse Width	t_{CH} t_{CL}	CLOCK HIGH CLOCK LOW	60 80			ns
START Pulse Width	t_{SH} t_{SL}	START HIGH START LOW	60 80			ns
START to CLOCK Skew	t_{SC0} t_{SC1}	Leading CLOCK Leading CLOCK + 1	 250		100	ns
CLOCK to DATA Delay	t_{PD}	T_A = 25°C		175	250	ns

Note 1: Isolation voltage is measured between pins 1 to 8 connected together and pins 9 to 16 connected together.
Note 2: Guaranteed by the "2 second withstand test voltage," which is 100% production tested.
Note 3: Typical change over temp is ±1 LSB.
Note 4: $V_{ISO\ V+}$ = +5V, $V_{ISO\ V-}$ = -15V, FS = +5.000V or +2.500V. Ideal last code transition = FS - 3/2LSB
Note 5: Full Scale Tempco = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Includes internal reference drift.
Note 7: V_{REF} Tempco = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 8: Output current should not change during conversion.
Note 9: Guaranteed by design, not subject to test.
Note 10: Specified performance with -12V supply is guaranteed by testing offset and full scale errors.
Note 11: Timing specifications are sample tested to LTPD = 10 at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

Pin Description

PIN DIP	NAME	FUNCTION
1	ISO DGND	Isolated Digital Ground
2	ISO V^-	Analog Negative Supply, -12V or -15V
3	ISO V^+	Analog Positive Supply, +5V
4	AIN	Analog Input, 0V to +5V Unipolar
5	REF	Reference Voltage Output, -5.25V
6	ISO AGND	Isolated Analog Ground. Normally tied to ISO DGND
7	TP	Test Pin. Leave unconnected
8	ISO DGND	Isolated Digital Ground
ELECTRICAL ISOLATION BARRIER		
9	V_{CC}	Digital Positive Supply. +5V
10	GND	Digital Ground
11	DATA	Serial Data Output
12	CK^-	Clock$^-$ Input
13	CK^+	Clock$^+$ Input
14	S^+	Conversion Start$^+$ Input
15	S^-	Conversion Start$^-$ Input
16	N.C.	No Connect

Converter Operation

A/D Converter

The MAX171 combines a successive approximation A/D converter and three opto-couplers to convert an unknown analog input to an electrically isolated 12-bit serial output code. The opto-coupled digital interface works with three interface signals: Conversion Start Input (S^+, S^-), Clock Input (CK^+, CK^-), and the Serial Data Output (DATA). Most applications require only a few external passive components to perform the analog-to-digital function. Figure 1 shows the MAX171 in its simplest operational configuration.

Figure 2 shows the MAX171 analog equivalent circuit. The internal digital-to-analog converter (DAC) is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero-crossing detector with its output feeding back to the SAR input.

Opto-Couplers

The Start (S^+, S^-) and Clock (CK^+, CK^-) inputs to the MAX171 are unbuffered LEDs and require a series resistor of typically 470Ω to a TTL or 5V-CMOS gate to set the drive current. The preferred connection is to tie the resistor from +5V to the LED anode and then connect logic LED cathode as shown in Figure 1. Alternatively, logic drive current may be sourced to a grounded LED, but this requires opposite logic polarity from Figure 1 for both the Start and Clock signals.

The serial data output is an open-collector NPN bipolar transistor, and normally requires a 470Ω pull-up resistor to a +5V supply. The external stray capacitance at the DATA output pin should be kept below 10pF for operation at the maximum clock rate. A low signal at the DATA output represents a logical "1" in the output word.

Power Supplies

The MAX171 requires three power supplies: +5V and -12V to -15V is required on the isolated analog side of the package (ISO V^+, ISO V^-). A separate +5V voltage source (V_{CC}) is required on the digital side of the isolation barrier for the DATA output transmitter.

Digital Interface

Clock — Data Skew

While the opto-isolators used in the MAX171 are fast enough for the specified conversion speed of 5.8µs, they do add a time delay that impacts high speed operation. The A/D cannot begin processing a clock edge before it crosses the isolation barrier. Therefore, the digital I/O signals at the A/D lag/lead the digital signals at the input/output pins. For example, as each successive approximation decision is sent out, it appears at the DATA pin following a delay induced by the opto-coupler. At low conversion rates (below 1MHz clock) these delays are negligible and Clock and Start signals may be applied simultaneously to the MAX171 and to the output register. At clock speeds above 1MHz, these delays become a significant portion of the clock cycle and must be compensated for best performance. Figure 3 illustrates using delay lines in the start and clock signals applied to the output register.

Timing and Control

A conversion cycle is initiated on the rising edge of the conversion start signal that is coincident with a falling edge of the Clock signal. Figure 4 shows a single conversion cycle with a continuous Clock. Once started, a conversion cannot be stopped and transitions at the Start input have no effect until the CURRENT conversion is completed (minimum of 14 clock cycles from the last rising edge of the conversion start signal).

Opto-Isolated Serial Output 5.8μs 12-Bit A/D Converter

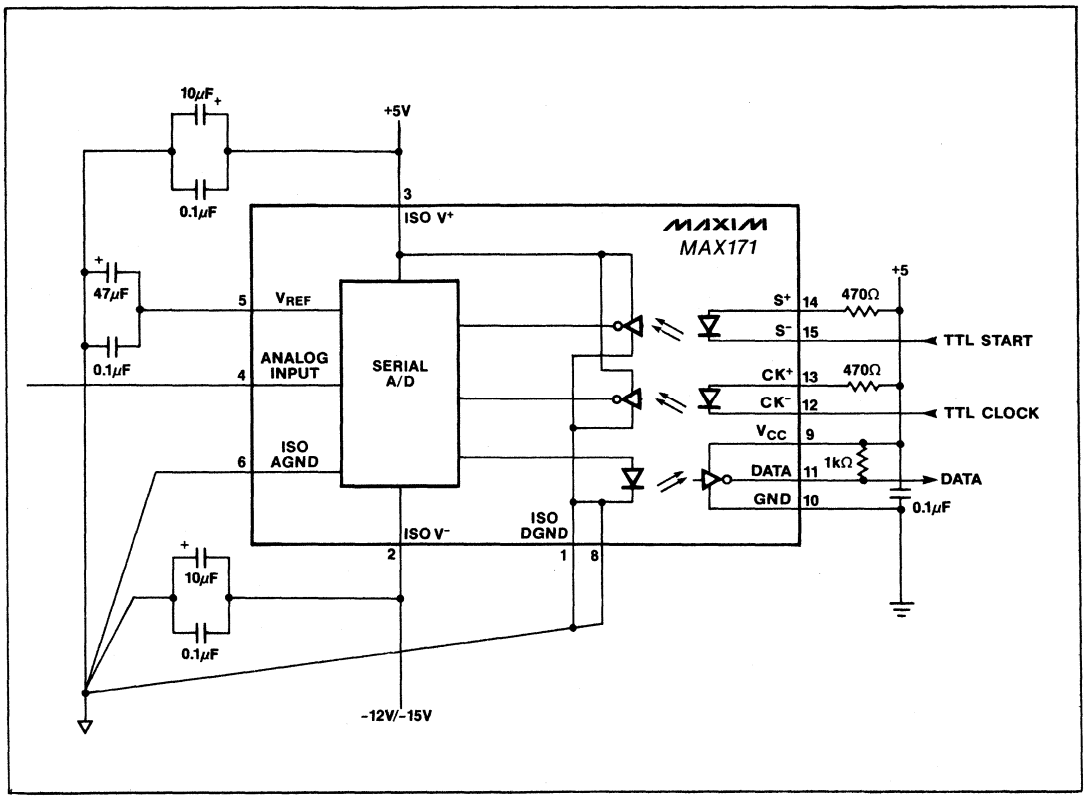


Figure 1. MAX171 Operating Circuit

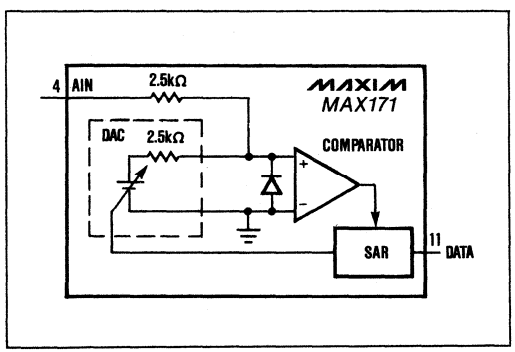


Figure 2. MAX171 Analog Equivalent Circuit

The Conversion Start transition causes the SAR to set B11 (MSB), driving the DAC output to half-scale. The analog input is compared to this value from the time of the conversion start transition until the second falling Clock edge which latches the MSB result and sets the SAR to compare the next bit. The MSB result appears at the DATA output after a delay, t_{PD} from the falling edge of Clock. Each subsequent bit conversion proceeds similarly until all 12 bits of the DAC have been tried. The conversion is completed at the falling edge of the 13th Clock cycle. The DATA output returns high at the falling edge of the 14th Clock cycle and remains so until the next conversion sends out its MSB result.

The next conversion can be started on the 14th Clock cycle of a previous conversion as shown in Figure 4. This allows the maximum throughput rate, one conversion per 14 Clock cycles.

Opto-Isolated Serial Output 5.8μs 12-Bit A/D Converter

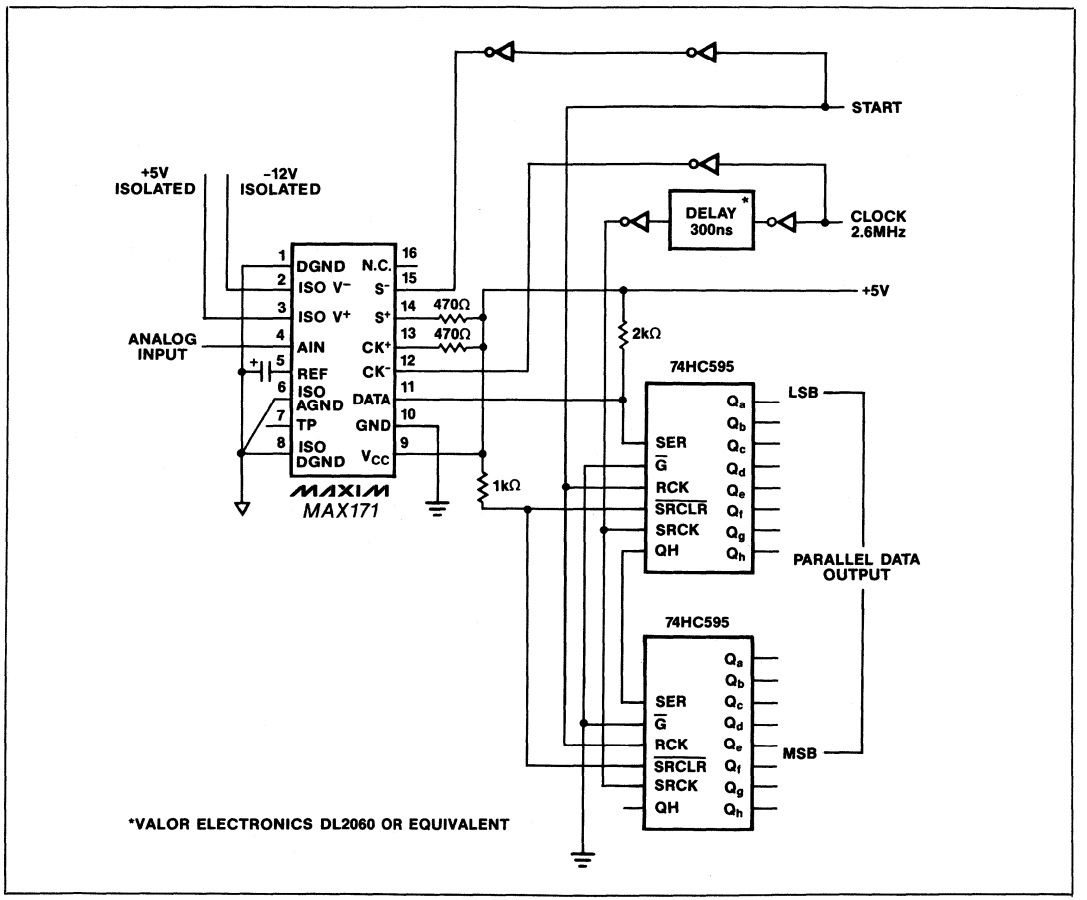


Figure 3. MAX171 Opto-Isolated Conversion with Parallel Data Output

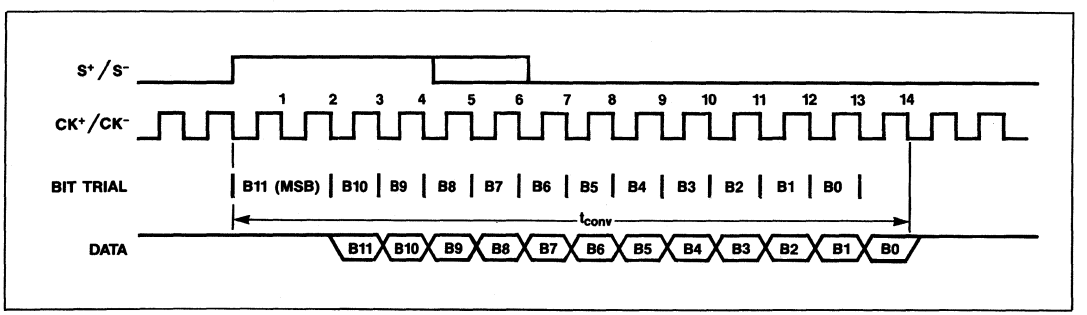


Figure 4. MAX171 Conversion Cycle Timing

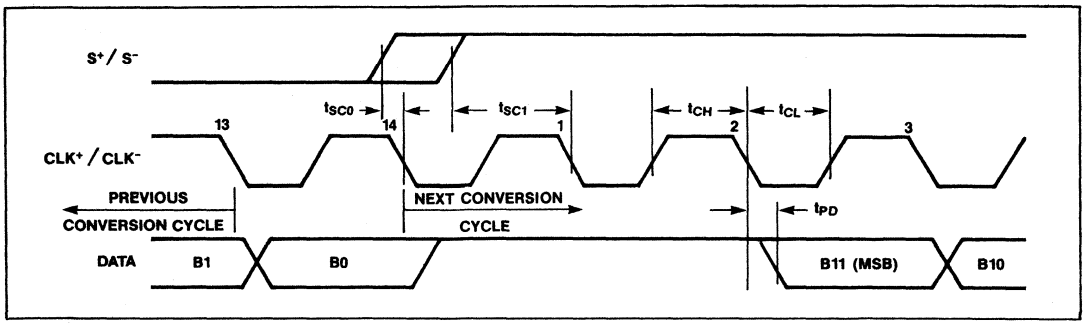


Figure 5. MAX171 Timing Diagram

Conversion Start Timing

Conversion start transitions must arrive within the setup limits t_{SCO} and t_{SC1} relative to the falling edge of the Clock. This guarantees that the serial DATA output stream starts at the second Clock cycle, as shown in Figure 5. Limits on t_{SCO} and t_{SC1} apply whether a conversion is started directly after a previous cycle on the 14th Clock, or if idle Clock pulses occur between conversions. Note that bringing the Start input high on the falling edge of the 14th Clock cycle allows the maximum time for the internal DAC to settle.

Output Coding

The data output from MAX171 is in Straight Binary Code. Other common binary codes, such as 2's complement, offset binary or complementary codes, can be obtained by inverting either the serial data, or the appropriate bit(s) of the parallel data in software or hardware.

Applications

Unipolar Input Operation

Figure 6 shows the nominal input/output transfer function of the MAX171. Code transitions occur halfway between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 7. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS - 3/2LSB (4.9817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

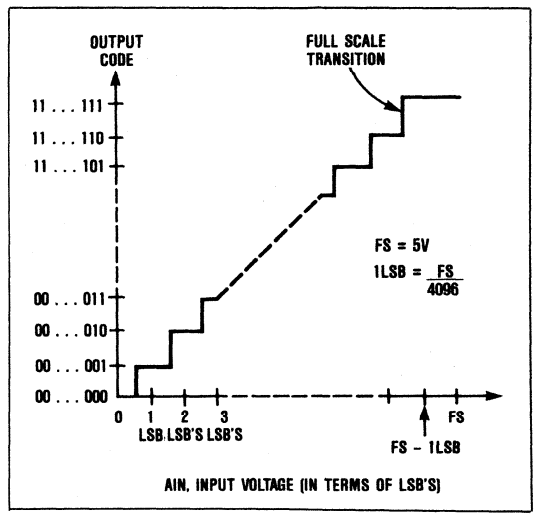


Figure 6. MAX171 Transfer Function

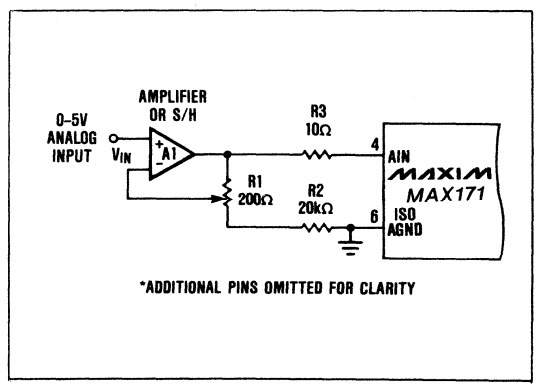


Figure 7. Full-Scale Adjustment

Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

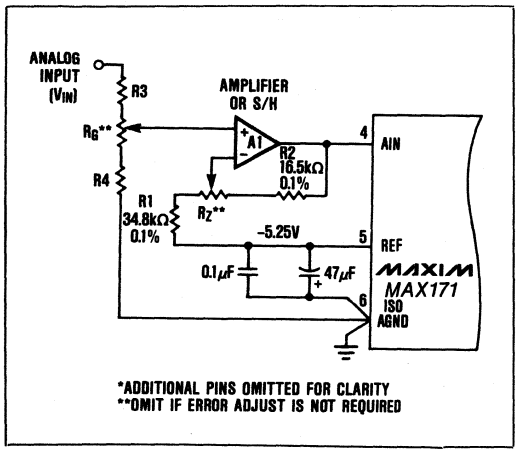


Figure 8. MAX171 Non-Inverting Bipolar Operation

Table 1. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 8

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

*R3 and R4 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

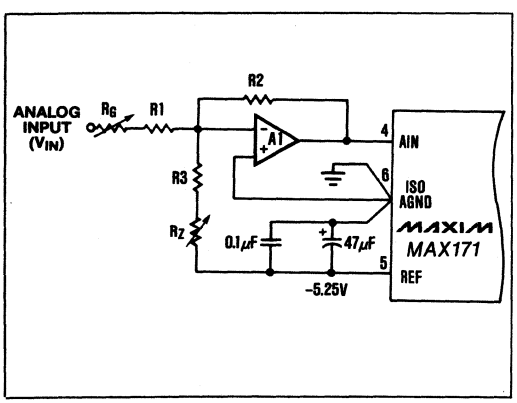


Figure 9. MAX171 Inverting Bipolar Operation

Table 2. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 9

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2 -3/2 LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

*R1, R2 and R3 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases, the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 1 and 2.

Figure 8 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 10 shows the ideal transfer function for this mode.

Figure 9 shows the bipolar operation in the inverting mode where the output coding is complementary offset binary. Figure 10 shows the ideal transfer function for the circuit in Figure 9.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drift. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see Tables 1 and 2) and adjust R_Z until the output code flickers bewteen the following codes:

For Non-Inverting (Figure 8) 1000 0000 0000
1000 0000 0001

For Inverting (Figure 9) 0111 1111 1111
0111 1111 1110

Apply FS - 3/2LSB (See Tables 1 and 2) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-Inverting (Figure 8) 1111 1111 1110
1111 1111 1111

For Inverting (Figure 9) 0000 0000 0001
0000 0000 0000

Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

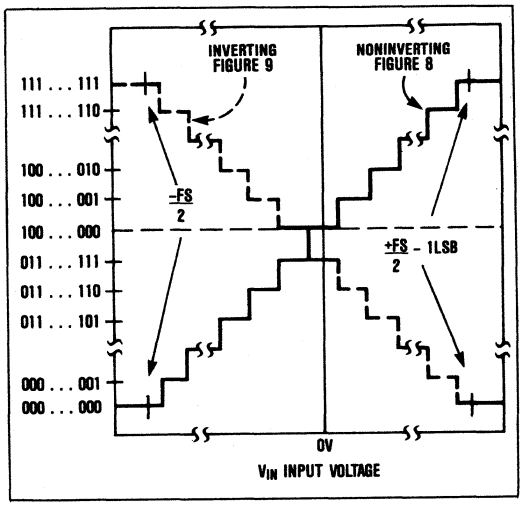


Figure 10. Ideal Input/Output Transfer Characteristics for the Bipolar Circuits in Figures 8 and 9

MAX171 to Sample-and-Hold Interface

The analog input to the MAX171 must be stable to within ±1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a few Hertz for sinusoidal inputs. For higher bandwidth signals a sample-and-hold should be used.

The signal that starts a conversion can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. Note that this signal is not available on the isolated side of the barrier and must be separately coupled. The MAX171's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal, otherwise code dependent errors will be observed. These can be avoided by starting the MAX171 slightly after the TRACK/HOLD signal by using a gate delay. For synchronous conversion start and CK^+, CK^- as described above, the maximum allowable hold settling time for the sample-and-hold is 600ns.

Circuit Layout

For best system performance printed circuit boards should be used for the MAX171. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX171 package.

The pin configuration of the MAX171 is designed to provide optimum electrical isolation in printed circuit layouts. To maintain this capability, connections from the analog side (Pins 1-8) of the A/D should be separated from the digital side (Pins 9-16) and should not reach or run underneath the package. In some cases it may be best to "notch" or cut out the circuit board material to form an air gap between the pin rows.

Grounding

No special precautions are necessary for the ground connection on the digital side of the MAX171. Connect GND (Pin 10) near the ground of the device that will receive the data. The isolated analog ground (ISO AGND, Pin 6) must be connected to the isolated digital ground pins (ISO DGND, Pins 1 and 8), and together they should be tied to the ground of the analog signal. No connection is needed between GND (Pin 10) and the isolated grounds.

Power-Supply Bypassing

The comparator in the MAX171 is sensitive to high frequency noise in the analog power supplies (ISO V^+, ISO V^-). These supplies should be bypassed close to the device with 0.1µF and 10µF capacitors with minimum lead length. If ISO V^+ is very noisy, a small resistor (10Ω to 20Ω) or inductor can be connected in series to form a low-pass filter with the by-pass capacitors. The digital +5V supply (V_{CC}) should be bypassed to GND with 0.1µF for best performance.

Internal Reference

The MAX171's on-chip reference is laser-trimmed to -5.25V ±1%. The reference output is available at REF (Pin 5) as a reference source for other components and also drives the internal DAC.

For minimum noise, REF must be bypassed with a 47µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor to maintain a low impedance at high frequencies (Figure 1). This capacitance also stabilizes the internal reference buffer amplifier preventing oscillations. No series resistance should be used between REF and the bypass capacitors.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, amplifiers like the OP-42, AD711, or OP-27 are recommended. At a 1MHz clock rate, a MAX400 or OP-07 can be used.

LH17 Module Product Reliability

For reliability data on Maxim's Module Product Line, consult factory for Reliability Report RR-4A.

Complete 10μs CMOS 12-Bit ADC

General Description

The MAX172 is a complete 12-Bit analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 10μs. The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX172 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

- ◆ 12-Bit Resolution and Linearity
- ◆ 10μs Conversion Time
- ◆ No Missing Codes
- ◆ On-Chip Voltage Reference
- ◆ 90ns Access Time
- ◆ 215mW Max Power Consumption
- ◆ 24-Lead Narrow DIP Package
- ◆ Pin-for-Pin AD7572 Replacement

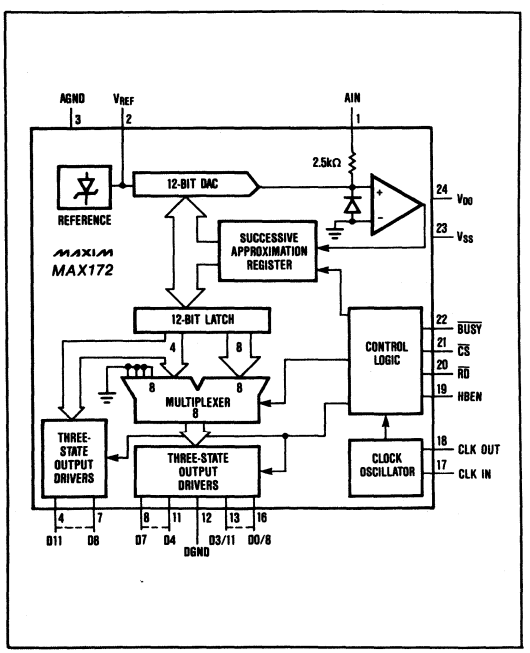
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX172ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX172BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX172ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX172BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX172CC/D	0°C to +70°C	Dice**	±1 LSB
MAX172AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX172BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX172AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX172BMRG	-55°C to +125°C	CERDIP	±1 LSB

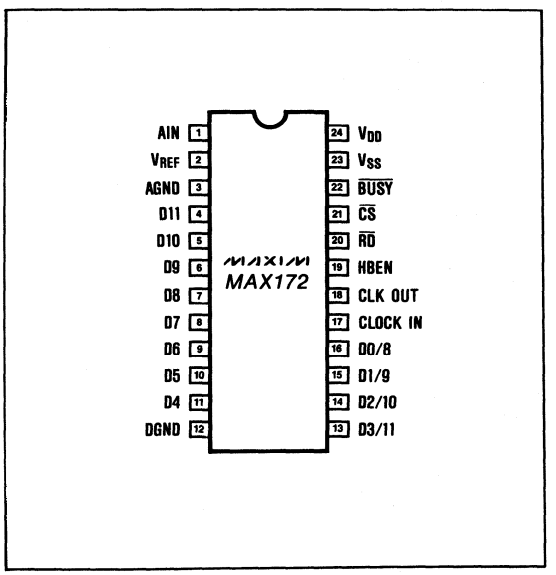
* *All devices — 24 lead packages*

** *Consult factory for dice specifications*

Functional Diagram



Pin Configuration



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Complete 10μs CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX172XC ..... 0°C to +70°C
MAX172XI ..... -25°C to +85°C
MAX172XM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral NonLinearity	INL	MAX172A	T_A = 25°C			±1/2	LSB
		MAX172AC/AI MAX172AM MAX172B				±1/2 ±3/4 ±1	
Differential NonLinearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX172B	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±6	LSB
		MAX172A	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±3 ±4	
Full Scale Error (Note 2)		MAX172B	T_A = 25°C			±15	LSB
		MAX172A	T_A = 25°C			±10	
Full Scale Tempco (Notes 3, 4)						±45	ppm/°C
ANALOG INPUT							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)					40		ppm/°C
Output Current Sink Capability		(Note 6)				500	μA
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	μA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200μA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	μA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION TIME						
MAX172	t_{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 9.6		10 10.4	μs
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V		±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V, V_{SS} = -5% to +5%		±1/8		LSB
POWER REQUIREMENTS						
V_{DD}		±5% for Specified Performance		5		V
V_{SS} (Note 8)		±5% for Specified Performance		-12 or -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1 LSB.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB.
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: Functional operation at V_{SS} = -12V ± 5% is guaranteed by testing offset error and full scale error.

TIMING CHARACTERISTICS (Note 9)

(V_{DD} = +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

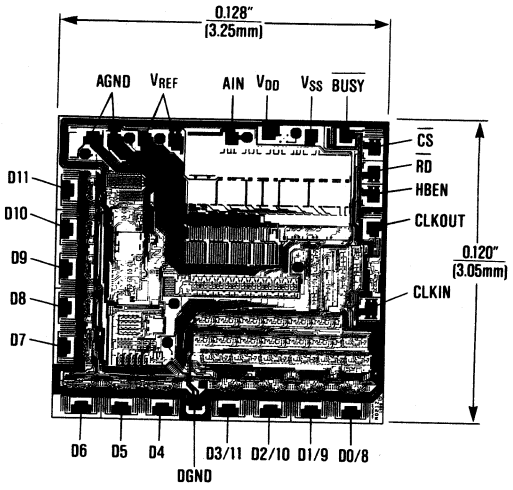
PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX172C/I		MAX172M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX172 please refer to MAX162 data sheet.

Complete 10μs CMOS 12-Bit ADC

Chip Topography



19-2765; Rev. 1; 5/91

MAXIM

Industry Standard Complete 12-Bit A/D Converters

General Description

The MAX174 and the MX574A/MX674A are complete 12-bit analog-to-digital converters (ADCs) that combine high speed, low-power consumption, and on-chip clock and voltage reference. The maximum conversion times are 8µs (MAX174), 15µs (MX674A) and 25µs (MX574A). Maxim's BiCMOS construction reduces power dissipation 3 times (150mW) over comparable devices. The internal buried zener reference provides low-drift and low-noise performance. External component requirements are limited to only decoupling capacitors and fixed resistors. The versatile analog input structure allows for 0V to +10V or 0V to +20V unipolar or ±5V or ±10V bipolar input ranges with pin strapping.

The MAX174/MX574A/MX674A use standard microprocessor interface architectures and can be interfaced to 8-, 12- and 16-bit wide buses. Three-state data outputs are controlled by $\overline{CS}$, CE and R/$\overline{C}$ logic inputs.

Applications

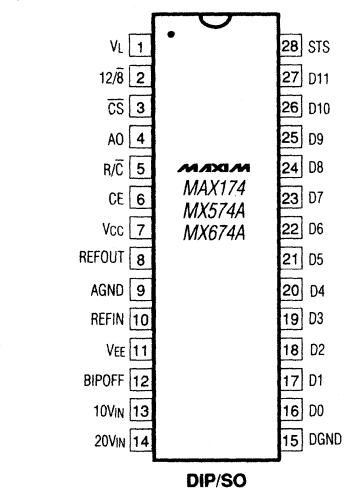
Digital Signal Processing

High-Accuracy Process Control

High-Speed Data Acquisition

Electro-Mechanical Systems

Pin Configurations



Pin Configurations continued on page 15.

Features

- ♦ **Complete ADC with Reference and Clock**
- ♦ **12-Bit Resolution and Linearity**
- ♦ **No Missing Codes Over Temperature**
- ♦ **150mW Power Dissipation**
- ♦ **8µs (MAX174), 15µs (MX674A) and 25µs (MX574A) Max Conversion Times**
- ♦ **Precision Low TC Reference: 10ppm/°C**
- ♦ **Monolithic BiCMOS Construction**
- ♦ **150ns Maximum Data Access Time**

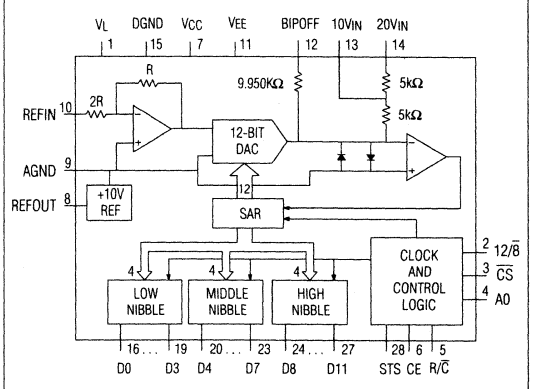
Ordering Information

PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/°C)
8µs Maximum Conversion Time			
TEMP. RANGE: 0°C to +70°C			
MAX174ACPI	28 Plastic DIP	1/2	10
MAX174BCPI	28 Plastic DIP	1/2	27
MAX174CCPI	28 Plastic DIP	1	50
MAX174ACWI	28 Wide SO	1/2	10
MAX174BCWI	28 Wide SO	1/2	27
MAX174CCWI	28 Wide SO	1	50
MAX174BC/D	Dice*	1/2	--

**Consult factory for dice specifications.*

Ordering information continued on page 1-116.

Functional Diagram



Industry Standard Complete 12-Bit A/D Converters

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND ..... 0V to +16.5V
V_{EE} to DGND ..... 0V to -16.5V
V_L to DGND ..... 0V to +7V
DGND to AGND ..... ±1V
Control Inputs to DGND ..... -0.3V to V_{CC} +0.3V
(CE, CS, A0, 12/8, R/C)
Digital Output Voltage to DGND ..... -0.3V, V_L +0.3V
(DB11-DB0, STS)
Analog Inputs to AGND ..... ±16.5V
(REFIN, BIPOFF, $10V_{IN}$)
$20V_{IN}$ to AGND ..... ±24V
REFOUT ..... Indefinite short to V_{CC} or AGND
Power Dissipation (any package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Operating Temperature Ranges:
MAX174_C, MX_74AJ/K/L ..... 0°C to +70°C
MAX174_E, MX_74AJE/KE/LE ..... -40°C to +85°C
MAX174_M, MX_74AS/T/U ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX174

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	MAX174A/B MAX174C			±1/2 ±1	LSB
		$T_A = T_{MIN}$ to T_{MAX}	MAX174AC/BC MAX174AE/BE/AM/BM MAX174C			±1/2 ±3/4 ±1	LSB
Differential Nonlinearity	DNL	12 bits, no missing codes over temp				±1	LSB
Unipolar Offset Error (Note 1)		MAX174A/B MAX174C				±1 ±2	LSB
Bipolar Offset Error (Notes 2, 3)		MAX174A MAX174B/C				±2 ±4	LSB
Full-Scale Calibration Error (Note 3)						±0.25	%
TEMPERATURE COEFFICIENTS (Using Internal Reference, Notes 2, 3, 4)							
Unipolar Offset Change		MAX174A/B MAX174C				±1 ±2	LSB
Bipolar Offset Change		MAX174AC/BC MAX174CC				±1 ±2	LSB
		MAX174AE/AM MAX174BE/BM MAX174CE/CM				±1 ±2 ±4	LSB

Note 1: Adjustable to zero.
Note 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.
Note 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.
Note 4: Maximum change in specification from T_A = +25°C to T_{MIN} or T_A = +25°C to T_{MAX}.
Note 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.

ELECTRICAL CHARACTERISTICS – MAX174 (continued)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Calibration Change		MAX174AC				±2 (10)	LSB (ppm/°C)
		MAX174BC				±5 (27)	
		MAX174CC				±9 (50)	
		MAX174AE				±5 (19)	
		MAX174BE				±10 (38)	
		MAX174CE				±20 (75)	
		MAX174AM				±5 (12)	
		MAX174BM				±10 (25)	
		MAX174CM				±20 (50)	
INTERNAL REFERENCE							
Output Voltage		No Load	MAX174A MAX174B/C	9.98 9.97	10.00 10.00	10.02 10.03	V
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load				2	mA

ELECTRICAL CHARACTERISTICS – MX574A, MX674A

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	MX574AK/L/T/U, MX674AK/L/T/U MX574AJ/S, MX674AJ/S			±1/2 ±1	LSB
		$T_A = T_{MIN}$ to T_{MAX}	MX574AK/L/KE/LE MX674AK/L/KE/LE MX574AT/U, MX674AT/U MX574AJ/S, MX674AJ/S			±1/2 ±1/2 ±3/4 ±1	
Differential Nonlinearity	DNL	12 bits, no missing codes over temp				±1	LSB

Industry Standard Complete 12-Bit A/D Converters

ELECTRICAL CHARACTERISTICS – MX574A, MX674A (continued)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unipolar Offset Error (Note 1)		MX574AK/L/T/U, MX674AK/L/T/U MX574AJ/S, MX674AJ/S			±1 ±2	LSB
Bipolar Offset Error (Notes 2, 3)		MX574AL/U, MX674AL/U MX574AJ/K/S/T, MX674AJ/K/S/T			±2 ±4	LSB
Full-Scale Calibration Error (Note 3)		MX574AL/U MX574AJ/K/S/T, MX674A			±0.125 ±0.25	%
TEMPERATURE COEFFICIENTS (Using Internal Reference, Notes 2, 3, 4)						
Unipolar Offset Change		MX574AK/L/T/U, MX674AK/L/T/U MX574AJ/S, MX674AJ/S			±1 ±2	LSB
Bipolar Offset Change		MX574AK/L, MX674AK/L MX574AJ, MX674AJ			±1 ±2	LSB
		MX574AU/LE, MX674AU/LE MX574AT/KE, MX674AT/KE MX574AS/JE, MX674AS/JE			±1 ±2 ±4	
Full-Scale Calibration Change		MX574AL, MX674AL			±2 (10)	LSB (ppm/°C)
		MX574AK, MX674AK			±5 (27)	
		MX574AJ, MX674AJ			±9 (50)	
		MX574ALE, MX674ALE			±5 (19)	
		MX574AKE, MX674AKE			±10 (38)	
		MX574AJE, MX674AJE			±20 (75)	
		MX574AU, MX674AU			±5 (12)	
		MX574AT, MX674AT			±10 (25)	
		MX574AS, MX674AS			±20 (50)	
INTERNAL REFERENCE						
Output Voltage		No Load; MX574AL/U No Load; MX574AJ/K/S/T, MX674AL/U No Load; MX674AJ/K/S/T	9.99 9.98 9.97	10.00 10.00 10.00	10.01 10.02 10.03	V
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load			2	mA

Note 1: Adjustable to zero.
Note 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.
Note 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.
Note 4: Maximum change in specification from T_A = +25°C to T_{MIN} or T_A = +25°C to T_{MAX}.
Note 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.

ELECTRICAL CHARACTERISTICS – MAX174/MX574A/MX674A

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Bipolar Input Range		Using 10V Input			±5	V
		Using 20V Input			±10	
Unipolar Input Range		Using 10V Input	0		+10	V
		Using 20V Input	0		+20	
Input Impedance		10V Input	3	5	7	kΩ
		20V Input	6	10	14	
POWER-SUPPLY REJECTION (Max change in Full-Scale Calibration)						
V_{CC} Only		+15V ±1.5V or +12V ±0.6V; MAX174A/B, MX_74AK/L/TU		±1/8	±1	LSB
		+15V ±1.5V or +12V ±0.6V; MAX174C, MX_74AJ/S		±1/8	±2	
V_{EE} Only		-15V ±1.5V or -12V ±0.6V		±1/8	±1/2	
V_L Only		+5V ±0.5V		±1/8	±1/2	
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$	2.0			V
Input Current	I_{IN}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$, V_{IN} = 0 to V_L			±5	µA
Input Capacitance	C_{IN}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$		7		pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	DB11-DB0, STS; I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	DB11-DB0, STS; I_{SOURCE} = 500µA	4			V
Floating State Leakage Current	I_{LKG}	DB11-DB0, STS; V_{OUT} = 0 to V_L			±10	µA
Floating State Output Capacitance	C_{OUT}	DB11-DB0		8		pF
CONVERSION TIME						
12-Bit Cycle,	t_{CONV}	MX574A	15	20	25	µs
		MX674A	9	12	15	
		MAX174	6	7	8	
8-Bit Cycle	t_{CONV}	MX574A	10	14	18	µs
		MX674A	6	8	11	
		MAX174	4	5	6	
POWER REQUIREMENTS						
VCC Operating Range			11.4		16.5	V
VL Operating Range			4.5		5.5	V
VEE Operating Range			-11.4		-16.5	V
VCC Supply Current (Note 5)	I_{CC}			3	5	mA
VL Supply Current (Note 5)	I_L			3	8	mA
VEE Supply Current (Note 5)	I_{EE}			6	10	mA
Power Dissipation (Note 5)	P_D	V_{CC} = +15V and V_{EE} = -15V		150	265	mW

Industry Standard Complete 12-Bit A/D Converters

TIMING CHARACTERISTICS – MAX174/MX574A/MX674A (Note 6)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C to +85°C T_A = 0°C to +70°C		T_A = -55°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CONVERT START TIMING – FULL CONTROL MODE										
STS Delay from CE	t_{DSC}	C_L = 50pF		100	200		250		320	ns
CE Pulse Width	t_{HEC}		50	15		50		50		ns
$\overline{CS}$ to CE Setup	t_{SSC}		50			50		50		ns
$\overline{CS}$ Low During CE High	t_{HSC}		50			50		50		ns
R/$\overline{C}$ to CE Setup	t_{SRC}		50			50		50		ns
R/$\overline{C}$ Low During CE High	t_{HRC}		50			50		50		ns
A0 to CE Setup	t_{SAC}		0			0		0		ns
A0 Valid During CE High	t_{HAC}		50			50		50		ns
READ TIMING – FULL CONTROL MODE										
Access Time (from CE)	t_{DD}	C_L = 100pF		60	120		150		200	ns
Data Valid after CE Low	t_{HD}		25	40		20		15		ns
Output Float Delay	t_{HL}				75		100		120	ns
$\overline{CS}$ to CE Setup	t_{SSR}		50			50		50		ns
R/$\overline{C}$ to CE Setup	t_{SRR}		0			0		0		ns
A0 to CE Setup	t_{SAR}		50			50		50		ns
$\overline{CS}$ Valid After CE Low	t_{HSR}		0			0		0		ns
R/$\overline{C}$ High After CE Low	t_{HRR}		0			0		0		ns
A0 Valid After CE Low	t_{HAR}		0			0		0		ns
STAND-ALONE MODE										
Low R/$\overline{C}$ Pulse Width	t_{HRL}		50	15		50		50		ns
STS Delay from R/$\overline{C}$	t_{DS}			115	200		250		320	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}		25	40		20		15		ns
STS Delay After Data Valid	t_{HS}	MX574A	300	600	1000	300	1000	300	1000	ns
		MX674A	30	320	600	30	600	30	600	
		MAX174	30	140	300	30	300	30	400	
High R/$\overline{C}$ Pulse Width	t_{HRH}		150			150		200		ns
Data Access Time	t_{DDR}	C_L = 100pF		60	120		150		200	ns

Note 6: Timing specifications guaranteed by design. All input control signals specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. See loading circuits in Figures 1 and 2.

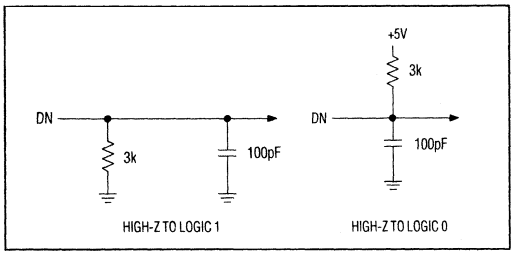


Figure 1. Load Circuit for Access Time Test

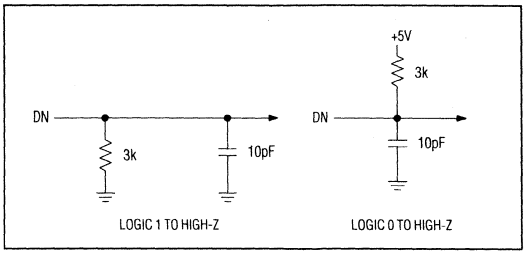


Figure 2. Load Circuit for Output Float Delay Test

Pin Description

PIN #	NAME	FUNCTION
1	V_L	Logic Supply, +5V
2	12/8	Data Mode Select Input
3	$\overline{CS}$	Chip-Select Input. Must be low to select device.
4	A0	Byte Address/Short Cycle Input. When starting a conversion, controls number of bits converted (low = 12 bits, high = 8 bits). When reading data, if 12/8 = low, enables low byte (A0 = high) or high byte (A0 = low).
5	R/$\overline{C}$	Read/Convert Input. When high, the device will be in the data-read mode. When low, the device will be in the conversion start mode.
6	CE	Chip-Enable Input. Must be high to select device.
7	V_{CC}	+12V or +15V Supply
8	REFOUT	+10V Reference Output
9	AGND	Analog Ground
10	REFIN	Reference Input
11	V_{EE}	-12V or -15V Supply
12	BIPOFF	Bipolar Offset Input. Connect to REFOUT for bipolar input range.
13	$10V_{IN}$	10V Span Input
14	$20V_{IN}$	20V Span Input
15	DGND	Digital Ground
16-27	D0-D11	Three-State Data Outputs
28	STS	Status Output

Converter Operation

The MAX174/MX574A/MX674A use a successive approximation technique to convert an unknown analog input to a 12-bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital (A/D) function.

The internal voltage output DAC is controlled by a Successive Approximation Register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 5kΩ resistor for the 10V input and 10kΩ resistor for the 20V input. The comparator is essentially a zero crossing detector, and its output is fed back to the SAR input.

The SAR is set to half scale as soon as a conversion starts. The analog input is compared to 1/2 of the full-scale voltage. The bit is kept if the analog input is greater than half scale or dropped if smaller. The next bit, bit 10, is then set with the DAC output either at 1/4 scale, if the Most Significant Bit (MSB) is dropped, or 3/4 scale if the MSB is kept. The conversion continues in this manner until the Least Significant Bit (LSB) is tried. At the end of the conversion, the SAR output is latched into the output buffers.

Digital Interface

CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the MAX174/MX574A/MX674A. While both CE and $\overline{CS}$ are asserted, the state of R/$\overline{C}$ selects whether a conversion (R/$\overline{C}$ = 0) or a data read (R/$\overline{C}$ = 1) is in progress. The register control inputs, 12/$\overline{8}$ and A0, select the data format and conversion length. A0 is usually tied to the LSB of the address bus. To perform a full 12-bit conversion, set A0 low during a convert start. For a shorter 8-bit conversion, A0 must be high during a convert start.

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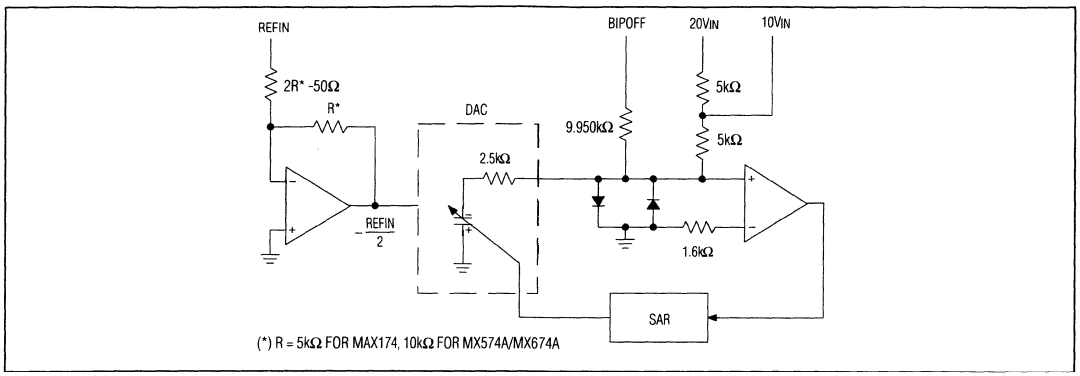


Figure 3. Analog Equivalent Circuit

Table 1. Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8MSBs
1	0	1	0	1	Enable 4LSBs + 4 trailing 0s

Output Data Format

During a data read, A0 also selects whether the three-state buffers contain the 8MSBs (A0 = 0) or the 4LSBs (A0 = 1) of the digital result. The 4LSBs are followed by 4 trailing 0s.

Output data is formatted according to the 12/$\overline{8}$ pin. If this input is low, the output will be a word broken into two 8-bit bytes. This allows direct interface to 8-bit buses without the need for external three-state buffers. If 12/$\overline{8}$ is high, the output will be one 12-bit word. A0 can change state while a data-read operation is in effect.

To begin a conversion, the microprocessor must write to the ADC address. Then, since a conversion usually takes longer than a single clock cycle, the microprocessor must wait for the ADC to complete the conversion. Valid data will be made available only at the end of the conversion, which is indicated by STS. STS can be either polled or used to generate an interrupt upon completion. Or, the microprocessor can be kept idle by inserting the appropriate number of No OPeration (NOP) instructions between the conversion-start and data-read commands.

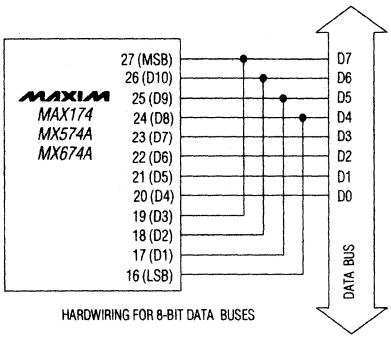
After the conversion is completed, data can be obtained by the microprocessor. The ADCs have the required logic for 8-, 12- and 16-bit bus interfacing, which is determined by the 12/$\overline{8}$ input. If 12/$\overline{8}$ is high, the ADCs are configured for a 16-bit bus. Data lines D0-D11 may be connected to the bus as either the 12MSBs or the 12LSBs. The other 4 bits must be masked out in software.

For 8-bit bus operation, 12/$\overline{8}$ is set low. The format is left justified, and the even address, A0 low, contains the 8MSBs. The odd address, A0 high, contains the 4LSBs, which is followed by 4 trailing 0s. There is no need to use a software mask when the ADCs are connected to an 8-bit bus.

Note that the output cannot be forced to a right-justified format by rearranging the data lines on the 8-bit bus interface.

Table 2. MAX174/MX574A/MX674A Data Format for 8-Bit Bus

	D7	D6	D5	D4	D3	D2	D1	D0
High Byte (A0 = 0)	MSB	D10	D9	D8	D7	D6	D5	D4
Low Byte (A0 = 1)	D3	D2	D1	D0	0	0	0	0



HARDWIRING FOR 8-BIT DATA BUSES

Timing and Control

Convert Start Timing - Full Control Mode

R/$\overline{C}$ must be low before asserting both CE and $\overline{CS}$. If it is high, a brief read operation occurs possibly resulting in system bus contention. To initiate a conversion, use either CE or $\overline{CS}$. CE is recommended since it is shorter by one propagation delay than $\overline{CS}$ and is the faster input of the two. CE is used to begin the conversion in Figure 4.

Once STS goes high, signaling that a conversion has started, all convert start commands will have no effect until the conversion is finished. Also, the output data buffers cannot be enabled during a conversion.

Read Timing - Full Control Mode

Figure 5 illustrates the read-cycle timing. While reading data, access time is measured from when CE and R/$\overline{C}$ are both high. Access time is extended 10ns if $\overline{CS}$ is used to initiate a read.

Stand-Alone Operation

For systems which do not use or require full bus interfacing, the MAX174/MX574A/MX674A can be operated in a stand-alone mode directly linked through dedicated input ports.

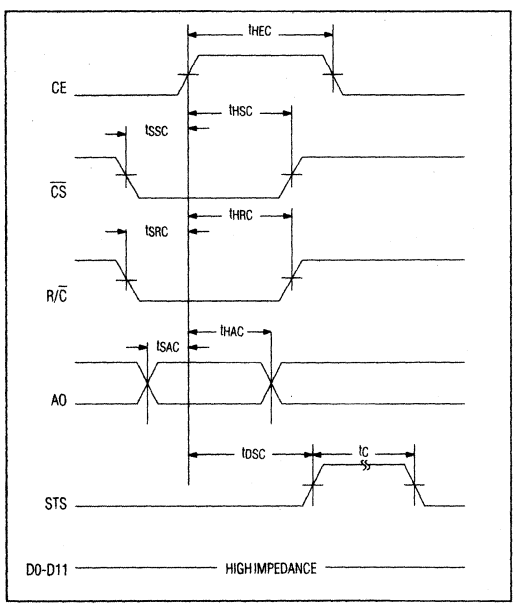


Figure 4. Convert Start Timing

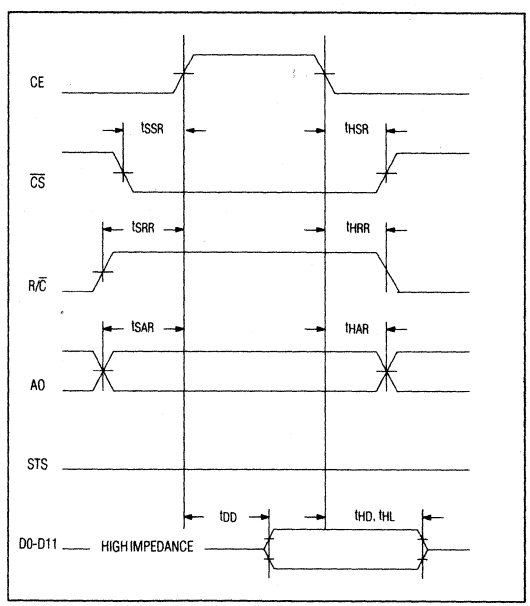


Figure 5. Read Timing

7

Industry Standard Complete 12-Bit A/D Converters

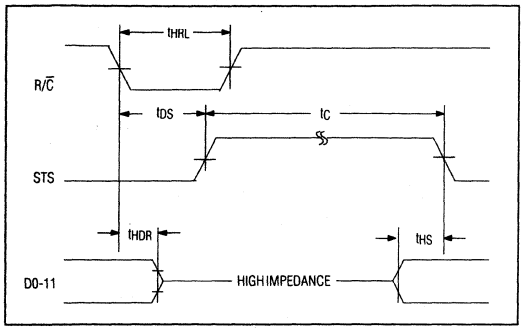


Figure 6. Low Pulse for R/C in Stand-Alone Mode

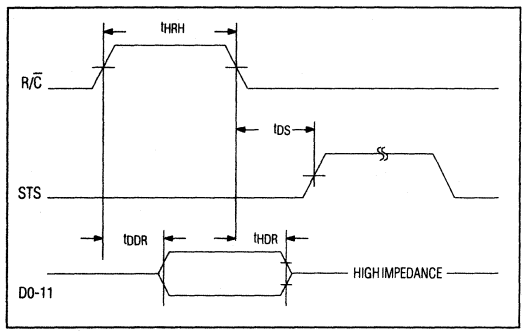


Figure 7. High Pulse for R/C in Stand-Alone Mode

When configured in the stand-alone mode, conversion is controlled by R/C. In addition, CS and A0 are wired low; CE and 12/8 are wired high. To enable the three-state buffers, set R/C low. A conversion starts when R/C is set high. This allows either a high- or a low-pulse control signal. Shown in Figure 6 is the operation with a low pulse. In this mode, the outputs, in response to the falling edge of R/C, are forced into the high impedance state and return to valid logic levels after the conversion is complete. The STS output goes high following R/C falling edge and returns low when the conversion is complete.

A high-pulse conversion initiation is illustrated in Figure 7. When R/C is high, the data lines are enabled. The next conversion starts with the falling edge of R/C. The data lines return and remain "high impedance state" until another R/C high pulse.

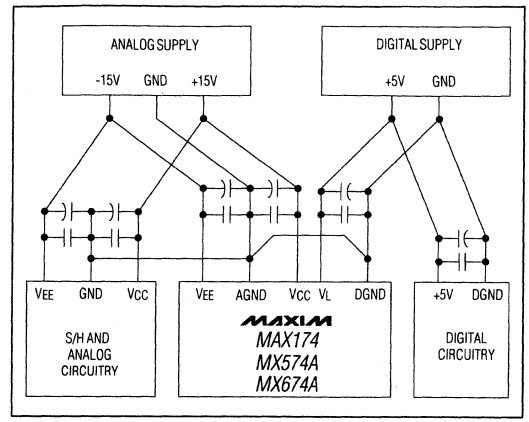


Figure 8. Power-Supply Grounding Practice

Analog Considerations

Application Hints

Physical Layout

For best system performance, printed circuit boards should be used for the MAX174/MX574A/MX674A. Wire-wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX174/MX574A/MX674A.

Grounding

The recommended power-supply grounding practice is shown in Figure 8. The ground reference point for the on-chip reference is AGND. It should be connected directly to the analog reference point of the system. The analog and digital grounds should be connected together at the package in order to gain all of the accuracy possible from the MAX174/MX574A/MX674A in high digital noise environments. In situations permitting, they can be connected to the most accesssible ground reference point. The preference is analog power return.

Power-Supply Bypassing

The MAX174/MX574A/MX674A power supplies must be filtered, well regulated, and free from high-frequency noise, or unstable output codes will result. Unless great care is taken in filtering any switching spikes present in the output, switching power supplies is not suggested for applications requiring 12-bit resolution. Take note that a few millivolts of noise converts to several error counts in a 12-bit ADC.

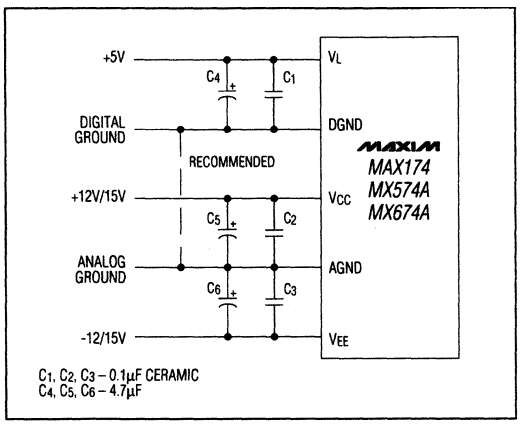


Figure 9. Power-Supply Bypassing

All power-supply pins should use supply decoupling capacitors connected with short lead length to the pins, as shown in Figure 9. The V_{CC} and V_{EE} pins should be decoupled directly to AGND. A 4.7µF tantalum type in parallel with a 0.1µF disc ceramic type is a suitable decoupling.

Internal Reference

The MAX174/MX574A/MX674A have an internal buried zener reference that provides a 10V, low-noise and low-temperature drift output. An external reference voltage can also be used for the ADC. When using ±15V supplies, the internal reference can source up to 2mA in addition to the BIPOFF and REFIN inputs over the entire operating temperature range. With ±12V supplies, the reference can drive the BIPOFF and REFIN inputs over temperature, but it CANNOT drive an additional load.

Driving the Analog Input

The input leads to AGND and $10V_{IN}$ or $20V_{IN}$ should be as short as possible to minimize noise pick up. If long leads are needed, use shielded cables.

When using the $20V_{IN}$ as the analog input, load capacitance on the $10V_{IN}$ pin must be minimized. Especially on the faster MAX174, leave the $10V_{IN}$ pin open to minimize capacitance and to prevent linearity errors caused by inadequate settling time.

The amplifier driving the analog input must have low enough DC output impedance for low full-scale error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during the conversion. The output impedance of an amplifier is the open-loop output impedance divided by the loop gain at the frequency of interest.

MX574A and MX674A - The approximate internal clock rate is 600kHz and 1MHz respectively, and amplifiers like the MAX400 can be used to drive the input.

MAX174 - The internal clock rate is 2MHz and faster amplifiers like the OP-27, AD711 or OP-42 are required.

Track-and-Hold Interface

The analog input to the ADC must be stable to within 1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a

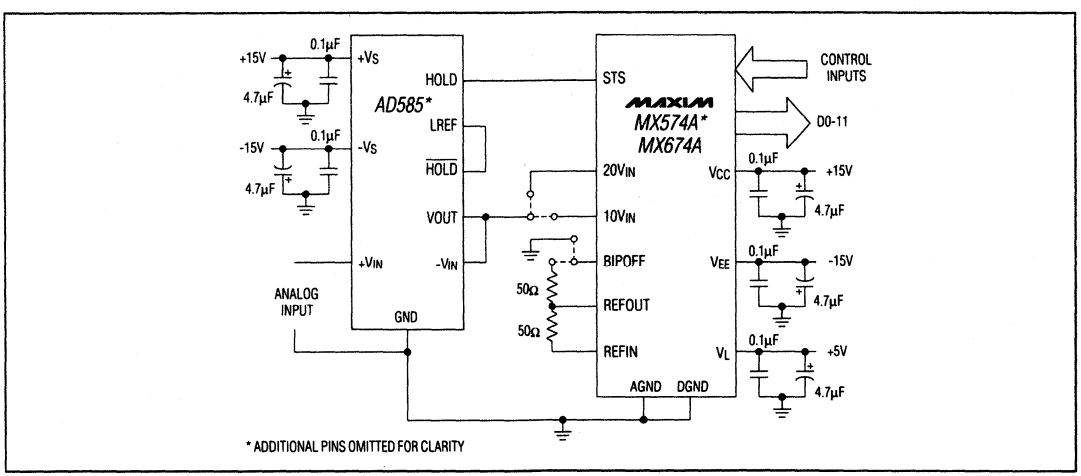


Figure 10. MX574A/MX674A to AD585 Sample-and-Hold Interface

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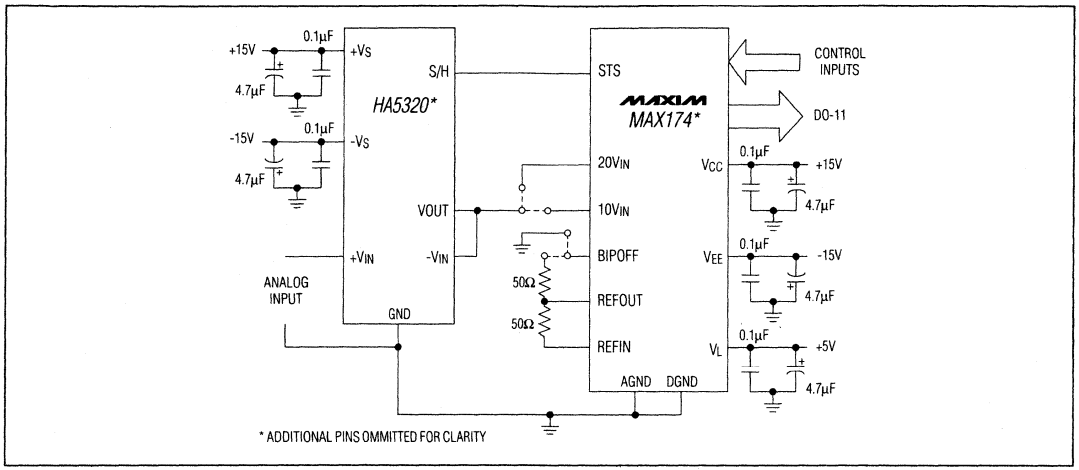


Figure 11. MAX174 to HA5320 Sample-and-Hold Interface

couple of hertz for sinusoidal inputs even with the faster MAX174. For higher bandwidth signals, a track-and-hold amplifier should be used.

The STS output may be used to provide the Hold signal to the track-and-hold amplifier. However, since the A/D's DAC is switched at approximately the same time as the conversion is initiated, the switching transients at the output of the T/H caused by the DAC switching may result in code dependent errors. It is recommended that the Hold signal to the T/H amplifier precede a conversion or be coincident with the conversion start.

The first bit decision by the A/D is made approximately 1.5 clock cycles after the start of the conversion. This is 2.5µs, 1.5µs and 0.8µs for the MX574A, MX674A, and MAX174 respectively. The T/H hold settling time must be less than this time. For the MX574A and MX674A, the AD585 sample-and-hold is recommended (Figure 10). For the MAX174, a faster T/H amplifier, like the HA5320 or HA5330, should be used (Figure 11).

Input Configurations

The MAX174/MX574A/MX674A input range can be set using pin strapping. Table 3 shows the possible input ranges and ideal transition voltages. End-point errors can be adjusted in all ranges.

Table 3. Input Ranges and Ideal Digital Output Codes

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to +10V	0 to +20V	±5V	±10V	MSB LSB
+10.0000	+20.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111 1111 1110*
+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 0000*
+4.9988	+9.9976	-0.0012	-0.0024	0111 1111 1111*
+4.9963	+9.9927	-0.0037	-0.0073	0111 1111 1110*
+0.0012	+0.0024	-4.9988	-9.9976	0000 0000 0000*
0.0000	0.0000	-5.0000	-10.0000	0000 0000 0000

Note 1: For unipolar input ranges, output coding is straight binary.
Note 2: For bipolar input ranges, output coding is offset binary.
Note 3: For 0V to +10V or ±5V ranges, 1LSB = 2.44mV.
Note 4: For 0V to +20V or ±10V ranges, 1LSB = 4.88mV.

* The digital outputs will be flickering between the indicated code and the indicated code plus one.

Unipolar Input Operation

The unipolar transfer function and input connections are shown in Figures 12 and 13.

Because all internal resistors of the MAX174/MX574A/MX674A are trimmed for absolute calibration, additional trimming is not necessary for most applications. The absolute accuracy for each grade is given in the specification tables.

If the offset trim is not needed, BIPOFF can be tied directly to AGND. The two resistors and trimmer for BIPOFF can then be discarded. A 50Ω ±1% metal film resistor should be attached between REFOUT and REFIN.

For a 0V to +10V input range, the analog input is connected between AGND and 10VIN. For a 0V to +20V input range, the analog input is connected between AGND and 20VIN. These ADCs can easily handle an input signal beyond the supplies. If full-scale trim is not needed, the gain trimmer, R2, should be swapped with a 50Ω resistor. Should a 10.24V input range be selected, a 200Ω trimmer should be inserted in series with 10VIN. For a full-scale input range of 20.48V, use a 500Ω trimmer in series with 20VIN. The nominal input impedance into 10VIN is 5kΩ and 10kΩ for 20VIN.

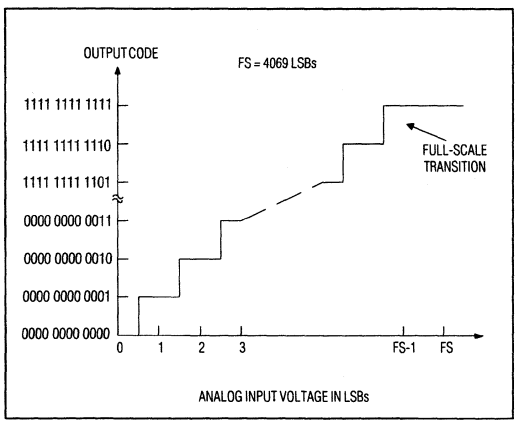


Figure 12. Ideal Unipolar Transfer Function

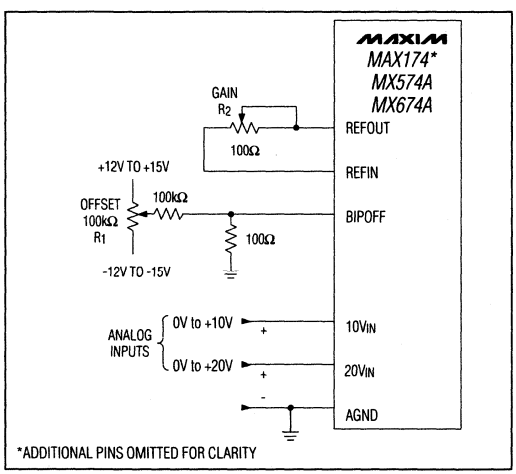


Figure 13. Unipolar Input Connections

Offset and Full-Scale Adjustment

In applications where the offset and full-scale range have to be adjusted, use the circuit shown in Figure 12. The offset should be adjusted first. Apply 1/2LSB at the analog input and adjust R1 until the digital output code flickers between 0000 0000 0000 and 0000 0000 0001.

To adjust the full-scale range, apply FS - 3/2LSB at the analog input and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

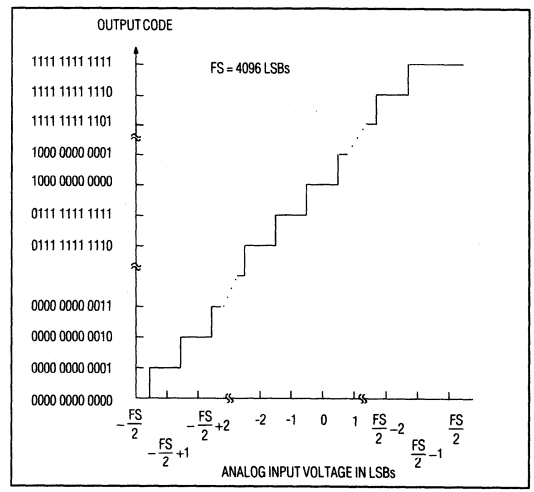


Figure 14. Ideal Bipolar Transfer Function

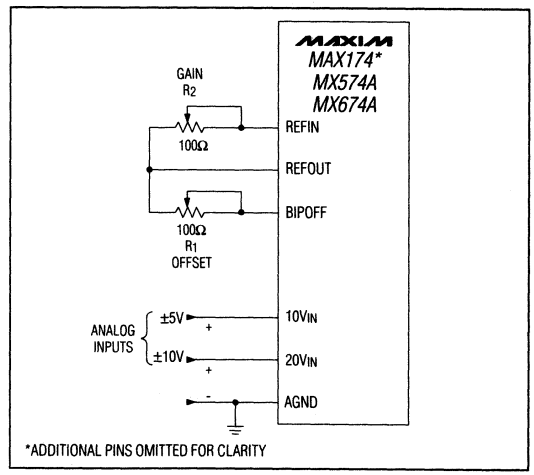


Figure 15. Bipolar Input Connections

Industry Standard Complete 12-Bit A/D Converters

Bipolar Input Operation

The Bipolar transfer function is shown in Figure 14, and input connections are shown in Figure 15. One or both of the trimmers can be exchanged with a 50Ω ±1% fixed resistor if the offset and gain specifications suffice.

Offset and Full-Scale Adjustment

To begin bipolar calibration, a signal 1/2LSB above negative full-scale is applied. R1 is trimmed until the digital output flickers between 0000 0000 0000 and 0000 0000 0001. Next, a signal 3/2LSB below positive full scale is applied. Then, R2 is trimmed until the output flickers between 1111 1111 1110 and 1111 1111 1111.

Ordering Information (continued)

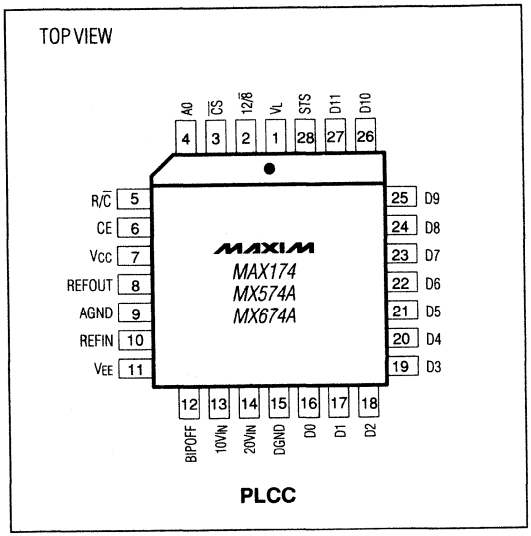
PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/°C)
8µs Maximum Conversion Time			
TEMP. RANGE:	**-40°C to +85°C**		
MAX174AEPI	28 Plastic DIP	1/2	19
MAX174BEPI	28 Plastic DIP	1/2	38
MAX174CEPI	28 Plastic DIP	1	75
MAX174AEWI	28 Wide SO	1/2	19
MAX174BEWI	28 Wide SO	1/2	38
MAX174CEWI	28 Wide SO	1	75
TEMP. RANGE:	**-55°C to +125°C**		
MAX174AMJI	28 CERDIP	3/4	12
MAX174BMJI	28 CERDIP	3/4	25
MAX174CMJI	28 CERDIP	1	50
15µs Maximum Conversion Time			
TEMP. RANGE:	**0°C to +70°C**		
MX674AJN	28 Plastic DIP	1	50
MX674AKN	28 Plastic DIP	1/2	27
MX674ALN	28 Plastic DIP	1/2	10
MX674AJCWI	28 Wide SO	1	50
MX674AKCWI	28 Wide SO	1/2	27
MX674ALCWI	28 Wide SO	1/2	10
MX674AK/D	Dice**	1/2	--
TEMP. RANGE:	**-40°C to +85°C**		
MX674AJEPI	28 Plastic DIP	1	75
MX674AKEPI	28 Plastic DIP	1/2	38
MX674ALEPI	28 Plastic DIP	1/2	19
MX674AJEWI	28 Wide SO	1	75
MX674AKEWI	28 Wide SO	1/2	38
MX674ALEWI	28 Wide SO	1/2	19
TEMP. RANGE:	**-55°C to +125°C**		
MX674ASQ	28 CERDIP*	1	50
MX674ATQ	28 CERDIP*	3/4	25
MX674AUQ	28 CERDIP*	3/4	12

PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/°C)
15µs Maximum Conversion Time			
TEMP. RANGE:	**-55°C to +125°C**		
MX674ASD	28 Ceramic SB	1	50
MX674ATD	28 Ceramic SB	3/4	25
MX674AUD	28 Ceramic SB	3/4	12
25µs Maximum Conversion Time			
TEMP. RANGE:	**0°C to +70°C**		
MX574AJN	28 Plastic DIP	1	50
MX574AKN	28 Plastic DIP	1/2	27
MX574ALN	28 Plastic DIP	1/2	10
MX574AJCWI	28 Wide SO	1	50
MX574AKCWI	28 Wide SO	1/2	27
MX574ALCWI	28 Wide SO	1/2	10
MX574AJP	28 PLCC	1	50
MX574AKP	28 PLCC	1/2	27
MX574ALP	28 PLCC	1/2	10
MX574AK/D	Dice**	1/2	--
TEMP. RANGE:	**-40°C to +85°C**		
MX574AJEPI	28 Plastic DIP	1	75
MX574AKEPI	28 Plastic DIP	1/2	38
MX574ALEPI	28 Plastic DIP	1/2	19
MX574AJEWI	28 Wide SO	1	75
MX574AKEWI	28 Wide SO	1/2	38
MX574ALEWI	28 Wide SO	1/2	19
TEMP. RANGE:	**-55°C to +125°C**		
MX574ASQ	28 CERDIP*	1	50
MX574ATQ	28 CERDIP*	3/4	25
MX574AUQ	28 CERDIP*	3/4	12
MX574ASD	28 Ceramic SB	1	50
MX574ATD	28 Ceramic SB	3/4	25
MX574AUD	28 Ceramic SB	3/4	12

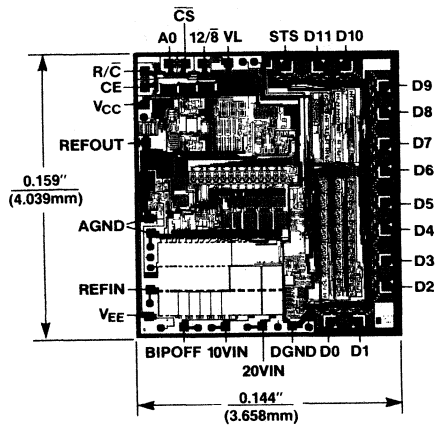
* Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.
** Consult factory for dice specifications.

Industry Standard Complete 12-Bit A/D Converters

Pin Configurations (continued)



Chip Topography



7

ADVANCE INFORMATION
First Page of Data Sheet in Preparation

MAXIM

Serial-Output, 12-Bit 250kS/S ADC

General Description

The MAX176 complete, CMOS, 12-bit sampling analog-to-digital converter combines speed and accuracy with a cost and space saving serial interface. A high-speed track-and-hold (T/H) and successive approximation A/D provide a 3.5µs conversion time and a tested 250kHz sampling rate. An on-chip reference provides low drift performance over the full temperature range.

Supply and reference decoupling capacitors are the only external components required. The CLOCK input can be driven from an external clock source such as a divided-down microprocessor clock. The MAX176 works with +5V and -12V or -15V supply voltages, typically dissipating only 144mW.

The MAX176 is designed to work with serial µP and general-purpose serial-to-parallel converters such as the 74HC595. It also communicates with digital-signal processors such as the TMS32020, TMS320C25, NEC µPD7720 or the DSP5600 via a three-wire serial interface.

Applications

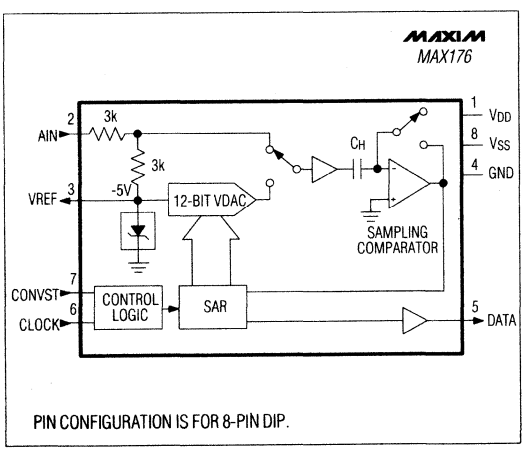
Isolated Industrial Data Acquisition

Telecommunication

Digital-Signal Processing (DSP)

Sonar/Radar Signal Processing

Functional Diagram



PIN CONFIGURATION IS FOR 8-PIN DIP.

Features

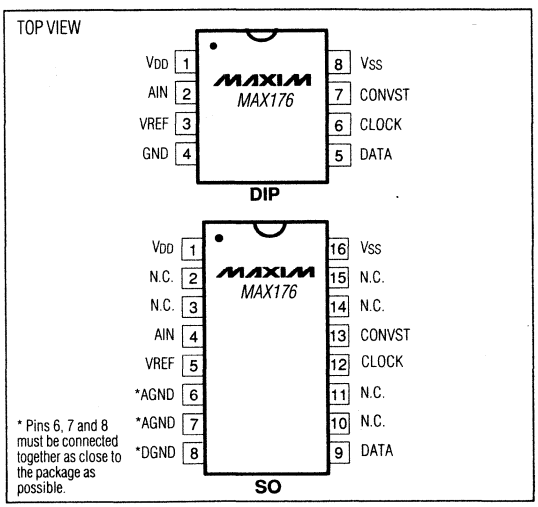
- ♦ **12-Bit Resolution and Linearity**
- ♦ **Internal Track-and-Hold**
- ♦ **3.5µs Conversion, 0.4µs Acquisition Time**
- ♦ **DC and Dynamically Tested**
- ♦ **±5V Bipolar Input Range**
- ♦ **Three-State Serial Output**
- ♦ **On-Chip Reference**
- ♦ **Low Power (144mW Typ)**
- ♦ **Easy to Opto- or Transformer-Isolate**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX176ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX176BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX176ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX176BCWE	0°C to +70°C	16 Wide SO	±1
MAX176BC/D	0°C to +70°C	Dice*	±1
MAX176AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX176BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX176AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX176BEWE	-40°C to +85°C	16 Wide SO	±1
MAX176AMJA	-55°C to +125°C	8 CERDIP	±1/2
MAX176BMJA	-55°C to +125°C	8 CERDIP	±1

** Contact factory for dice specifications.*

Pin Configurations



MAXIM

Calibrated 12-Bit ADC with T/H and Reference

General Description

The MAX178 is a complete, calibrated 12-bit A/D converter (ADC) which includes a precision voltage reference, track-and-hold, and conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each conversion includes an auto-zero cycle which reduces zero errors to typically below 100µV.

$\overline{\text{CHIP SELECT}}$, $\overline{\text{READ}}$, and $\overline{\text{WRITE}}$ inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two converter busy flags facilitate polling of the converter's status.

The MAX178's analog input range is 0V to +5V when using a +5V reference. The MAX178A's internal reference accuracy is ±0.3%, while the MAX178B is intended for use with an external reference.

Applications

Digital-Signal Processing

Audio and Telecom Processing

High-Speed Data Acquisition

High-Accuracy Process Control

Features

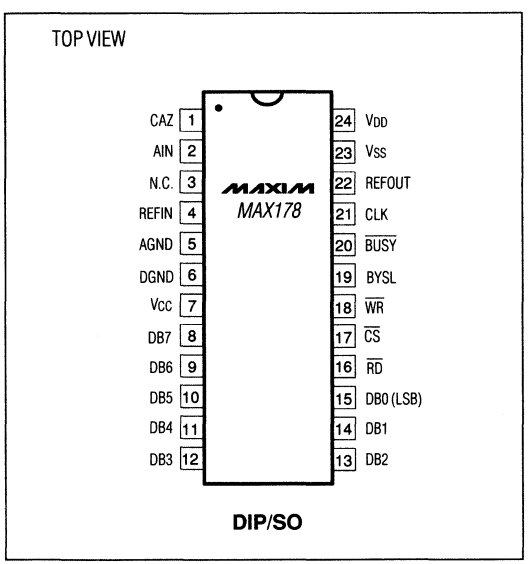
- ♦ **Continuous Transparent Calibration of Offset and Gain**
- ♦ **True 12-Bit Performance without Adjustments**
- ♦ **T/H Front End and Internal Reference**
- ♦ **DC and Dynamically Specified**
- ♦ **Zero Error Typically <100µV**
- ♦ **Standard Microprocessor Interface**
- ♦ **24-Pin DIP and Wide SO Packages**

Ordering Information

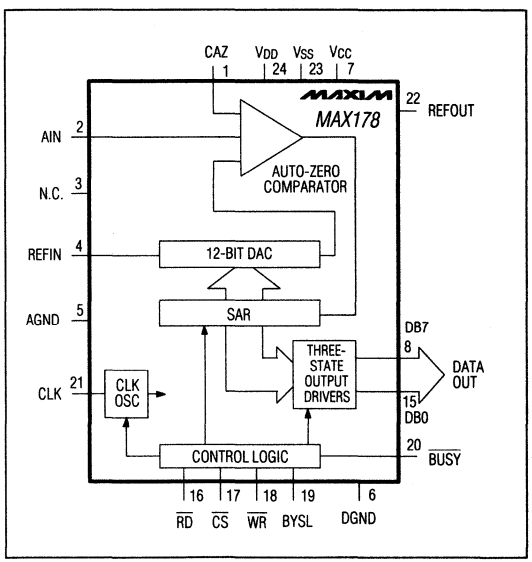
PART	TEMP. RANGE	PIN-PACKAGE
MAX178ACNG	0°C to +70°C	24 Plastic DIP
MAX178BCNG	0°C to +70°C	24 Plastic DIP
MAX178ACWG	0°C to +70°C	24 Wide SO*
MAX178BCWG	0°C to +70°C	24 Wide SO*
MAX178AENG	-40°C to +85°C	24 Plastic DIP
MAX178BENG	-40°C to +85°C	24 Plastic DIP
MAX178AEWG	-40°C to +85°C	24 Wide SO*
MAX178BEWG	-40°C to +85°C	24 Wide SO*
MAX178AMRG	-55°C to +125°C	24 CERDIP
MAX178BMRG	-55°C to +125°C	24 CERDIP

** Consult factory.*

Pin Configuration



Functional Diagram



Calibrated 12-Bit ADC with T/H and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... +0.3V, -7V
AGND to DGND ..... -0.3V, REFIN +0.3V
V_{CC} to DGND ..... -0.3V, +7V
REFIN to AGND ..... -0.3V, V_{DD} +0.3V
AIN to AGND ..... -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND ..... -0.3V, V_{DD} +0.3V

Operating Temperature Range
MAX178_C ..... 0°C to +70°C
MAX178_E ..... -40°C to +85°C
MAX178_M ..... -55°C to +125°C
Power Dissipation (any Package)
To +75°C 1,000mW
Derate above +75°C by 10mW/C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Total Unadjusted Error (Note 1)	TUE				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Full-Scale Error (Gain Error)		T_A = +25°C			±1/2	LSB
Full-Scale Error Tempco				0.5		ppm/°C
Zero Error		T_A = +25°C			±1/2	LSB
Zero Error Tempco				0.5		ppm/°C
ANALOG INPUT						
Input Voltage Range		V_{REF} = +5V	0		+5	V
On-Channel Input Capacitance	C_{AIN}			8		pF
Input Leakage Current	I_{AIN}	AIN = 0V to +5V: T_A = +25°C T_A = T_{MIN} to T_{MAX}			 10 100	nA
DYNAMIC ACCURACY ($f_{\overline{WR}}$ = 14.81kHz, f_{AIN} = 2.011kHz, T_A = 25°C, Note 2)						
Signal-to-Noise + Distortion	S/(N + D)		70			dB
Total Harmonic Distortion	THD				-80	dB
Peak Harmonic or Spurious Noise					-80	dB
REFERENCE INPUT						
REFIN Range	V_{REFIN}	For specified performance		+5 ±5%		V
		Degraded transfer accuracy	+4		+6	
REFIN Input Current		REFIN = +5V			1.0	mA
REFERENCE OUTPUT						
MAX178A						
REFOUT Voltage		T_A = +25°C	+4.985	+5	+5.015	V
REFOUT Temp (C°)				±10	±40	ppm/°C
REFOUT Sink Current					1	mA
MAX178B						
Use External Reference Only						

ELECTRICAL CHARACTERISTIC (continued)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, $\overline{WR}$, BYSL						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+2.4			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input Current	I_{IN}	V_{IN} = 0 to V_{CC}: T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance	C_{IN}	(Note 3)			10	pF
CLOCK						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+3.0			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input High Current	I_{IH}	V_{CC} = +5V ±5%			1.5	mA
Input Low Current	I_{IL}	V_{CC} = +5V ±5%			1.2	mA
LOGIC OUTPUTS						
DB0-DB7, $\overline{BUSY}$						
Output High Voltage	V_{OH}	V_{CC} = +5V ±5%, I_{SOURCE} = 200µA	+4.0			V
Output Low Voltage	V_{OL}	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA			+0.4	V
Floating State Leakage Current (DB0-DB7)	I_{LKG}	V_{OUT} = 0V to V_{CC}			±1	µA
Floating State Output Capacitance (DB0-DB7)	C_{OUT}	(Note 3)			15	pF
CONVERSION TIME (Note 4)						
With External Clock		f_{CLK} = 266.67kHz	60			µs
With Internal Clock		T_A = +25°C	90		140	µs
POWER REQUIREMENTS (Note 5)						
Power-Supply Voltage	V_{DD}		+11.4		+15.75	V
	V_{SS}		-4.75		-5.25	
	V_{CC}		+4.75		+5.25	
V_{DD} Supply Rejection		V_{DD} = +14.25V to +15.75V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		VSS = -4.75V to -5.25V, V_{DD} = +15V		±1/8		LSB
V_{DD} Supply Rejection		V_{DD} = +11.4V to +12.6V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		V_{SS} = -4.75V to -5.25V, V_{DD} = +12V		±1/8		LSB
Power-Supply Current	I_{DD}	V_{IN} = V_{IL} or V_{IH}		6	10	mA
	I_{SS}				8	
	I_{CC}			0.1	1.0	

Note 1: Includes: Full-Scale Error, Offset Error, Relative Accuracy.
Note 2: Up to 5th Harmonic is measured.
Note 3: Guaranteed by design.
Note 4: Track/Hold aquisition time included in conversion time, using t_{13} condition (see Timing Characteristics).
Note 5: Power-supply current is measured when MAX178 is inactive ($\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = $\overline{BUSY}$ = High).

Calibrated 12-Bit ADC with T/H and Reference

TIMING CHARACTERISTICS (Note 6, Figures 1 and 2)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C to +85°C			T_A = -55°C to +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0			0			0			ns
$\overline{WR}$ Pulse Width	t_2		120			120			120			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3		0			0			0			ns
$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	t_4			85	120		100	140		115	160	ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_5	(Note 3)	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_6		0			0			0			ns
$\overline{RD}$ Pulse Width	t_7		120			120			120			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_8		0			0			0			ns
BYSL to $\overline{RD}$ Setup Time	t_9		50			50			50			ns
BYSL to $\overline{RD}$ Hold Time	t_{10}		0			0			0			ns
$\overline{RD}$ to Valid Data (Note 7)	t_{11}	(Bus Access Time)		60	100		70	110		90	130	ns
$\overline{RD}$ to Three-State Output (Note 8)	t_{12}	(Bus Relinquish Time)	20		100	20		100	20		100	ns
$\overline{WR}$ to CLK for 16 Clock Conversions (Note 9)	t_{13}		20			20			20			ns
$\overline{WR}$ to CLK for 17 Clock Conversions (Note 9)	t_{14}		20			20			20			ns

Note 6: Data is timed from V_{OH}, V_{OL}; all input control signals are timed from a voltage level of +1.6V and specified with t_r = t_f = 20ns (10% to 90% of +5V).
Note 7: t_{11}, the time required for an output to cross 0.8V or 2.4V, is measured with the load circuits of Figure 3.
Note 8: t_{12}, the time required for the data lines to change 0.5V, is measured with the load circuits of Figure 4.
Note 9: See Figure 7.

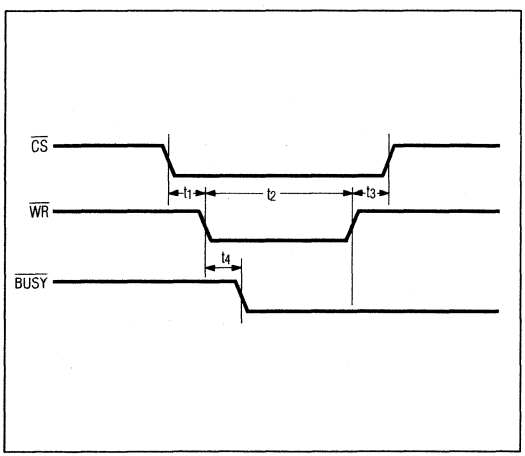


Figure 1: Start Cycle Timing

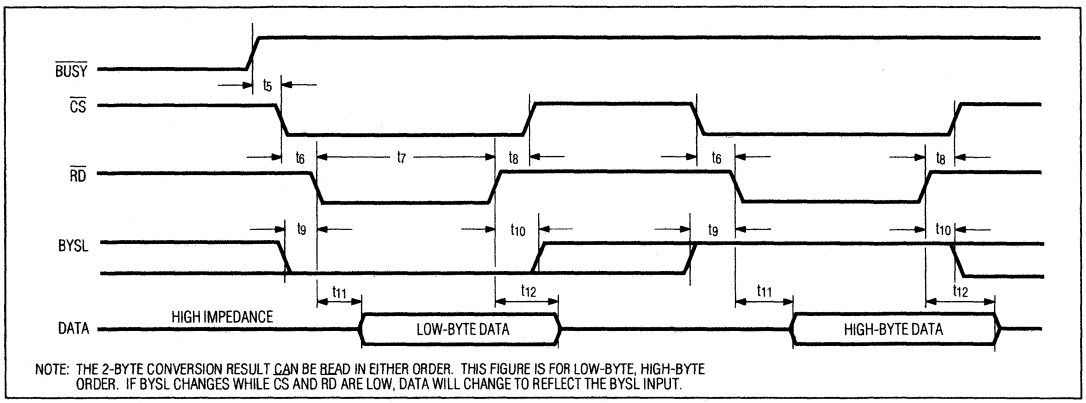


Figure 2. Read Cycle Timing

Pin Description

PIN	NAME	FUNCTION
1	CAZ	Auto-Zero Capacitor Input. Connect other end of capacitor to AGND.
2	AIN	Analog Input
3	N.C.	No Connect
4	REFIN	Voltage Reference Input. The MAX178 is specified with REFIN = +5V.
5	AGND	Analog Ground
6	DGND	Digital Ground
7	VCC	Logic Supply. Digital inputs and outputs are TTL compatible for VCC = +5V.
8-15	DB0-DB7	Three-State Data Outputs. Active when $\overline{CS}$ and $\overline{RD}$ are brought low. Individual pin functions depend upon BYTE SELECT (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$, $\overline{RD}$ = LOW		
PIN	BYSL = HIGH	BYSL = LOW
8	BUSY (Note 10)	DB7
9	LOW (Note 11)	DB6
10	LOW (Note 11)	DB5
11	LOW (Note 11)	DB4
12	DB11 (MSB)	DB3
13	DB10	DB2
14	DB9	DB1
15	DB8	DB0 (LSB)

PIN	NAME	FUNCTION
16	$\overline{RD}$	$\overline{READ}$ Input. Used with $\overline{CS}$ to enable the three-state data outputs. $\overline{RD}$ is active low.
17	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input. Used with either $\overline{RD}$ or $\overline{WR}$ for control. $\overline{CS}$ is active low.
18	$\overline{WR}$	$\overline{WRITE}$ Input. In combination with $\overline{CS}$, this active low signal starts a new conversion.
19	BYSL	BYTE SELECT. BYSL selects high- or low-byte output during a data READ operation. ($\overline{RD}$, $\overline{CS}$ = low). See pins 8-15.
20	$\overline{BUSY}$	Converter Status. $\overline{BUSY}$ is only low during conversion.
21	CLK	CLOCK Input. Internal clock operation, with this pin floating and unloaded, typically results in 120µs conversion time (Figure 8). This can be lowered by using an external 74HC clock source (Figure 9).
22	REFOUT	Reference Output
23	VSS	Negative Supply Voltage, -5V
24	VDD	Positive Supply Voltage, +15V

Note 10: High during a conversion, BUSY is a converter status flag.

Note 11: When BYSL is high, pins 9-11output a logic low. The 12-bit digital result is in DB0-DB11. DB11 is the MSB.

Calibrated 12-Bit ADC with T/H and Reference

Detailed Operation

Operating Information

Figure 5 shows an operational diagram for the MAX178. The only required passive components are a hold capacitor (CAZ) and a reference bypass capacitor and resistor. Individual pin functions are listed in the Pin Description table.

On-Chip Clock Operation

The on-chip oscillator requires no external components. Therefore, the CLK pin can be left unconnected resulting in a typical 120µs conversion time. The conversion time can be increased by adding a capacitive load on the CLK pin. The timing diagrams in Figures 6 and 7 show the resulting tracking duration for relative positions of $\overline{WR}$ and CLK. Figure 8 is a schematic for on-chip clock operation.

A new conversion is initiated by bringing $\overline{WR}$ low, with $\overline{CS}$ low. This starts a track acquisition sequence. In this state, the T/H goes into track mode. Capacitor CAZ charges to the analog input voltage minus the input offset voltage of the comparator. Note: when $\overline{WR}$ is low (with $\overline{CS}$ low), the MAX182 is in track mode. When $\overline{WR}$ goes high, tracking time is extended by another 4 to 5 clock periods (4 clock periods beginning with the first falling clock edge following the rising edge of $\overline{WR}$). 16 to 17 clock periods are required for each conversion (Figure 7).

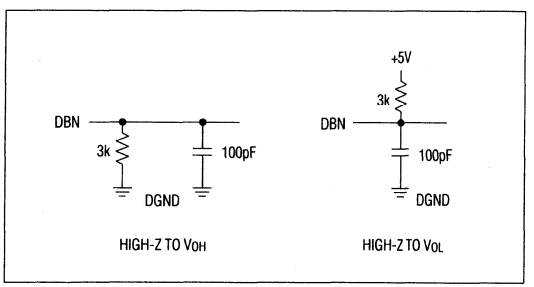


Figure 3. Load Circuits for Access Time Test (t_{11})

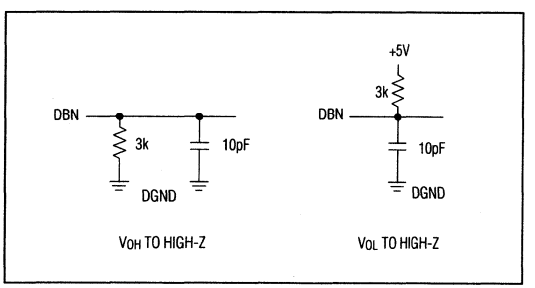


Figure 4. Load Circuits for Output Three-State Delay Test (t_{12})

The MAX178 is in track mode between conversions when $\overline{BUSY}$ is high. After the tracking sequence, the most significant bit (MSB) decision is made. Following this, the remaining 11 bits are digitized on successive clock cycles, as indicated in Figure 6. The $\overline{WR}$ pulse need not be synchronized with the internal clock.

External Clock Operation

For external clock operation, drive the CLK input with a 74HC compatible clock source (Figure 9).

The MAX178 automatically tracks for the appropriate time by means of an on-chip counter. Both $\overline{WR}$ and $\overline{CS}$ must be low to initiate a new conversion. Whenever $\overline{WR}$ and $\overline{CS}$ are low, the chip enters into track mode until $\overline{WR}$ or $\overline{CS}$ rises. After the rising edge of $\overline{WR}$, the next falling edge of the clock starts a counter, which extends the tracking time by 4 to 5 external clock periods.

The analog input acquisition is complete at the end of the tracking period, and the signal is stored in the internal track-and-hold. The external clock source need not be synchronized with the $\overline{WR}$ pulse.

Reading Data

The 12-bit result of a conversion plus the converter status flag are accessible over an 8-bit data bus. The data is available from the MAX178 in right-justified format (the least significant bit (LSB) is the right-most bit in a 16-bit word). Two byte sized read operations are needed. The Byte Select (BYSL) input determines which byte is to be read first, 8LSBs or 4MSBs plus status flag.

It is necessary to wait for the end of a conversion to obtain valid 12-bit data from the MAX178's successive approx-

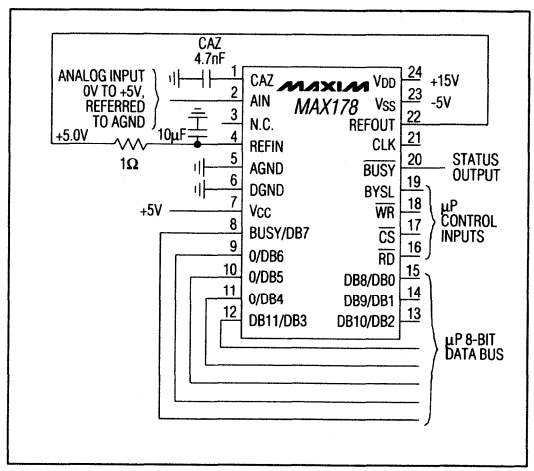


Figure 5. MAX178 Operational Diagram

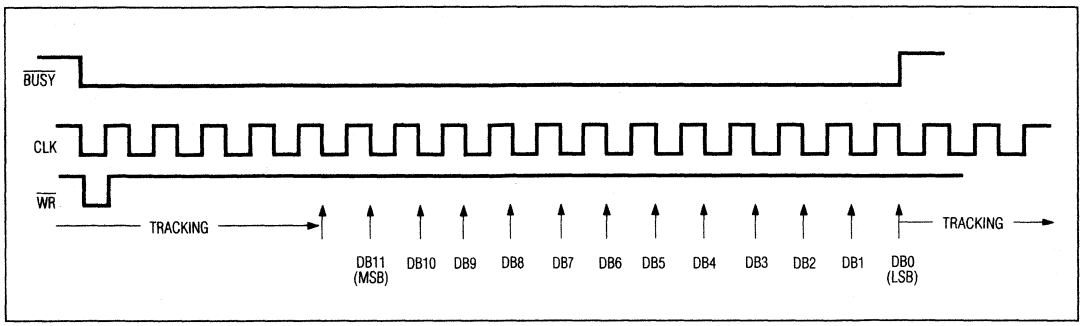


Figure 6. MAX178 Timing Diagram

imation register (SAR). If a read operation instruction is performed during a conversion, the MAX178 will dump the existing contents of the SAR onto the data bus. There are three methods to ensure correct operation:

1. Insert a software delay longer than the ADC conversion time between the conversion start and the data read operations.
2. The $\overline{BUSY}$ output is low during the conversion and high at the conversion end. Use this signal as an interrupt to the µP.
3. Poll the converter status flag, BUSY, at user-defined intervals after a conversion start. The status flag is available on DB7 during a high-byte $\overline{READ}$. The flag is the left-most bit and can be shifted directly into the µP's carry flag for testing. BUSY is high during a conversion.

A write operation to the MAX178 during a conversion restarts the conversion.

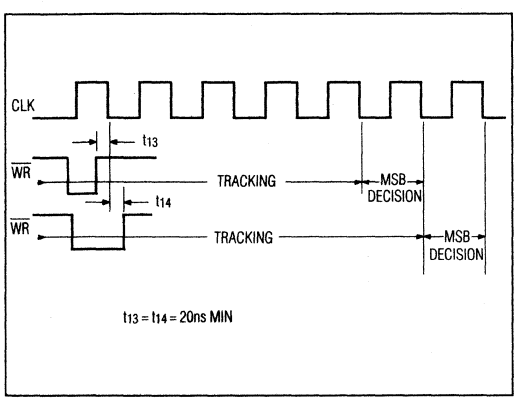


Figure 7. Width of Tracking Interval as a Function of $\overline{WR}$ Rising Edge Timing with Respect to CLK Falling Edge

Application Hints

Auto-Zero Capacitor (CAZ)

CAZ (Figure 5) must be a low-leakage, low-dielectric absorption capacitor such as polypropylene, polystyrene, or teflon. Connect the outside foil of CAZ to AGND to minimize noise. CAZ should be 4,700pF.

Clock

Figure 10 shows typical conversion time versus temperature when using the MAX178's on-chip clock. Due to variations in manufacturing, the actual operating frequency can differ from chip-to-chip by up to 20%. For this reason, it is suggested that an external clock be used when fixed conversion times are required.

Analog Inputs

The high-impedance analog input, AIN, allows simple analog interfacing. Signal sources from 0V to +5V may be connected directly to AIN without extra buffering for source impedances up to 5kΩ (Figure 11). The input/output (I/O) transfer characteristic and transition points for this input signal range are demonstrated in Figure 12 and Table 1. The MAX178 transfer characteristic has transi-

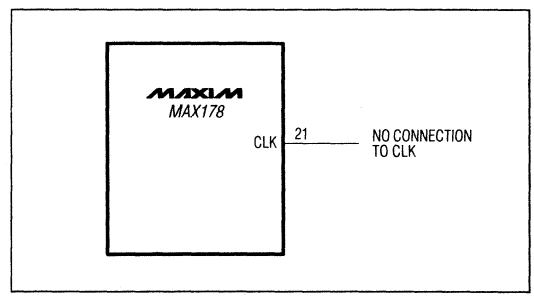


Figure 8. Internal Clock Operation

Calibrated 12-Bit ADC with T/H and Reference

tion points designed to occur on integer multiples of 1LSB. The output code is natural binary with:

1LSB = (Full Scale (FS))/4096
= (5/4096)V = 1.22mV.

For signal ranges other than 0V to +5V, use resistor divider networks to provide 0V to +5V signal ranges at the MAX178 input pins. The connection in Figure 13 shows a divider network for a 0V to +10V signal range. Resistors should be of the same type and manufacturer to ensure matched temperature coefficients. The source impedance must now be as low as possible since it adds to the resistor divider impedance.

Figure 14 shows how bipolar signals -5V to +5V are accommodated by referencing the resistor divider network to REFIN. The signal source must be capable of sinking 0.5mA with the resistor values shown. Refer to Figure 15 and Table 2 for the I/O transfer characteristic and transition points for this signal range. Output coding is offset binary with an LSB size of:

(FS)(1/4096) = (10/4096)V = 2.44mV.

To adjust bipolar zero error, apply 1.22mV (+1/2LSB) to AIN and adjust the offset of A1 so that the ADC output switches between 1000 0000 0000 and 1000 0000 0001.

Power-Supply Decoupling

Power supplies to the MAX178 should be bypassed with either a 10µF electrolytic or tantulum capacitor in parallel with a 0.01µF disc ceramic capacitor for clean, high-frequency performance. Place all capacitors as close as possible to the MAX178 supply pins.

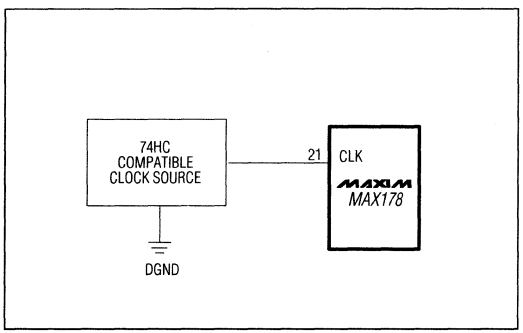


Figure 9. External Clock Operation

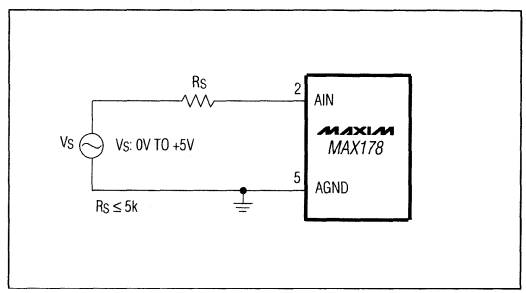


Figure 11. Unipolar 0V to +5V Operation

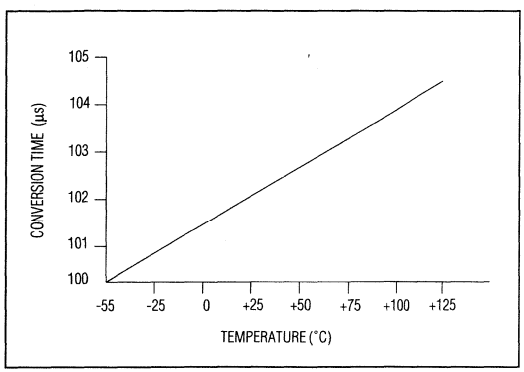


Figure 10. Typical Change in Conversion Time Variation vs. Temperature when Using Internal Clock

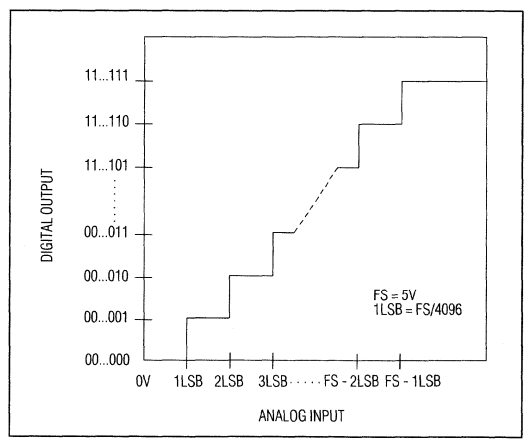


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Internal Reference

The internal reference (REFOUT) should be bypassed with a 1Ω resistor in series with a capacitor. The capacitor should be a 10µF electrolytic or tantalum in parallel with a 0.01µF disc ceramic (Figure 16). Figure 17 shows a circuit that allows input adjustment which is useful for trimming out initial (room temperature) error in the reference voltage.

Table 1. Transition Points for Unipolar 0V to +5V Operation

Analog Input (V)	Digital Output
0.00122	0000 0000 0001
0.00244	0000 0000 0010
. . .	. . .
2.49878	0111 1111 1111
2.50000	1000 0000 0000
2.50122	1000 0000 0001
. . .	. . .
4.99756	1111 1111 1110
4.99878	1111 1111 1111

Table 2. Transition Points for Bipolar -5V to +5V Operation

Analog Input (V)	Digital Output
-4.99878	0000 0000 0001
-4.99634	0000 0000 0010
. . .	. . .
-0.00122	1000 0000 0000
+0.00122	1000 0000 0001
. . .	. . .
+4.99389	1111 1111 1110
+4.99634	1111 1111 1111

External Reference Circuit

Figure 18 shows how to set up a MX584LH to generate a reference voltage of 5.00V. A typical adjustment range of 75mV is provided by R2. Over the commercial temperature range, the MX584LH contributes no more than ±1LSB of gain error.

During a conversion, transient currents flow at the REFIN input. To prevent dynamic errors, place either a 10µF electrolytic or tantalum smoothing capacitor in parallel with a 0.01µF disc ceramic from the REFIN pin to AGND.

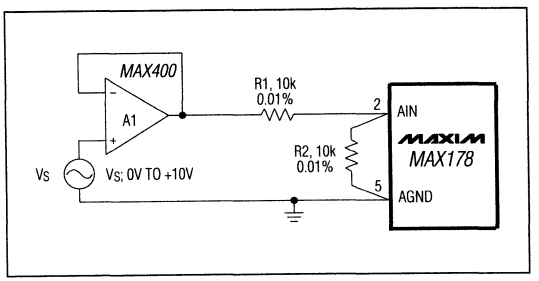


Figure 13. Unipolar 0V to +10V Operation

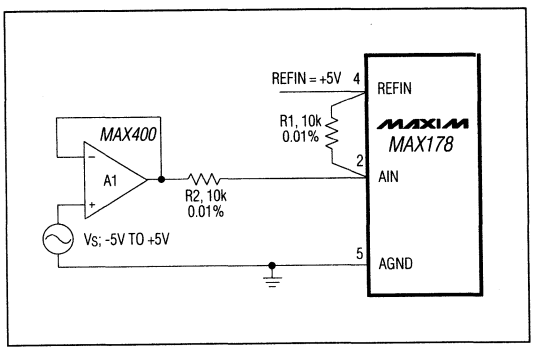


Figure 14. Bipolar -5V to +5V Operation

Calibrated 12-Bit ADC with T/H and Reference

Layout

When designing layout for a printed circuit board, keep digital and analog signal lines separated whenever possible. It is critical that no digital line runs alongside an analog signal line or near the CAZ. Guard the analog inputs, the reference input and the CAZ input with AGND.

Establish a single-point analog ground (AGND) as close to the MAX178 as possible, isolated from the logic system. Connect the single-point analog ground to the digital system ground, which is attached to DGND at one point, as close as possible to the MAX178. The following should be returned to the analog ground point: input-signal common, input guards, the CAZ, and any bypass capacitors for the reference input and the analog supplies. Low-impedance analog and digital power-supply common returns, with wide trace widths, are essential for quiet operation of the MAX178.

Noise

To minimize input noise coupling, input signal leads to AIN and signal return leads from AGND should be kept as short as possible. A shielded cable between source and ADC is suggested in applications where longer leads are required. Also, care should be taken to reduce ground circuit impedances as much as possible since any potential difference in grounds between the signal source and ADC creates an error voltage in series with the input signal.

When interfacing to continuously busy and noisy µP buses, it is possible to get errors at the LSB level. These errors exist because of feedthrough from the bus to the integrated circuit through the package. The problem can be minimized in ceramic packaged chips by grounding the metal lid. Another solution is to isolate the MAX178 from the noisy µP bus using three-state buffers.

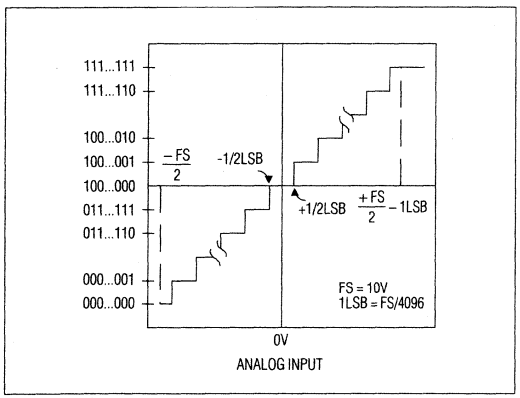


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

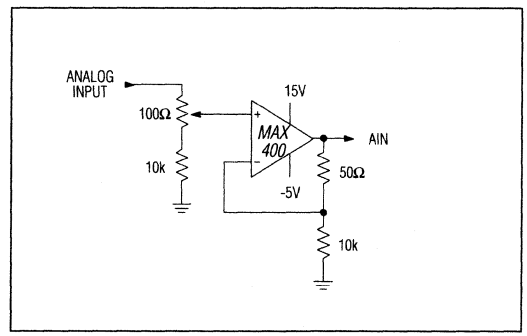


Figure 17. Adjusting Analog Input Gain to Trim Out Initial Reference Voltage Error

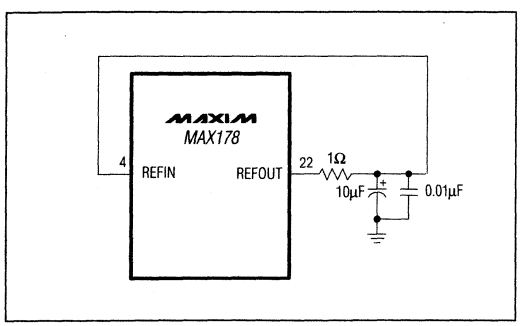


Figure 16. Internal Reference Hookup. Note: Reference Value Is Not Adjustable.

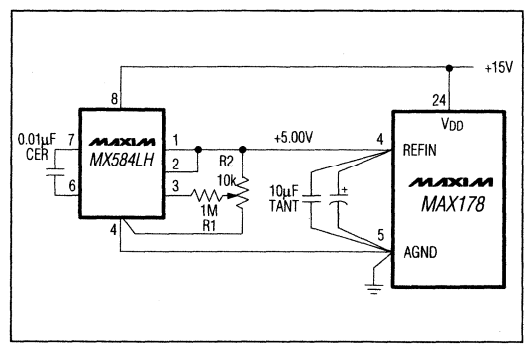
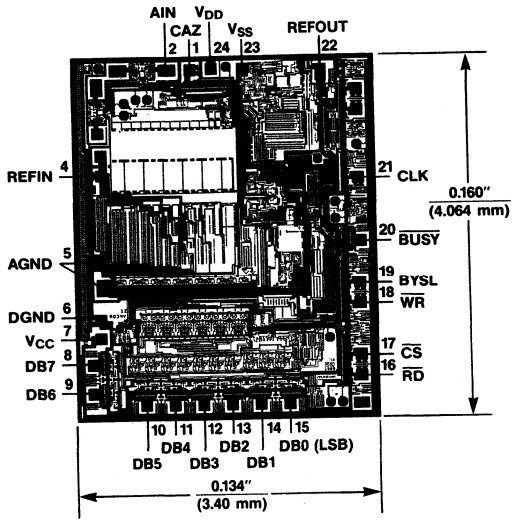


Figure 18. MX584LH as Reference Generator

Calibrated 12-Bit ADC with T/H and Reference

Chip Topography



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19-3950; Rev 0; 6/91

MAXIM

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

General Description

The MAX180/MAX181 are complete 12-bit Data Acquisition System (DAS) which combine 8/6-channel input multiplexer, high bandwidth Track-and-Hold (T/H), low-drift zener reference, and flexible microprocessor (µP) interface with high conversion speed and low power consumption. The MAX180/MAX181 can be configured by a µP for unipolar or bipolar conversions and single-ended or differential inputs. Both devices sample and digitize at 100kHz throughput rate and feature a fast 8- or 16-bit µP interface.

The MAX180 has 8 analog input channels, while the MAX181 has 6. The multiplexer output of the MAX180 is fed directly into the Analog-to-Digital Converter (ADC) input. The MAX181 brings out both the multiplexer output and ADC input to separate pins, allowing a programmable gain amplifier to be inserted between the MUX and the ADC.

The systems allow the user to choose between an internal or an external reference. Futhermore, the internal reference value and the offset can be adjusted, allowing the overall system gain and offset errors to be nulled. The multiplexer has high impedance inputs, simplifying analog drive requirements.

Applications

High-Speed Servo Loops

Digital-Signal Processing

High-Accuracy Process Control

Automatic Testing Systems

Features

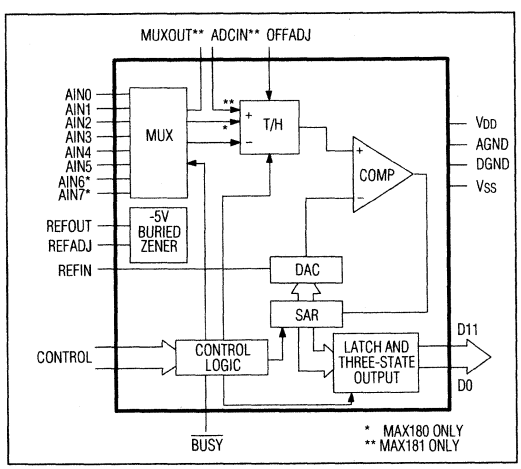
- **12-Bit Resolution, ±1/2LSB Linearity**
- **8-Channel Multiplexed Inputs (MAX180)**
- **Single-Ended 1-of-6 Multiplexer (MAX181)**
- **Built-In Track-and-Hold**
- **100kHz Sampling Rate**
- **DC and Dynamically Tested**
- **Internal 25ppm/°C Voltage Reference**
- **Each Channel Configurable for Unipolar (0V to +5V) or Bipolar (-2.5V to +2.5V) Input Range**
- **Each Channel Configurable for Single-Ended or Differential Inputs**
- **Fast 8-/16-Bit µP Interface**
- **+5V and -12V to -15V Supply Operation**
- **110mW Power Consumption**

Ordering Information

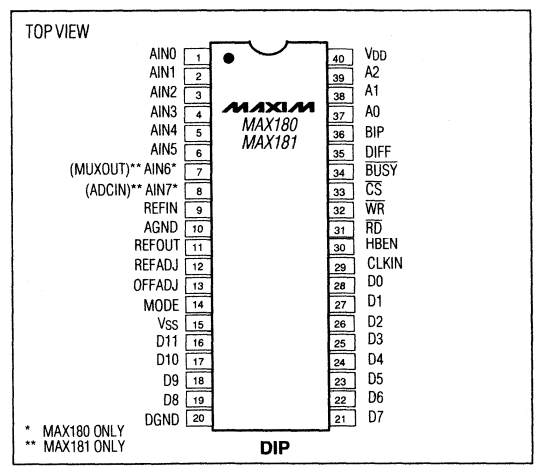
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX180ACPL	0°C to +70°C	40 Plastic DIP	±1/2
MAX180BCPL	0°C to +70°C	40 Plastic DIP	±1
MAX180CCPL	0°C to +70°C	40 Plastic DIP	±1
MAX180ACQH	0°C to +70°C	44 PLCC	±1/2
MAX180BCQH	0°C to +70°C	44 PLCC	±1

Ordering information continued on last page.

Block Diagram



Pin Configurations



Complete, 8-Channel, 12-Bit Data-Acquisition Systems

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +7V
V_{SS} to DGND ..... -0.3V, -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN _, MUXOUT, ADCIN, REFADJ, OFFADJ to REFIN ..... -0.3V, V_{DD} + 0.3V
REFIN to DGND ..... +0.3V, V_{SS} - 0.3V
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLK, A2-A0, BIP, DIFF, HBEN to DGND ..... -0.3V, V_{DD} + 0.3V
$\overline{BUSY}$, D0-D11 to DGND ..... -0.3V, V_{DD} + 0.3V

Continuous Power Dissipation (any package)
to +70°C 1000mW
derates above +70°C by ..... 10mW/°C
Operating Temperature Ranges:
MAX18 _C _ _ ..... 0°C to +70°C
MAX18 _E _ _ ..... -40°C to +85°C
MAX18 _MJL ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 2)						
Resolution	N		12			Bits
Integral Nonlinearity Error	INL	MAX18_A			±1/2	LSB
		MAX18_B/C			±1	
Differential Nonlinearity Error	DNL	Guaranteed monotonic over temperature			±1	LSB
Unipolar Offset Error (Note 3)				±1	±4	LSB
Bipolar Offset Error (Note 3)				±1	±6	LSB
Unipolar Gain Error				±2	±10	LSB
Bipolar Gain Errror				±2	±15	LSB
Gain-Error Tempco (Note 4)				±5		ppm/°C
Channel-to-Channel Matching				±1/4		LSB
DYNAMIC PERFORMANCE (Note 2)						
Signal-to-Noise + Distortion Ratio	SINAD	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C	70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C			-80	dB
Spurious-Free Dynamic Range	SFDR	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C	80			dB
Full-Power Sampling Bandwidth		In track mode, under-sampled waveform		6		MHz
Track-and-Hold Acquisition Time (Note 5)	t_{ACQ}		1.875			µs
Conversion Time	t_{CONV}	Asynchronous hold mode; Note 5	7.500		8.125	µs
		ROM, Slow-Memory, and I/O Port Modes; 15-16 clock cycles	9.375		10.000	
ANALOG INPUT						
Voltage Range		AIN_, MUXOUT, and ADCIN	REFIN		V_{DD}	V
Unipolar, Single-Ended Range		AIN_ to AGND	0		5.0	
Unipolar, Differential Range		AIN_+ to AIN_-	0		5.0	
Bipolar, Single-Ended Range		AIN_ to AGND	-2.5		2.5	
Bipolar, Differential Range		AIN_+ to AIN_-	-2.5		2.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT (continued)							
Input Current		AIN_ ,	MAX180			±1.0	µA
		ADCIN,	MAX181			±0.1	
Mux-On Resistance	R_{ON}	AIN_ = 2.5V, I_{MUXOUT} = 1.25mA, MAX181				2	kΩ
Mux-On Leakage Current	I_{ON}	AIN_ = MUXOUT = ±5V, MAX181				±100	nA
Mux-Off Leakage Current	$I_{IN (OFF)}$	AIN_ = ±5V, V_{OUT} = ±5V, MAX181				±100	nA
	$I_{OUT (OFF)}$	AIN_ = ±5V, V_{OUT} = ±5V, MAX181				±100	
Input Capacitance (Note 5)	C_{IN}	AIN_ , ADCIN			25	35	pF
		MUXOUT			35	45	
REFERENCE INPUT							
Input Range (Note 5)				-4.92	-5.00	-5.08	V
Input Current						-2	mA
Input Resistance				2.5			kΩ
REFERENCE OUTPUT							
VREF Output Voltage		T_A = +25°C		-4.98	-5.00	-5.02	V
VREF Output Tempco (Note 6)		MAX18_A/B				25	ppm/°C
		MAX18_C				45	
VREF Load Regulation (Note 7)		I_{OUT} = 0mA to 5mA, T_A = +25°C			0.2	1.0	mV/mA
REFADJ, OFFADJ							
Input Current		V_{REFADJ}, V_{OFFADJ} = V_{DD} to REFIN				±1	µA
Disable Threshold				4.5			V
REFADJ Adjustment Range		REFIN < REFADJ <AGND		±60	±80		mV
OFFADJ Adjustment Range		REFIN < OFFADJ <AGND		±15	±25		LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}	MODE				0.5	V
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN				0.8	
Input High Voltage	V_{IH}	MODE		4.5			V
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN		2.4			
Input Mid-Level Voltage	V_{MID}	MODE		1.5		3.5	V
Input Floating Voltage	V_{FLT}	MODE			2.5		V
Input Current	I_{IN}	MODE	T_A = +25°C		±50	±100	µA
			T_A = T_{MIN} to T_{MAX}		±50	±100	
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN	T_A = +25°C			±1	
			T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 5)	C_{IN}					15	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0, $\overline{BUSY}$, RDY, I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0, $\overline{BUSY}$, RDY, I_{SOURCE} = 360µA		4.0			V
Floating State Leakage Current	I_{LKG}	D11-D0, V_{OUT} = 0V to V_{DD}				±10	µA
Floating State Output Capacitance (Note 5)	C_{OUT}					15	pF

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage (Note 1)	V_{DD}		4.75	5.00	5.25	V
	V_{SS}		-11.40		-15.75	
Supply Current	I_{DD}	V_{DD} = 5V		4.5	7.0	mA
	I_{SS}	V_{SS} = -12V		7.0	10.0	
Power Dissipation	PD	V_{DD} = 5V, VSS = -15V		110	155	mW
Power-Supply Rejection, with Internal Reference	PSR	Input near FS, V_{SS} = -12V, V_{DD} = 4.75V to 5.25V		±1/2	±1	LSB
		Input near FS, V_{DD} = 5V, V_{SS} = -14.25V to -15.75V		±1/8	±1/2	
		Input near FS, V_{DD} = 5V, V_{SS} = -11.4V to = -12.6V		±1/8	±1/2	

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -12V, f_{CLK} = 1.6MHz, Internal Reference Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			MAX18_C/E			MAX18_M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup time	t_1		Note 5	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold time	t_2			0			0			0			ns
$\overline{CS}$ to $\overline{WR}$ Setup time	t_3			0			0			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold time	t_4		Note 5	0			0			0			ns
$\overline{WR}$ Low Pulse Width	t_5			120			120			120			ns
$\overline{WR}$ High Pulse Width	t_6	MODE = 0 or 1	Note 5	200			200			200			ns
DATA IN to $\overline{WR}$ Setup Time	t_7			80			100			120			ns
DATA IN to $\overline{WR}$ Hold Time	t_8			0			0			0			ns
$\overline{WR}$ Rising to $\overline{BUSY}$ Delay	t_9	C_L = 50pF, MODE = 1				160			180			200	ns
$\overline{WR}$ Falling to $\overline{BUSY}$ Delay	t_{10}	C_L = 50pF, MODE = open				220			260			280	ns
$\overline{RD}$ Low Pulse Width	t_{11}			100			130			150			ns
$\overline{RD}$ High Pulse Width	t_{12}		Note 5	200			200			200			ns
DATA IN to $\overline{RD}$ Setup Time	t_{13}			80			100			120			ns
DATA IN to $\overline{RD}$ Hold Time	t_{14}			0			0			0			ns
$\overline{RD}$ to $\overline{BUSY}$ Fall Delay	t_{15}	C_L = 50pF				150			170			200	ns
$\overline{RD}$ to Data out Valid	t_{16}	C_L = 100pF	Note 9		50	100			130			150	ns
$\overline{RD}$ to Data out Three-State	t_{17}		Notes 9, 10		30	50			65			75	ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Setup Time	t_{18}			80			100			120			ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Hold Time	t_{19}			0			0			0			ns
$\overline{CS}$ to $\overline{READY}$ Fall Delay	t_{20}	C_L = 50pF				110			130			150	ns

TIMING CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = -12V, f_{CLK} = 1.6MHz, Internal Reference Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C MIN	TYP	MAX	MAX18_C/E MIN	TYP	MAX	MAX18_M MIN	TYP	MAX	UNITS
$\overline{BUSY}$ to Data Out Valid	t_{21}	C_L = 100pF	Note 9			125			150			170	ns
$\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to CLK Setup time for 15 clock conversion	t_{22}		Note 5	220			220			220			ns
$\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to CLK Setup time for 16 clock conversion	t_{23}		Note 5	0			0			0			ns

Note 1: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5V, REFIN = -5V.
Note 3: Typical change over temperature is ±1LSB.
Note 4: FS Tempco = ΔFS/ΔT, where ΔFS is full-scale change from T_A = +25°C to T_{MIN} or to T_{MAX}.
Note 5: Guaranteed by design.
Note 6: REFIN TC = ΔREFIN/ΔT, where ΔREFIN is reference voltage change from T_A = +25°C to T_{MIN} or to T_{MAX}
Note 7: Load current should remain constant during conversion. This current is in addition to the DAC input current.
Note 8: All inputs are 0V to +5V swing with t_r = t_f = 5ns (10% to 90% of 5V) and timed from a voltage level of +1.6V.
Note 9: t_{16} and t_{21} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 10: t_{17} is defined as the time required for the data lines to change 0.5V when the circuit load is as shown in Figure 2.

Pin Description

NAME	MAX180 DIP	MAX180 PLCC	MAX181 DIP	MAX181 PLCC	FUNCTION
AIN0-AIN5	1-6	2-7	1-6	2-7	Analog Inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
AIN6-AIN7	7,8	8,9			Analog Inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
MUXOUT			7	8	Muliplexer Output
ADCIN			8	9	Analog Input to track-and-hold
REFIN	9	10	9	10	Reference Input
AGND	10	11	10	11	Analog Ground
REFOUT	11	13	11	13	-5V Reference Output
REFADJ	12	14	12	14	-5V Reference Adjust. Connect to V_{DD} if not required.
OFFADJ	13	15	13	15	Offset Adjust. Connect to V_{DD} if not required.
MODE	14	16	14	16	Interface Mode Select pin.
V_{SS}	15	17	15	17	Negative Supply: -15V or -12V
D11-D8	16-19	18-21	16-19	18-21	Three-State Data Outputs, MSB = D11
DGND	20	22	20	22	Digital Ground
D7-D0	21-28	24-31	21-28	24-31	Three-State Data Outputs, LSB = D0
CLKIN	29	32	29	32	Clock Input, TTL/CMOS compatible
HBEN	30	33	30	33	High-Byte Enable Input
$\overline{RD}$	31	35	31	35	$\overline{READ}$ Input
$\overline{WR}$	32	36	32	36	$\overline{WRITE}$ Input (MODE = 1 or Open) $\overline{READY}$ Output (MODE = 0)
$\overline{CS}$	33	37	33	37	$\overline{CHIP\text{-}SELECT}$ Input
$\overline{BUSY}$	34	38	34	38	$\overline{BUSY}$ Output
DIFF	35	39	35	39	Single-Ended Mode: DIFF = 0, Differential Mode: DIFF = 1
BIP	36	40	36	40	Unipolar Mode: BIP = 0, Bipolar Mode: BIP = 1
A0-A2	37-39	41-43	37-39	41-43	Multiplexer Channel Address Input: A2 = MSB, A0 = LSB
V_{DD}	40	44	40	44	Positive Supply: +5V Input (substrate connected to V_{DD})
N.C.		1,12, 23,34		1,12, 23,34	No Connect. No internal connection. Leave pin open or connect to AGND.

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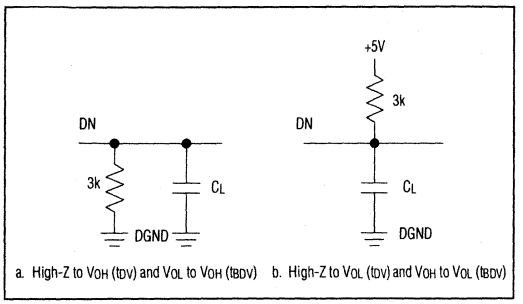

Figure 1. Load Circuits for Access Time

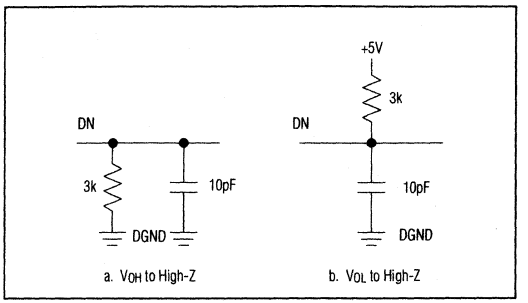

Figure 2. Load Circuits for Bus-Relinquish Time

A/D Converter Operation

The MAX180/MAX181 use successive approximation and input track-and-hold (T/H) circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic interfaces easily to uPs, requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 3 shows the MAX180 typical operating circuit.

Starting a Conversion

Regardless of the mode or interface selected, the following sequence occurs once conversion is started:

1. The data inputs that configure the data-acquisition system (DAS) latch, and the interface signals the µP that a conversion has started.
2. The mux directs the selected input signal to the T/H input.
3. A fixed time delay allows the T/H to acquire the signal. In all modes except asynchronous hold, this delay is 3 clock cycles. In asynchronous hold, the µP controls this delay.
4. The T/H switches to hold mode. The T/H output delivers a stable, single-ended sample of the input signal to the A/D input.
5. The successive approximation cycle begins. The ADC tests and sets each of the 12 bits in turn, from most to least significant. Bit decisions occur on the CLKIN falling edges, for a total of 12 clock cycles.
6. Output data is latched by the output registers, and the interface signals the µP that conversion is complete and data is available.

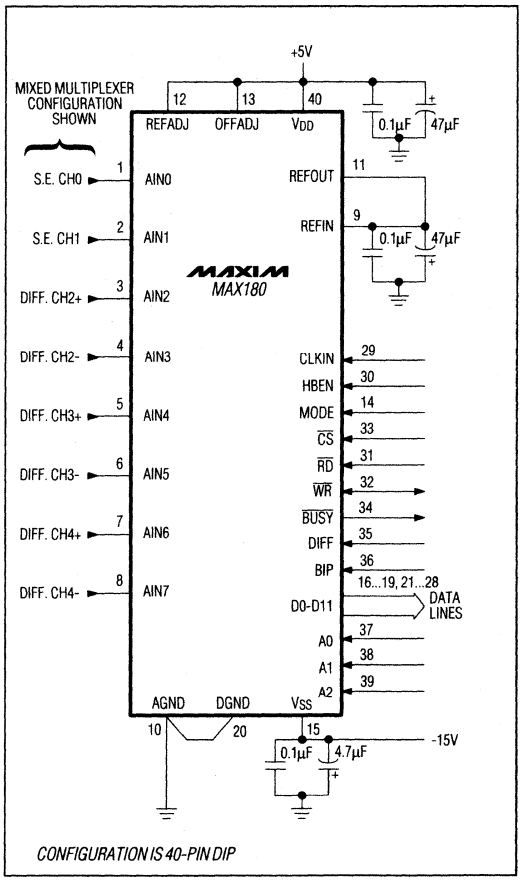

Figure 3. MAX180 Typical Operating Circuit

Analog Input - Track-and-Hold

Figure 4 shows the equivalent input circuit, illustrating the sampling architecture of the ADC's analog comparator. The input capacitance acts as the hold capacitor and is charged by the input signal with every A/D conversion. The capacitance is charged through an internal 1kΩ resistor in series with the input. Note: Figure 4's switches represents both the mux and hold switches.

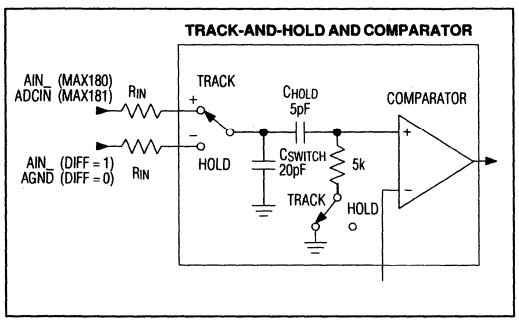

Figure 4. Equivalent Input Circuit

When in single-ended input mode and between conversions ($\overline{BUSY}$ = High), the selected analog input is connected to the hold capacitor (track mode). When a conversion starts, C_{HOLD} disconnects from the + T/H input, thus sampling the input (see "Digital Interface" section for percise T/H timing). When the switch closes at conversion end, C_{HOLD} reconnects to the input and charges to the input signal. The loading effect of the analog inputs on the signal is such that a high-speed input buffer is usually NOT needed because the ADC disconnects from the input during the actual conversion.

The previous explanation applies for the differential input mode if "input" is replaced by AIN+ and "analog ground" is replaced by AIN-. In the differential input mode, A0-A2 select the input channel pairs (Table 1). Only the signal side of the input channel is held by the T/H; the return side must remain stable within ±0.5LSB (±0.1LSB for best results) during the conversion. For example, a common-mode signal of 0.33Vp-p at 60Hz results in a maximum error of 0.5LSB.

The T/H starts tracking when the ADC is deselected ($\overline{BUSY}$ = High). Hold mode begins 3 clock cycles after a conversion is initiated in all but the Asynchronous Hold Mode. Variation in hold-mode delay from one conversion to the next (aperture jitter) is less than 100ps. Figures 7-11 detail the T/H and interface timing for the various interface modes.

The time required for the T/H to acquire an input signal is a function of how quickly the input capacitance is charged. If the input source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + R_{IN})20pF \text{ (but never less than } 1.875\mu s)$$

where R_{IN} = 1kΩ, and R_S = source impedance of the input signal.

Input Bandwidth

The A/D's input tracking circuitry is excellent for tracking large signals and wide bandwidths and does not exhibit the slew-rate limitations of many other ADC T/Hs. The MAX180/MAX181 T/H's full-power bandwidth is typically 6MHz; this allows the measurement of periodic signals with bandwidths exceeding the ADC's sample rate (100kHz) using under-sampling techniques. Important note: If under-sampling is used to measure high-frequency signals, take special care to avoid aliasing errors. Without adequate input filtering, high-frequency noise could be aliased into the measurement band.

Reference

The MAX180/MAX181 operate with either the internal reference or an external -5V reference. In both cases, REFIN must be bypassed to AGND with a 47µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor to minimize noise and maintain a low impedance at high frequencies. REFIN is connected directly to the internal DAC, and the current load varies between 0mA and 1mA during conversion.

Internal Reference

The internal reference is buffered through an amplifier whose output connects to REFOUT. To operate the MAX180/MAX181 with the internal reference, connect REFIN to REFOUT. Do not connect a resistor between the bypass capacitors and REFIN. The reference buffer amplifier can sink 5mA for external loads. Adjust the reference output at REFADJ (Figure 14).

External Reference

With a -5V external reference, bypass REFIN to AGND with a 47µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. The reference source impedance must be less than 0.2Ω and must be able to sink the internal DAC load of 1mA. Connect REFOUT to V_{SS} and REFADJ to V_{DD} to prevent noise. If REFIN is driven above AGND during power sequencing, latchup can occur. Connect a Schottky clamp diode (IN5817) to prevent REFIN from substantially exceeding AGND.

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Table 1. Address vs. Channel Selection (see Figure 4)

	A2	A1	A0	SE/DIFF	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	COM
MAX180/MAX181	0	0	0	0	+								–
MAX180/MAX181	0	0	1	0		+							–
MAX180/MAX181	0	1	0	0			+						–
MAX180/MAX181	0	1	1	0				+					–
MAX180/MAX181	1	0	0	0					+				–
MAX180/MAX181	1	0	1	0						+			–
MAX180	1	1	0	0							+		–
MAX181	1	1	0	0		MUXOUT CONNECTED TO AGND							+, –
MAX180	1	1	1	0								+	–
MAX181	1	1	1	0		CH 0-5, AND MUXOUT ARE OPEN							–
MAX180/MAX181	0	0	0	1	+	–							
MAX180/MAX181	0	0	1	1	–	+							
MAX180/MAX181	0	1	0	1			+	–					
MAX180/MAX181	0	1	1	1			–	+					
MAX180/MAX181	1	0	0	1					+	–			
MAX180/MAX181	1	0	1	1					–	+			
MAX180	1	1	0	1							+	–	
MAX180	1	1	1	1							–	+	
MAX181	1	1	0	1		MUXOUT CONNECTED TO AGND							+, –
MAX181	1	1	1	1		CH 0-5, AND MUXOUT ARE OPEN							–

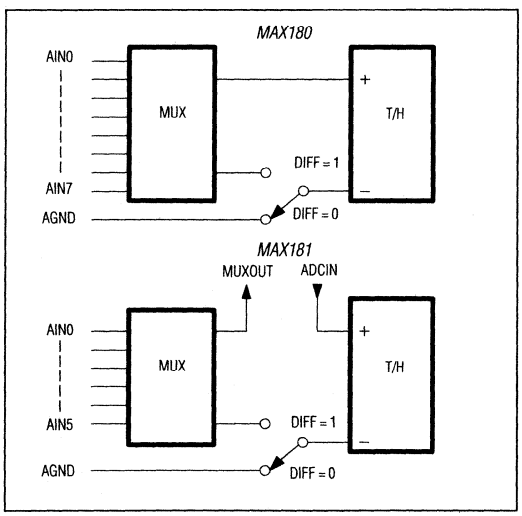

Figure 5. Multiplexer channel configuration

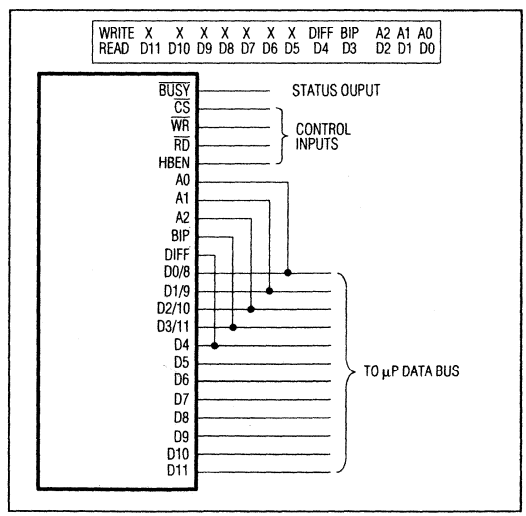

Figure 6. Input/Output Port Mode (12-Bit-Wide Data Bus Shown)

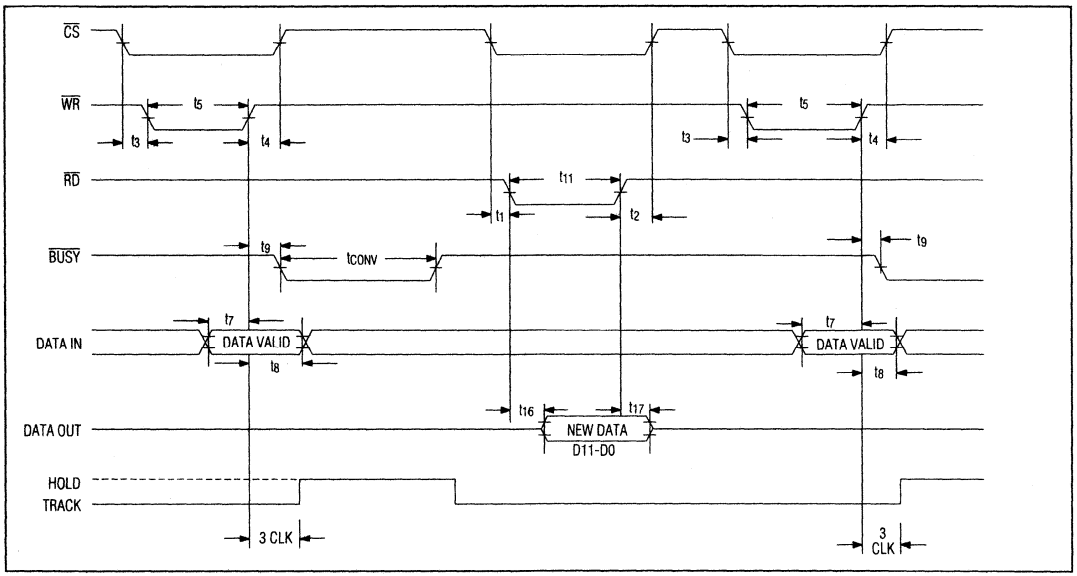

Figure 7a. Input/Output Port-Mode timing, parallel read (MODE = 1, HBEN = 0).

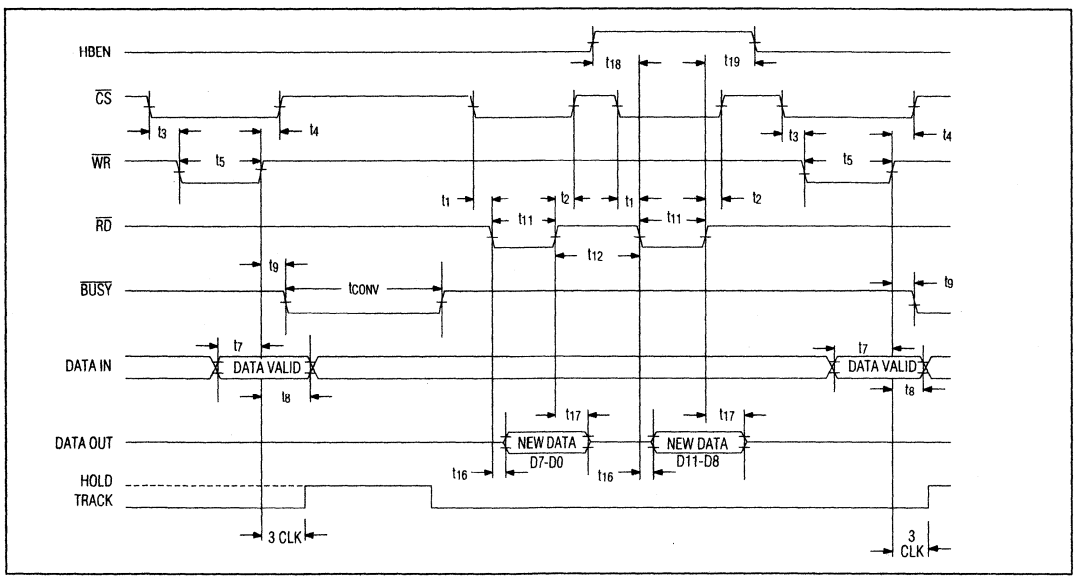

Figure 7b. Input/Output Port-Mode timing, two-byte read (MODE = 1).

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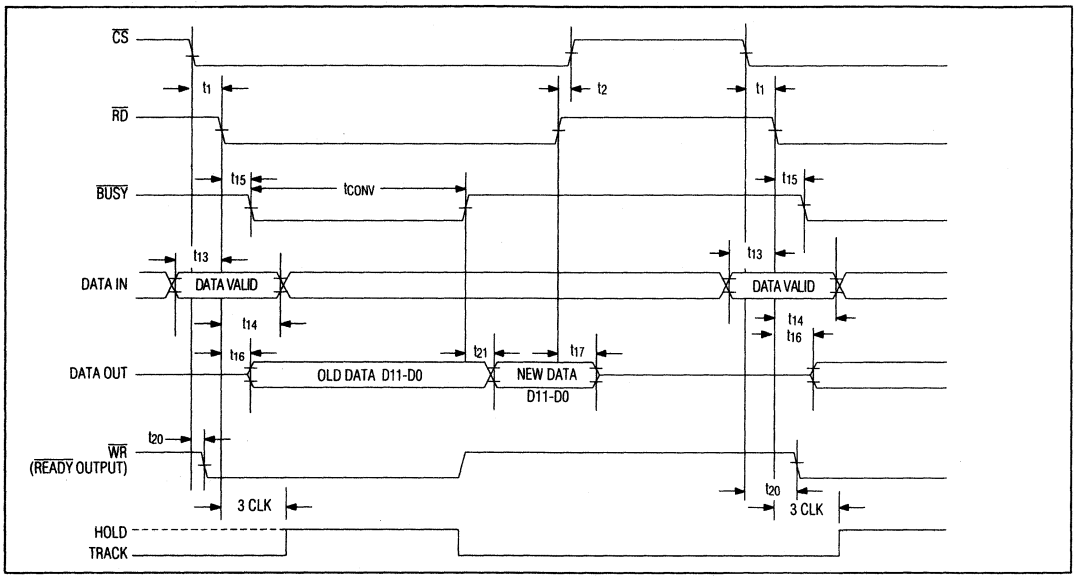

Figure 8a. Slow Memory Mode timing, parallel read (MODE = 0, HBEN = 0).

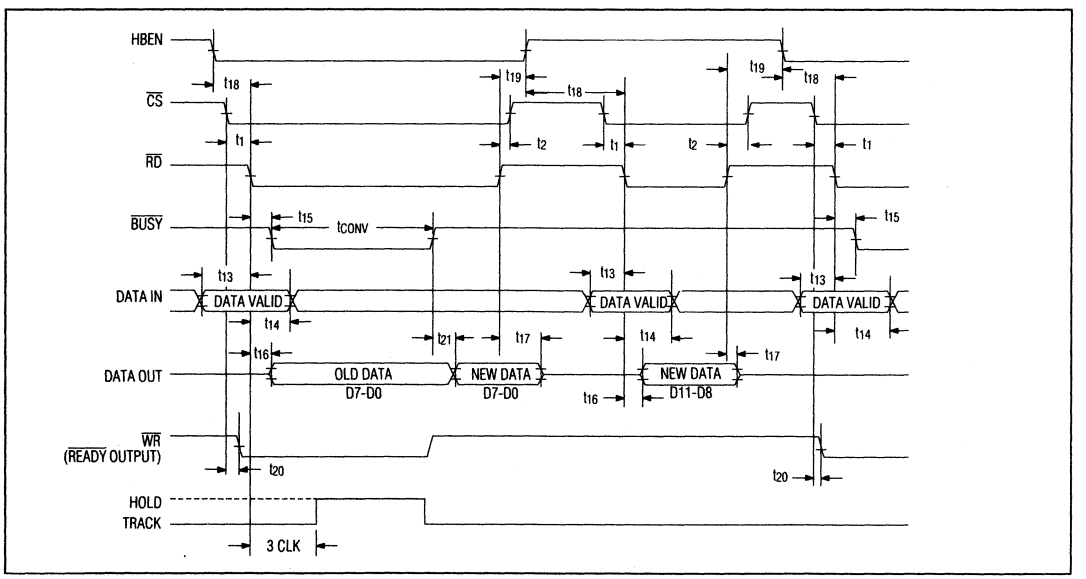

Figure 8b. Slow Memory Mode timing, two-byte read (MODE = 0).

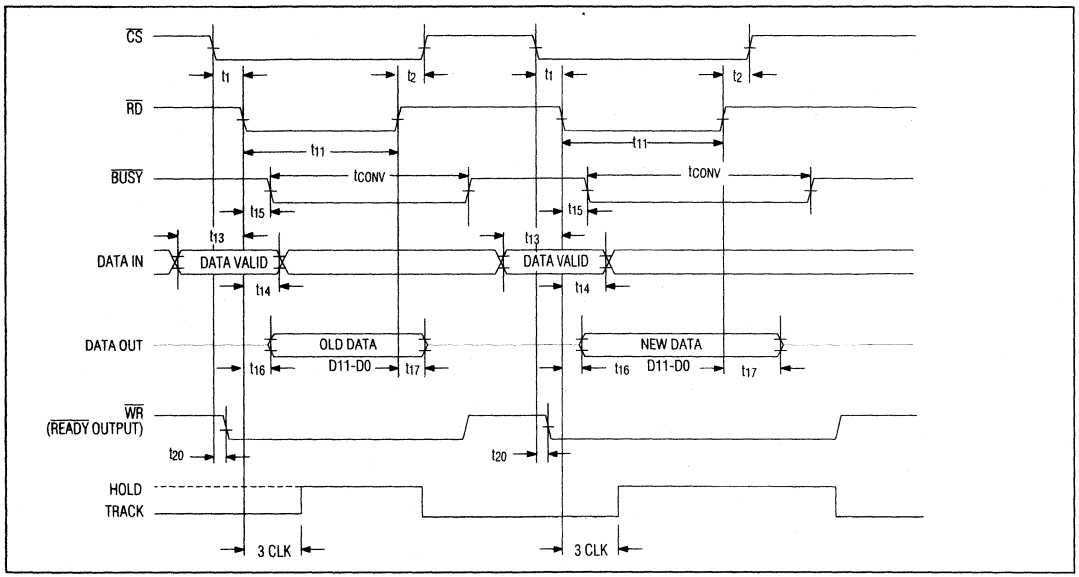

Figure 9a. ROM Mode timing, parallel read (MODE = 0, HBEN = 0).

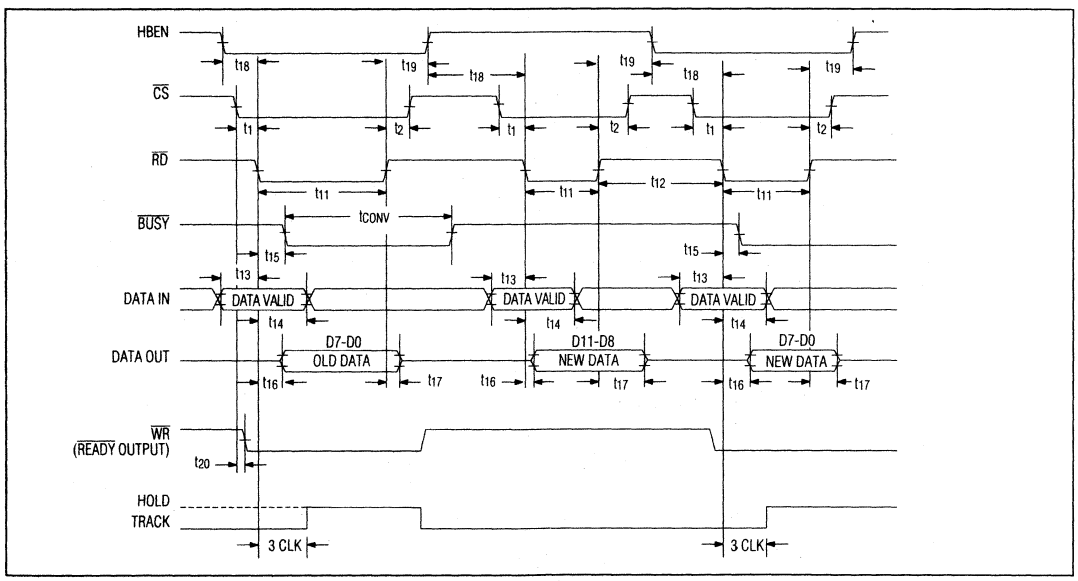

Figure 9b. ROM Mode timing, two-byte read (MODE = 0).

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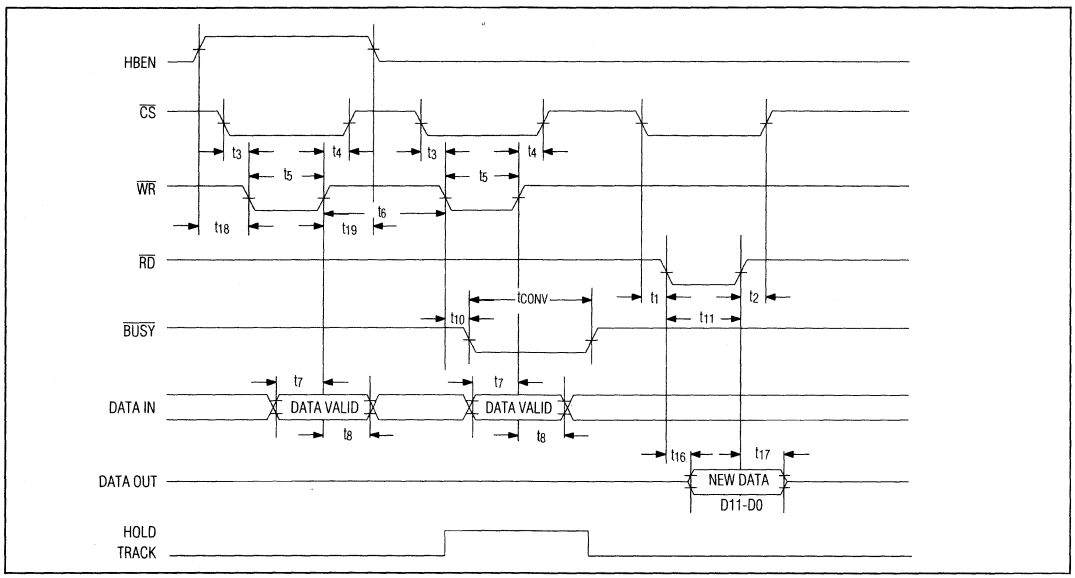

Figure 10a. Asynchronous Hold Mode timing, parallel read (MODE = open circuit)

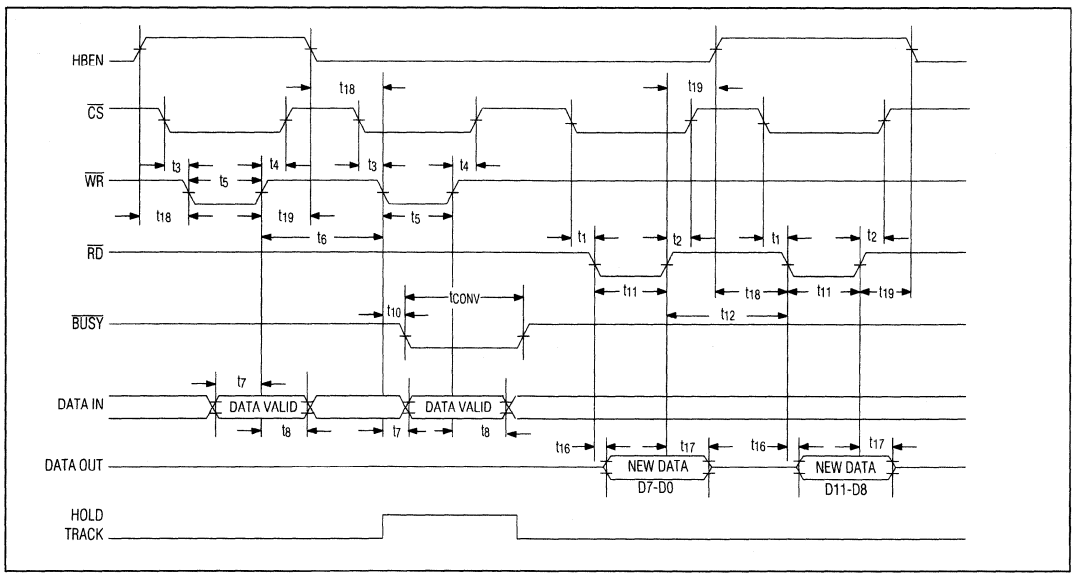

Figure 10b. Asynchronous Hold Mode timing, two-byte read (MODE = open circuit)

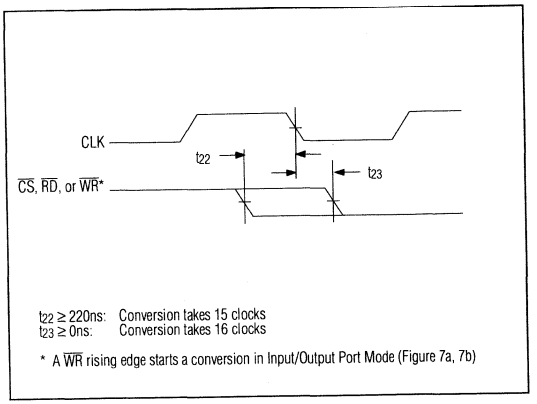

Figure 11. CS, RD, or WR to CLK Setup and Hold Time for Synchronous Operation

Digital Interface

Input/Output Port Mode (MODE = 1)

In this mode, data inputs and outputs are usually connected together (Figure 6), and the µP writes the configuration data to the DAS internal register with a write instruction (Figure 7). This starts a conversion, as indicated by the high-to-low transition of BUSY. The mux connects the selected input channel to the T/H, which acquires the signal during the first 3 clock cycles. On the falling edge of the 3rd clock, the T/H switches to hold mode, and the A/D conversion starts. 15 clock cycles after WR goes high, BUSY goes high, and the conversion result latches into three-state output buffers. The µP can then access the conversion result with a read instruction. For 16-bit bus operation, HBEN = 0, and the 12-bit result is read directly. For 8-bit bus operation, HBEN = 0 during the conversion, and the read instruction returns the 8 LSBs. A second read with HBEN = 1 returns the 4 MSBs in the low nibble. Note: In any mode, HBEN = 1 disables conversion start.

The DAS internal register is 5 bits wide: 3 bits for the analog-channel address, 1 bit for single-ended/differential mux operation, and 1 bit for unipolar/bipolar A/D operation.

Slow Memory Mode (MODE = 0)

The DAS appears to the µP as memory or as a slow peripheral in memory mode. The 5 configuration bits can be preset by an external data latch, a decoded device address, or any external selection logic. A read instruction initiates a conversion as shown in Figure 8. In this mode, the WR input functions as the RDY output and goes low when CS goes low. BUSY goes low after RD goes low, indicating the beginning of a signal acquisition cycle, and can be used to place the µP into a wait state. When the conversion is complete, BUSY releases the µP from its wait state. The µP can then access the conversion result with a read instruction. For 16-bit bus operation, HBEN = 0, and the 12-bit result is read directly. For 8-bit bus operation, HBEN = 0 during the conversion, and the read instruction returns the 8 LSBs. A second read with HBEN = 1 returns the 4 MSBs in the low nibble. Note: In any mode, HBEN = 1 disables conversion start.

ROM Mode, Parallel Read (MODE = 0)

ROM mode avoids using µP wait states. A conversion starts with a read instruction, and the 12 data bits from the previous conversion appear at D11-D0. The data from the first read in a sequence is often disregarded when ROM mode is used. A second read accesses the results of the first conversion and starts a new conversion. The time between successive reads must be longer than the conversion time of the MAX180/MAX181 (Figure 9a, 16-bit bus).

ROM Mode, 2-Byte Read (MODE = 0)

As in memory mode, only D7-D0 are used for a 2-byte read. A conversion starts with a read instruction when HBEN is low. At this point, the data outputs contain the 8 LSBs from the previous conversion. Two more read operations are needed to access the conversion result. The first, with HBEN high, accesses the 4 MSBs with 4 leading zeros. The second read, with HBEN low, outputs the 8 LSBs and starts a new conversion. Figure 9b (8-bit bus) details this mode.

Asynchronous Hold Mode (MODE = Open)

Asynchronous hold mode is helpful when a precise or repeatable sample timing is required. Asynchronous hold is very similar to the I/O port mode, except two write instructions are required. The first write, with HBEN = 1, configures the MAX180/MAX181 and connects the selected channel to the T/H input; the second write, with HBEN = 0, places the T/H into hold and starts the conversion. In other words, the three-clock cycle delay for T/H acquisition can be changed by controlling when the second write instruction occurs. The falling edge of the second WR pulse places the T/H into hold (Figure 10).

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External Clock

The range for the external clock duty cycle is between 20% and 80%. A precise square wave is not required.

Clock and Control Synchronization

For best analog performance, the MAX180/MAX181 clock should be synchronized to the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs (Figure 11) with at least 100ns separating convert start from the nearest clock edge. This synchronization ensures that transitions at CLKIN are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough is only a few millivolts. If CLKIN and convert start ($\overline{CS}$, $\overline{WR}$ and $\overline{RD}$) are asynchronous, frequency components caused by mixing of the clock and convert signals can increase the apparent input noise.

When the clock and convert signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough, but even these errors are eliminated by ensuring that the start of a conversion ($\overline{RD}$ or $\overline{WR}$ and $\overline{CS}$ falling edge) does not occur within 100ns of a clock transition (Figure 11).

Output Data Format

The 12 data bits can be output either in full parallel or as two 8-bit bytes. Table 2 shows the data-bus output format. To obtain parallel output for 16-bit µPs, HBEN is tied low. Note: The output data, D11-D0, is right-justified (i.e. D0, the LSB, is the right-most bit in the 16-bit word).

A two-byte read makes use of outputs D7-D0. Byte selection is controlled by HBEN, which multiplexes the data outputs. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0-D3 with the leading 4 bits low in locations D4-D7. Note: The 4 MSBs always appear at D11-D8 when the outputs are enabled, regardless of the state of HBEN.

Application Hints

Initialization After Power-Up

In some applications, power is removed from the ADC during periods of inactivity to conserve power. This is increasingly common in battery-powered systems. To initialize the MAX180/MAX181 at power-up, execute a read operation with HBEN low, ignoring the data outputs.

Minimizing System-Induced Noise

The MAX180/MAX181 are insensitive to most noise sources, especially when the layout, bypass, and grounding recommendations are followed. The following practices should also be considered:

1. Minimize digital activity during conversion, especially activity that is asynchronous with the MAX180/MAX181 clock.
2. Avoid data-bus activity within ±20ns of the CLKIN falling edge.

If the data bus connected to the ADC is active during a conversion, coupling from the data pins to the ADC comparator can cause errors. Using slow-memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, the bus should be isolated from the ADC using three-state drivers if the data bus is active during the conversion.

In ROM mode, the ADC generates considerable digital noise when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after conversion start. This noise can affect the ADC comparator and cause large errors if it coincides with the SAR latching a comparator decision. To prevent this, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high on a rising edge of CLKIN because the comparator output is latched on the falling edge of CLKIN.

Table 2. Data-Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

DIP Pin #	Pin 16	Pin 17	Pin 18	Pin 19	Pin 21	Pin 22	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28
Pin Label*	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = LOW**	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = HIGH**	D11	D10	D9	D8	LOW	LOW	LOW	LOW	D11	D10	D9	D8

Note: * D11–D0 are the ADC data output pin names.
** D11–D0 are the 12-bit conversion results. D11 is the MSB.

Layout, Grounding, Bypassing

Use printed circuit boards for best system performance; wire-wrap boards are not recommended. The board layout should ensure that digital- and analog-signal lines are separated as much as possible. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

Figure 12a shows the recommended system-ground connections. A single-point analog STAR ground should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this STAR ground, and no other digital system grounds should be connected here. For noise-free operation, the ground return to the power supply from this STAR ground should be low impedance and as short as possible.

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog STAR ground with 0.1µF and 47µF bypass capacitors. Minimize capacitor lead length for best supply noise rejection. If the 5V power supply is very noisy, connect a small (10Ω) resistor to filter the noise (Figure 12b).

Gain and Offset Adjustment

Figure 13 plots the nominal unipolar I/O transfer function of the MAX180/MAX181. Code transitions occur halfway between successive integer LSB values. Output coding for unipolar operation is natural binary with 1LSB = 1.22mV (5V/4096). Figure 14 shows the bipolar-input transfer function, where output coding is twos-complement.

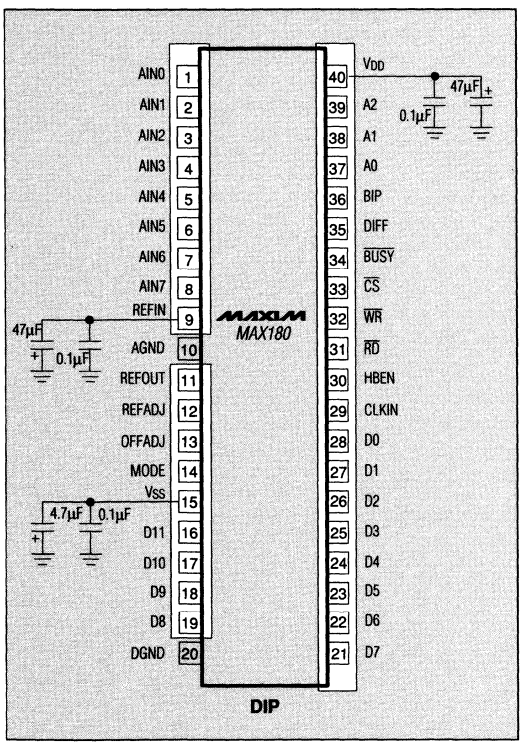

Figure 12a. Recommended Grounding and Ground Plane

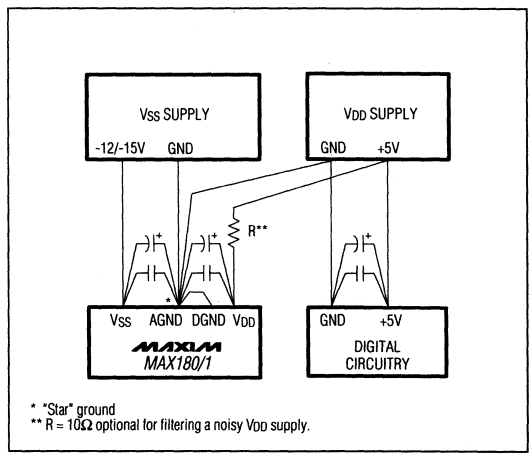

Figure 12b. Power-Supply Grounding

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

If offset and gain adjustments are not desired, connect OFFADJ and REFADJ to V_{DD}. Figure 15's circuit provides ±1.2% (±50 LSBs) of adjustment range for gain and ±0.44% (±18LSBs) of adjustment range for offset. This is ideal for applications that require gain (full-scale range) or offset adjustment. If the adjustment inputs are used, bypass to AGND with a 0.1µF capacitor. Offset should be adjusted before gain. For the 0V to 5V input range, apply LSB (0.61mV) to the analog input, and adjust R1 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply FS - 1LSB (4.99817V), and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111. There may be a slight interaction between the adjustments.

To adjust bipolar (±2.5V) offset, apply LSB (0.61mV) to the analog input, and adjust R1 until the output code switches between 0000 0000 0000 and 0000 0000 0001. For full scale, apply FS - 1LSB (2.49817V) to the input, and adjust R2 so the output code switches between 0111 1111 1110 and 0111 1111 1111 (Figure 15). There may be some interaction between these adjustments. If an external reference is used, adjust gain by varying the value of the reference instead of R2.

Dynamic Performance

Wide-bandwidth analog input and 100kHz throughput make the MAX180/MAX181 ideal for wideband-signal processing. To support these and other related applications, fast Fourier transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm that determines its spectral content. Conversion errors are seen as spectral elements outside of the fundamental input frequency.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error and integral (INL) and differential (DNL) nonlinearity. Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of the various DC parameters does not translate well to the dynamic case, so different tests are required.

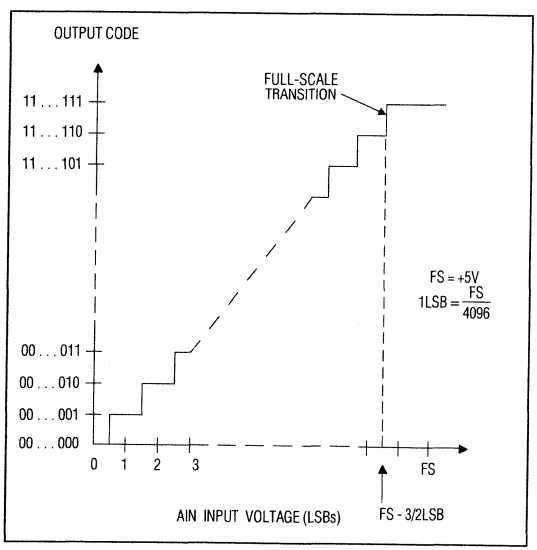

Figure 13. MAX180/MAX181 Unipolar Transfer Function

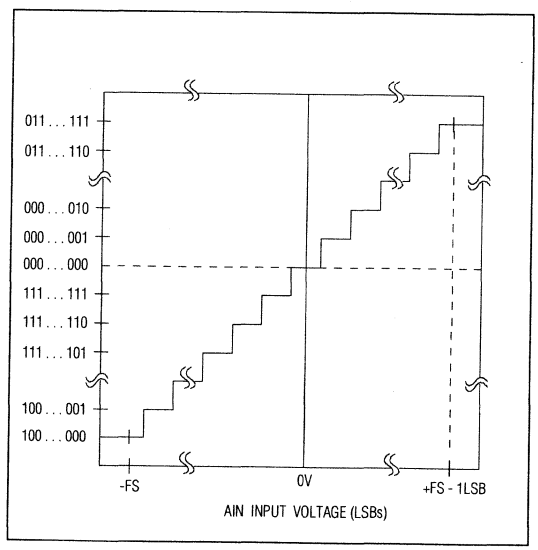

Figure 14. MAX180/MAX181 Bipolar Transfer Function

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental frequency to the RMS amplitude of all other ADC spectral components, excluding harmonics. The output band is limited to frequencies above DC and below one-half the ADC sample (conversion) rate. This band includes both distortion and noise components. For this reason, the signal-to-noise and distortion ratio (SINAD) is a better measure of the ADC's performance.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution:

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits of resolution. A perfect 12-bit ADC can therefore do no better than 74dB. Figure 16 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX180/MAX181. An output FFT plot shows the relative output amplitude at discrete spectral frequencies (Figure 16).

By transposing the equation that converts resolution to SNR, we can determine the effective resolution (effective number of bits) the ADC provides from the measured SNR: N = (SNR - 1.76)/6.02. Figure 17 shows the effective number of bits as a function of the input frequency for the MAX180/MAX181.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate) to the RMS amplitude of the fundamental frequency. This is expressed as:

$$THD = 20\text{Log}\left[\frac{\sqrt{(V_2^2 + V_3^2 + \ldots + V_N^2)}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if

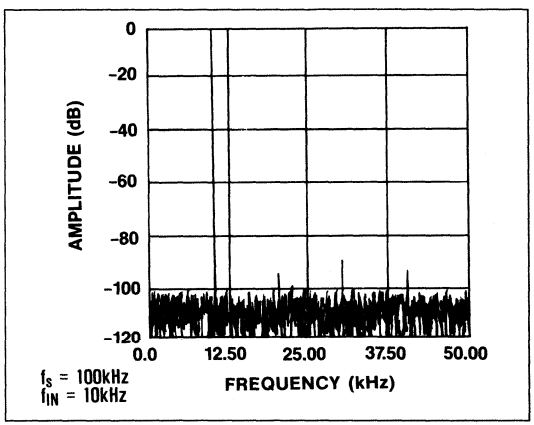

Figure 16. FFT Plot for the MAX180/MAX181

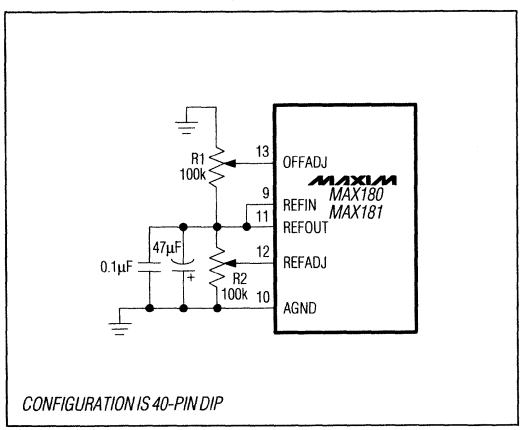

Figure 15. Offset and Gain Adjustment

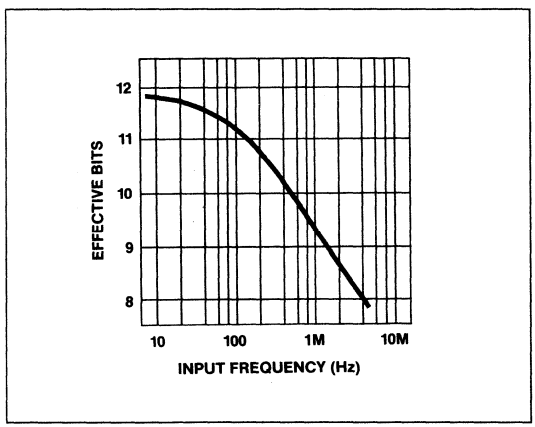

Figure 17. MAX180/MAX181 Effective Bits vs. Input Frequency

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Typical Applications

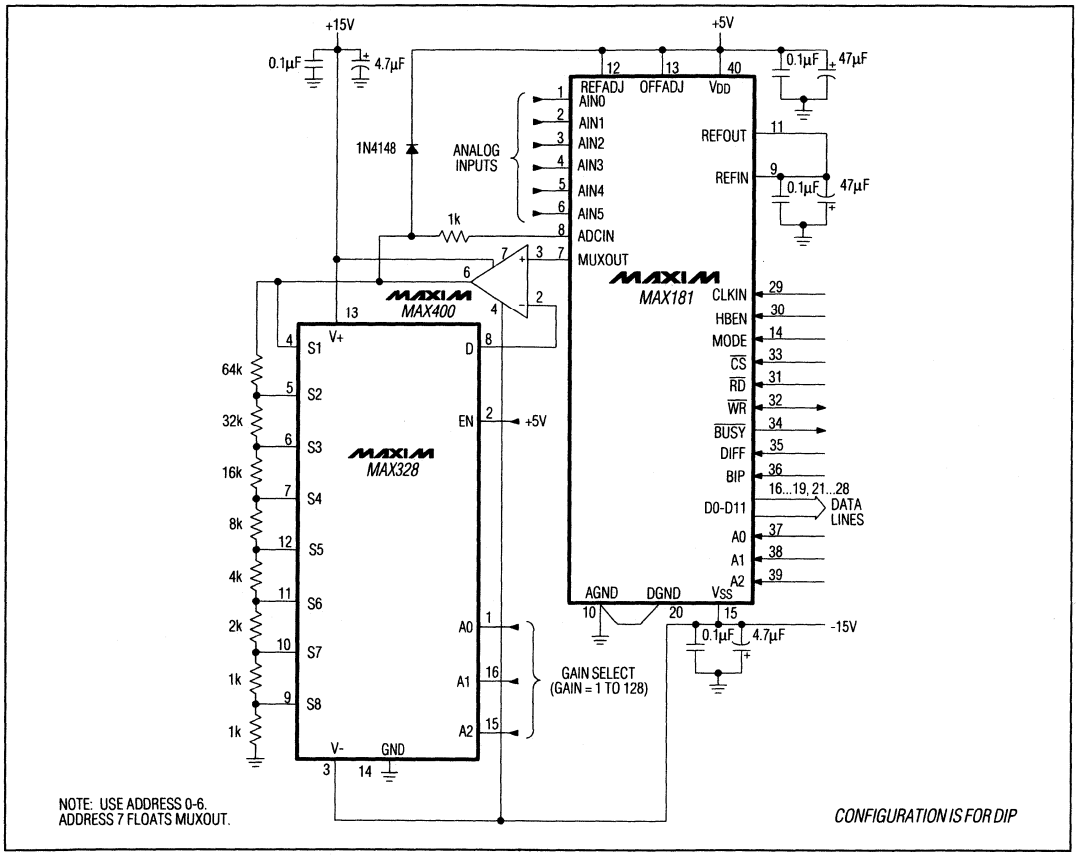


Figure 18a. MAX181 operating as a 6-channel programmable gain ADC. Gains are 1, 2, 4, 8, 16, 32, 64, and 128.

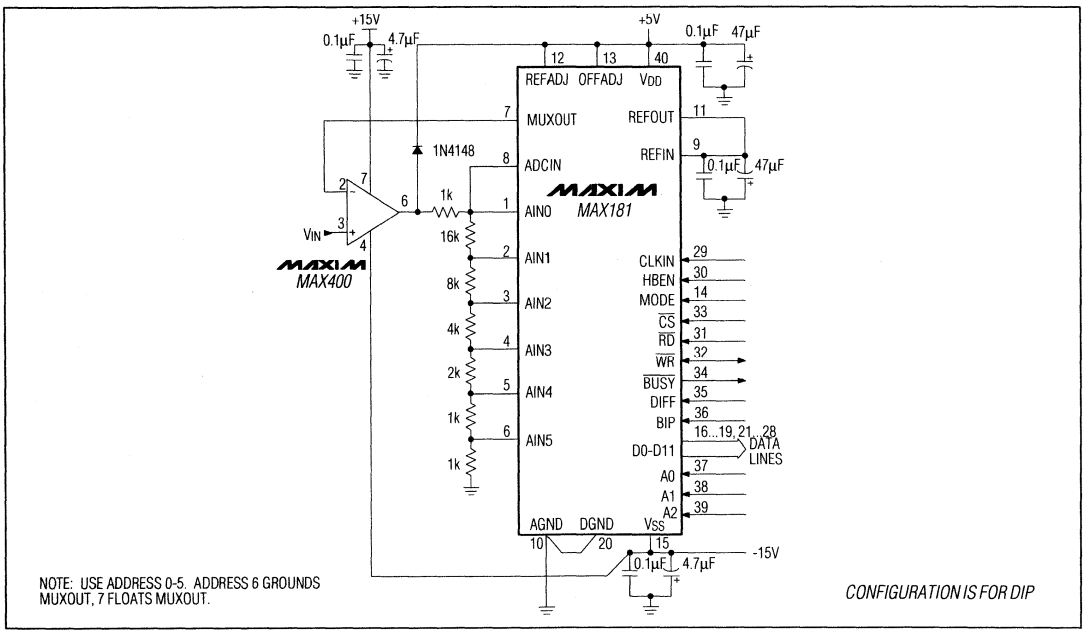
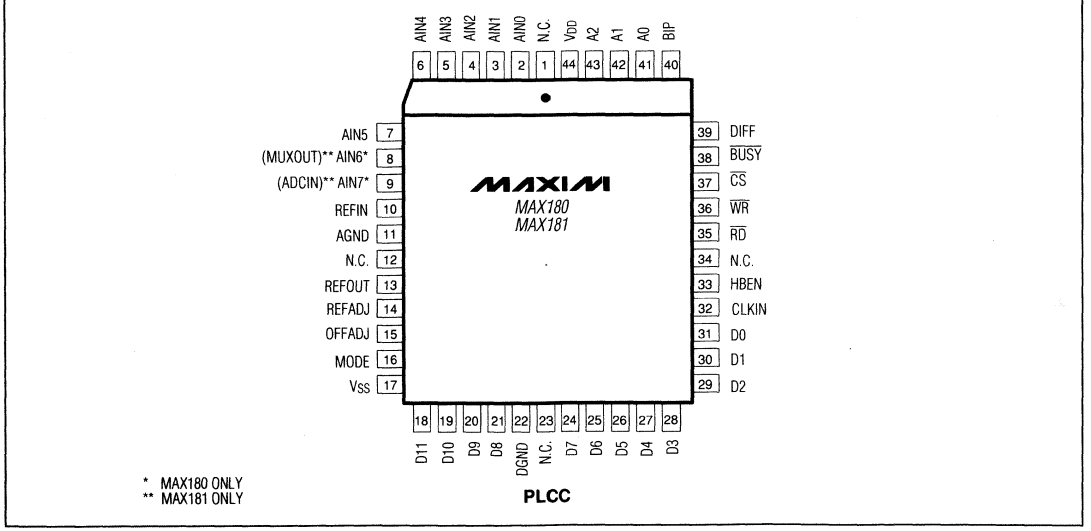


Figure 18b. MAX181 operating as a single-channel programmable gain ADC. Gains are 1, 2, 4, 16, and 32.

Pin Configurations (continued)



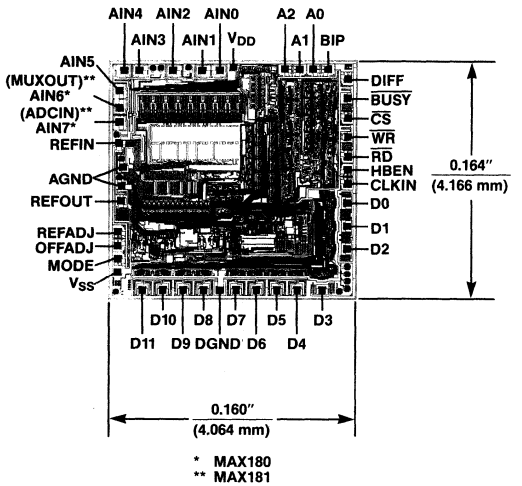
Complete, 8-Channel, 12-Bit Data-Acquisition Systems

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX180CCQH	0°C to +70°C	44 PLCC	±1
MAX180CC/D	0°C to +70°C	Dice*	±1
MAX180AEPL	-40°C to +85°C	40 Plastic DIP	±1/2
MAX180BEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX180CEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX180AEQH	-40°C to +85°C	44 PLCC	±1/2
MAX180BEQH	-40°C to +85°C	44 PLCC	±1
MAX180CEQH	-40°C to +85°C	44 PLCC	±1
MAX180AMJL	-55°C to +125°C	40 CERDIP**	±1/2
MAX180BMJL	-55°C to +125°C	40 CERDIP**	±1
MAX180CMJL	-55°C to +125°C	40 CERDIP**	±1
MAX181ACPL	0°C to +70°C	40 Plastic DIP	±1/2
MAX181BCPL	0°C to +70°C	40 Plastic DIP	±1
MAX181CCPL	0°C to +70°C	40 Plastic DIP	±1
MAX181ACQH	0°C to +70°C	44 PLCC	±1/2
MAX181BCQH	0°C to +70°C	44 PLCC	±1
MAX181CCQH	0°C to +70°C	44 PLCC	±1
MAX181CC/D	0°C to +70°C	Dice*	±1
MAX181AEPL	-40°C to +85°C	40 Plastic DIP	±1/2
MAX181BEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX181CEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX181AEQH	-40°C to +85°C	44 PLCC	±1/2
MAX181BEQH	-40°C to +85°C	44 PLCC	±1
MAX181CEQH	-40°C to +85°C	44 PLCC	±1
MAX181AMJL	-55°C to +125°C	40 CERDIP**	±1/2
MAX181BMJL	-55°C to +125°C	40 CERDIP**	±1
MAX181CMJL	-55°C to +125°C	40 CERDIP**	±1

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



* MAX180
** MAX181

MAXIM

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

General Description

The MAX182 is a complete, calibrated 4-channel 12-bit A/D converter (ADC) which includes a precision voltage reference, track-and-hold, and conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each 60µs conversion includes an auto-zero cycle which reduces zero errors to typically below 100µV.

$\overline{\text{CHIP SELECT}}$, $\overline{\text{READ}}$, and $\overline{\text{WRITE}}$ inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two address bits control the 4-channel input multiplexer.

The MAX182's analog input range is 0V to +5V when using a +5V reference. All four high-impedance input channels have excellent matching (typically 0.05 LSB). The MAX182A's internal reference accuracy is ±0.3%, while the MAX182B is intended for use with an external reference.

Applications

Digital-Signal Processing

Audio and Telecom Processing

High-Speed Data Acquisition

High-Accuracy Process Control

Features

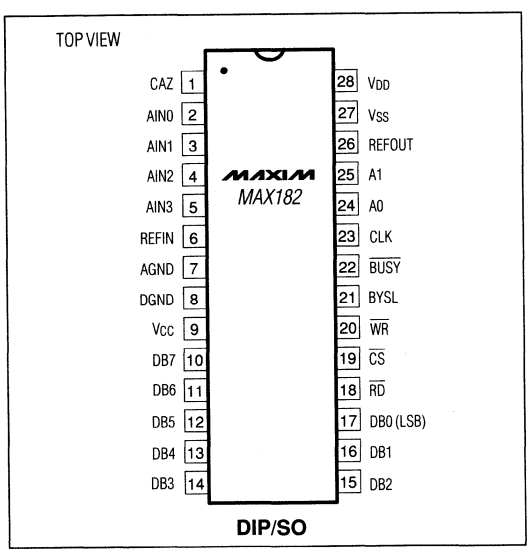
- ♦ **Continuous Transparent Calibration of Offset and Gain**
- ♦ **True 12-Bit Performance without Adjustments**
- ♦ **T/H Front End and Internal Reference**
- ♦ **Four High-Impedance Input Channels**
- ♦ **DC and Dynamically Specified**
- ♦ **Zero Error Typically < 100µV**
- ♦ **Standard Microprocessor Interface**
- ♦ **28-Pin DIP and Wide SO Packages**

Ordering Information

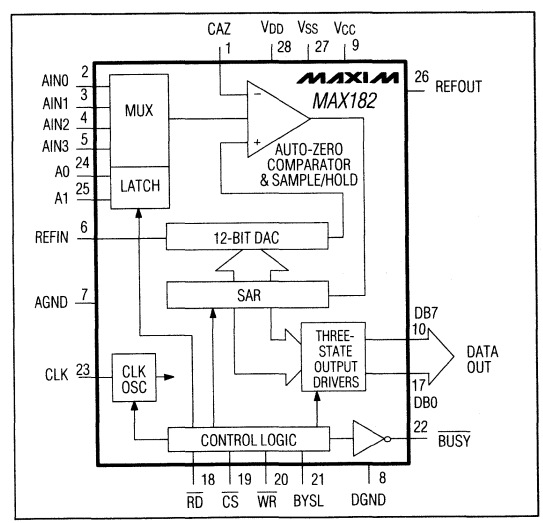
PART	TEMP. RANGE	PIN-PACKAGE
MAX182ACPI	0°C to +70°C	28 Plastic DIP
MAX182BCPI	0°C to +70°C	28 Plastic DIP
MAX182ACWI	0°C to +70°C	28 Wide SO*
MAX182BCWI	0°C to +70°C	28 Wide SO*
MAX182BC/D	0°C to +70°C	Dice**
MAX182AEPI	-40°C to +85°C	28 Plastic DIP
MAX182BEPI	-40°C to +85°C	28 Plastic DIP
MAX182AEWI	-40°C to +85°C	28 Wide SO*
MAX182BEWI	-40°C to +85°C	28 Wide SO*
MAX182AMJI	-55°C to +125°C	28 CERDIP*
MAX182BMJI	-55°C to +125°C	28 CERDIP*

* *Consult factory.*
** *Consult factory for dice specifications*

Pin Configuration



Functional Diagram



Calibrated 4-Channel 12-Bit ADC with T/H and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... +0.3V, -7V
AGND to DGND ..... -0.3V, REFIN +0.3V
V_{CC} to DGND ..... -0.3V, +7V
REFIN to AGND ..... -0.3V, V_{DD} +0.3V
AIN to AGND ..... -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND ..... -0.3V, V_{DD} +0.3V

Power Dissipation (any Package)
To +75°C 1,000mW
Derate above +75°C by 10mW/C
Operating Temperature Ranges:
MAX182_C ..... 0°C to +70°C
MAX182_E ..... -40°C to +85°C
MAX182_M ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} =266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Total Unadjusted Error (Note 1)	TUE	AIN0-AIN3			±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Full-Scale Error (Gain Error)		AIN0-AIN3 | T_A = +25°C			±1/2	LSB
Full-Scale Tempco				0.5		ppm/°C
Zero Error		AIN0-AIN3 | T_A = +25°C			±1/2	LSB
Zero Tempco				0.5		ppm/°C
Channel-to-Channel Mismatch					±1/2	LSB
ANALOG INPUT						
Input Voltage Range		V_{REF} = +5V	0		+5	V
On-Channel Input Capacitance	C_{AIN}			8		pF
Input Leakage Current	I_{AIN}	AIN0-AIN3 = 0V to +5V: T_A = +25°C T_A = T_{MIN} to T_{MAX}			10 100	nA
DYNAMIC ACCURACY ($f_{\overline{WR}}$ = 14.81kHz, f_{AIN} = 2.011kHz, T_A = 25°C, Note 2)						
Signal-to-Noise + Distortion	S/(N + D)		70			dB
Total Harmonic Distortion	THD	2kHz Input Signal T_A = +25°C			-80	dB
Peak Harmonic or Spurious Noise					-80	dB
REFERENCE INPUT						
REFIN Range	V_{REFIN}	For specified performance		+5 ±5%		V
		Degraded transfer accuracy	+4		+6	
REFIN Input Current		REFIN = +5V			1.0	mA
REFERENCE OUTPUT						
MAX182A						
REFOUT Voltage		T_A = +25°C	+4.985	+5	+5.015	V
REFOUT Temp (C°)				±10	±40	ppm/°C
REFOUT Sink Current					1	mA
MAX182B Use External Reference Only						

ELECTRICAL CHARACTERISTIC (continued)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (RD, CS, WR, BYSL, A0, A1)						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+2.4			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input Current	I_{IN}	V_{IN} = 0 to V_{CC}: T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance	C_{IN}	(Note 3)			10	pF
CLOCK						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+3.0			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input High Current	I_{IH}	V_{CC} = +5V ±5%			1.5	mA
Input Low Current	I_{IL}	V_{CC} = +5V ±5%			1.2	mA
LOGIC OUTPUTS (DB0-DB7, BUSY)						
Output High Voltage	V_{OH}	V_{CC} = +5V ±5%, I_{SOURCE} = 200µA	+4.0			V
Output Low Voltage	V_{OL}	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA			+0.4	V
Floating State Leakage Current (DB0-DB7)	I_{LKG}	V_{OUT} = 0V to V_{CC}			±1	µA
Floating State Output Capacitance (DB0-DB7)	C_{OUT}	(Note 3)			15	pF
CONVERSION TIME (Note 4)						
With External Clock		f_{CLK} = 266.67kHz	60			µs
With Internal Clock		T_A = +25°C	90		140	µs
POWER REQUIREMENTS (Note 5)						
Power-Supply Voltage	V_{DD}		+11.4		+15.75	V
	V_{SS}		-4.75		-5.25	
	V_{CC}		+4.75		+5.25	
V_{DD} Supply Rejection		V_{DD} = +14.25V to +15.75V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		V_{SS} = -4.75V to -5.25V, V_{DD} = +15V		±1/8		LSB
V_{DD} Supply Rejection		V_{DD} = +11.4V to +12.6V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		V_{SS} = -4.75V to -5.25V, V_{DD} = +12V		±1/8		LSB
Power-Supply Current	I_{DD}	V_{IN} = V_{IL} or V_{IH}		6	10	mA
	I_{SS}				8	
	I_{CC}			0.1	1.0	

Note 1: Includes: Full-Scale Error, Offset Error, Relative Accuracy.
Note 2: Up to 5th Harmonic is measured.
Note 3: Guaranteed by design.
Note 4: Track/Hold aquisition time included in conversion time, using t_{13} condition (see Timing Characteristics).
Note 5: Power-supply current is measured when MAX182 is inactive (CS = WR = RD = BUSY = High).

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

TIMING CHARACTERISTICS (Note 6, Figures 1 and 2)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C to +85°C			T_A = -55°C to +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0			0			0			ns
$\overline{WR}$ Pulse Width	t_2		120			120			120			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3		0			0			0			ns
$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	t_4			85	120		100	140		115	160	ns
A0, A1 Valid to $\overline{WR}$ Setup Time	t_5		0			0			0			ns
A0, A1 Valid to $\overline{WR}$ Hold Time	t_6		0			0			0			ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_7	(Note 3)	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_8		0			0			0			ns
$\overline{RD}$ Pulse Width	t_9		120			120			120			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{10}		0			0			0			ns
BYSL to $\overline{RD}$ Setup Time	t_{11}		50			50			50			ns
BYSL to $\overline{RD}$ Hold Time	t_{12}		0			0			0			ns
$\overline{RD}$ to Valid Data (Note 7)	t_{13}	(Bus Access Time)		60	100		70	110		90	130	ns
$\overline{RD}$ to Three-State Output (Note 8)	t_{14}	(Bus Relinquish Time)	20		100	20		100	20		100	ns
$\overline{WR}$ to CLK for 16 Clock Conversions (Note 9)	t_{15}		20			20			20			ns
$\overline{WR}$ to CLK for 17 Clock Conversions (Note 9)	t_{16}		20			20			20			ns

Note 6: Data is timed from V_{OH}, V_{OL}; all input control signals are timed from a voltage level of +1.6V and specified with t_r = t_f = 20ns (10% to 90% of +5V).
Note 7: t_{11}, the time required for an output to cross 0.8V or 2.4V, is measured with the load circuits of Figure 3.
Note 8: t_{12}, the time required for the data lines to change 0.5V, is measured with the load circuits of Figure 4.
Note 9: See Figure 7.

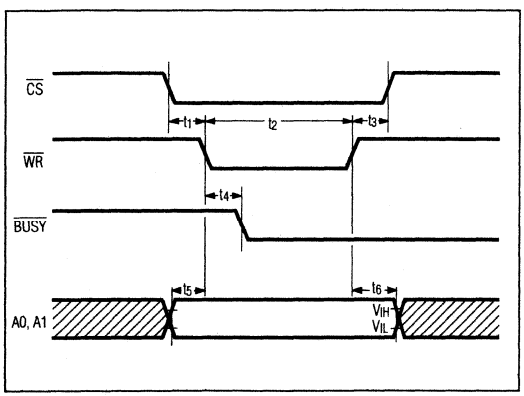


Figure 1: Start Cycle Timing

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

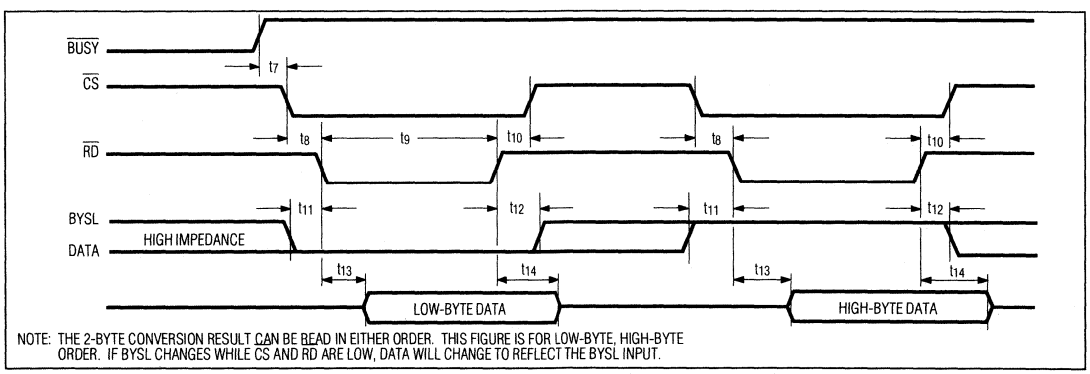
Pin Description

PIN	NAME	FUNCTION
1	CAZ	Auto-Zero Capicitor Input. Connect other end of capacitor to AGND.
2	AIN0	Analog Input for Channel 0
3	AIN1	Analog Input for Channel 1
4	AIN2	Analog Input for Channel 2
5	AIN3	Analog Input for Channel 3
6	REFIN	Voltage Reference Input. The MAX182 is specified with REFIN = +5V.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible for V_{CC} = +5V.
10-17	DB0-DB7	Three-State Data Outputs. Active when $\overline{CS}$ and $\overline{RD}$ are brought low. Individual pin functions depend upon BYTE SELECT (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$, $\overline{RD}$ = LOW		
PIN	**BYSL = HIGH**	**BYSL = LOW**
10	BUSY (Note 10)	DB7
11	LOW (Note 11)	DB6
12	LOW (Note 11)	DB5
13	LOW (Note 11)	DB4
14	DB11 (MSB)	DB3
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0 (LSB)

PIN	NAME	FUNCTION
18	$\overline{RD}$	$\overline{READ}$ Input. Used with $\overline{CS}$ to enable the three-state data outputs. $\overline{RD}$ is active low.
19	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input. Used with either $\overline{RD}$ or $\overline{WR}$ for control. $\overline{CS}$ is active low.
20	$\overline{WR}$	$\overline{WRITE}$ Input. In combination with $\overline{CS}$, this active low signal starts a new conversion.
21	BYSL	BYTE SELECT. BYSL selects high- or low-byte output during a data READ operation. ($\overline{RD}$, $\overline{CS}$ = low.) See pins 10-17.
22	$\overline{BUSY}$	Converter Status. $\overline{BUSY}$ is only low during conversion.
23	CLK	CLOCK Input. Internal clock operation with this pin floating and unloaded, typically results in 120µs conversion time (Figure 8). This can be shortened by using an external 74HC clock source (Figure 9).
24	A0	Address input A0. See description of A1.
25	A1	Address Input A1. Address inputs A0 and A1 determine the input channel to be digitized. The address input latch is available when $\overline{CS}$ and $\overline{WR}$ are low. The address inputs are entered by $\overline{WR}$ returning high. A1 A0 Channel Selected 0 0 AIN0 0 1 AIN1 1 0 AIN2 1 1 AIN3
26	REFOUT	Reference Output
27	V_{SS}	Negative Supply Voltage, -5V
28	V_{DD}	Positive Supply Voltage, +15V

Note 10: High during a conversion, *BUSY* is a converter status flag.
Note 11: *When BYSL is high, pins 11-13 output a logic low. The 12-bit digital result is in DB0-DB11.* DB11 is the MSB.



NOTE: THE 2-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. THIS FIGURE IS FOR LOW-BYTE, HIGH-BYTE ORDER. IF BYSL CHANGES WHILE CS AND RD ARE LOW, DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Detailed Operation

Operating Information

Figure 5 shows an operational diagram for the MAX182. The only required passive components are a hold capacitor (CAZ) and a reference bypass capacitor and resistor. Individual pin functions are listed in the Pin Description table.

On-Chip Clock Operation

The on-chip oscillator requires no external components. Therefore, the CLK pin can be left unconnected resulting in a typical 120µs conversion time. The conversion time can be increased by adding a capacitive load on the CLK pin. The timing diagrams in Figures 6 and 7 show the resulting tracking duration for relative positions of $\overline{WR}$ and CLK. Figure 8 is a schematic for on-chip clock operation.

A new conversion is initiated by bringing $\overline{WR}$ low, with $\overline{CS}$ low. This starts a track acquisition sequence. In this state, the T/H goes into track mode. Capacitor CAZ charges to the analog input voltage minus the input offset voltage of the comparator. Note: when $\overline{WR}$ is low (with $\overline{CS}$ low), the MAX182 is in track mode. When $\overline{WR}$ goes high, tracking time is extended by another 4 to 5 clock periods (4 clock periods beginning with the first falling clock edge following the rising edge of $\overline{WR}$). 16 to 17 clock periods are required for each conversion (Figure 7).

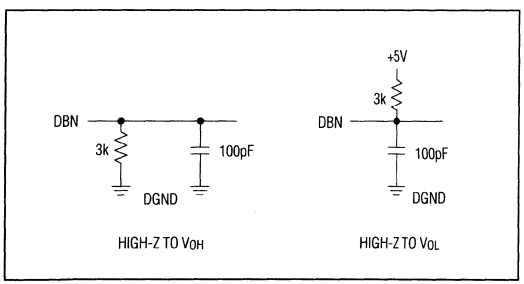


Figure 3. Load Circuits for Access Time Test (t_{13})

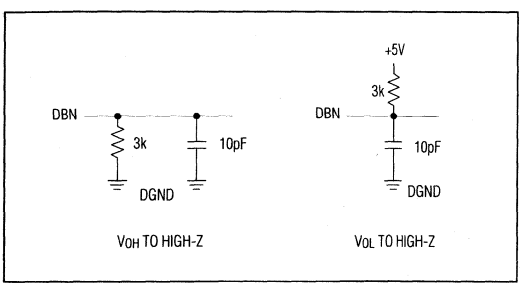


Figure 4. Load Circuits for Output Three-State Delay Test (t_{14})

The MAX182 is in track mode between conversions when $\overline{BUSY}$ is high. After the tracking sequence, the most significant bit (MSB) decision is made. Following this, the remaining 11 bits are digitized on successive clock cycles, as indicated in Figure 6. The $\overline{WR}$ pulse need not be synchronized with the internal clock.

External Clock Operation

For external clock operation, drive the CLK input with a 74HC compatible clock source (Figure 9).

The MAX182 automatically tracks for the appropriate time by means of an on-chip counter. Both $\overline{WR}$ and $\overline{CS}$ must be low to initiate a new conversion. Whenever $\overline{WR}$ and $\overline{CS}$ are low, the chip enters into track mode until $\overline{WR}$ or $\overline{CS}$ rises. After the rising edge of $\overline{WR}$, the next falling edge of the clock starts a counter, which extends the tracking time by 4 to 5 external clock periods.

The analog input acquisition is complete at the end of the tracking period, and the signal is stored in the internal track-and-hold. The external clock source need not be synchronized with the $\overline{WR}$ pulse.

Reading Data

The 12-bit result of a conversion plus the converter status flag are accessible over an 8-bit data bus. The data is available from the MAX182 in right-justified format (the least significant bit (LSB) is the right-most bit in a 16-bit word). Two byte sized read operations are needed. The Byte Select (BYSL) input determines which byte is to be read first, 8LSBs or 4MSBs plus status flag.

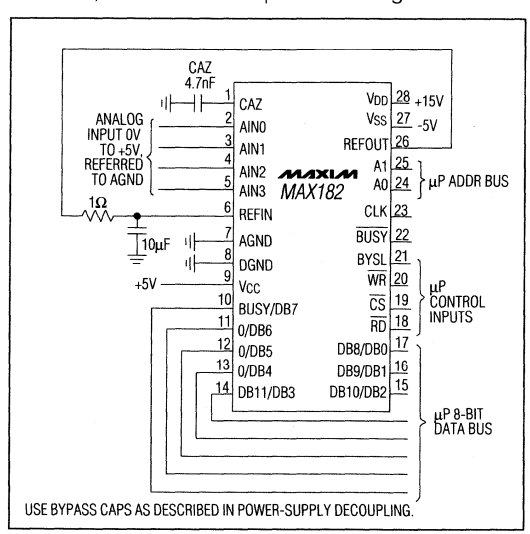


Figure 5. MAX182 Operational Diagram

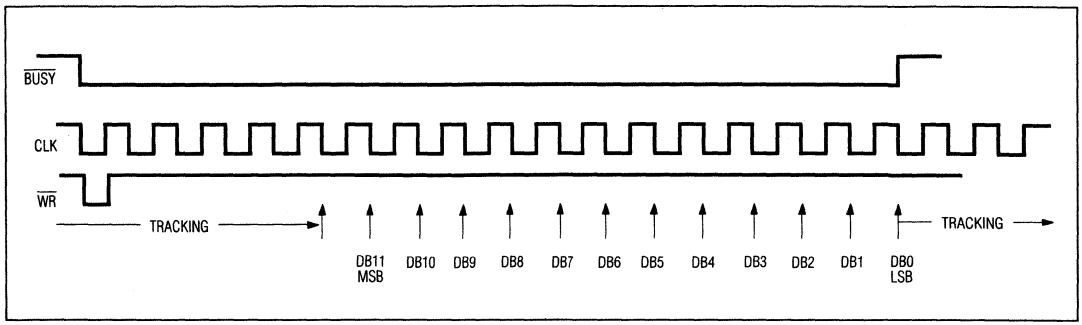


Figure 6. MAX182 Timing Diagram

It is necessary to wait for the end of a conversion to obtain valid 12-bit data from the MAX182's successive approximation register (SAR). If a read instruction is performed during a conversion, the MAX182 will dump the existing contents of the SAR onto the data bus. There are three methods to ensure correct operation:

1. Insert a software delay longer than the ADC conversion time between the conversion start and the data read operations.
2. The $\overline{BUSY}$ output is low during the conversion and high at the conversion end. Use this signal as an interrupt to the µP.
3. Poll the converter status flag, BUSY, at user-defined intervals after a conversion start. The status flag is available on DB7 during a high-byte $\overline{READ}$. The flag is the left-most bit and can be shifted directly into the µP's carry flag for testing. BUSY is high during a conversion.

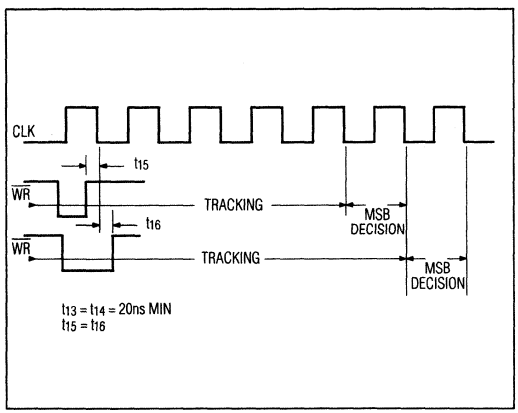


Figure 7. Width of Tracking Interval as a Function of $\overline{WR}$ Rising Edge Timing with Respect to CLK Falling Edge

A write operation to the MAX182 during a conversion restarts the conversion.

Application Hints

Auto-Zero Capacitor (CAZ)

CAZ (Figure 5) must be a low-leakage, low-dielectric absorption capacitor such as polypropylene, polystyrene, or teflon. Connect the outside foil of CAZ to AGND to minimize noise. CAZ should be 4,700pF.

Clock

Figure 10 shows typical conversion time versus temperature when using the MAX182's on-chip clock. Due to variations in manufacturing, the actual operating frequency can differ from chip-to-chip by up to 20%. For this reason, it is suggested that an external clock be used when fixed conversion times are required.

Analog Inputs

The high-impedance analog inputs, AIN0-AIN3, allow simple analog interfacing. Signal sources from 0V to +5V may be connected directly to AIN without extra buffering for source impedances up to 5kΩ (Figure 11). The input/output (I/O) transfer characteristic and transition

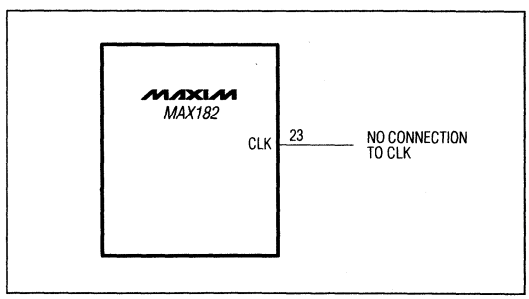


Figure 8. Internal Clock Operation

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

points for this input signal range are demonstrated in Figure 12 and Table 1. The MAX182 transfer characteristic has transition points designed to occur on integer multiples of 1LSB. The output code is natural binary with:

1LSB = (Full Scale (FS))/4096
= (5/4096)V = 1.22mV.

For signal ranges other than 0V to +5V, use resistor divider networks to provide 0V to +5V signal ranges at the MAX182 input pins. The connection in Figure 13 shows a divider network on channel 0 for a 0V to +10V signal range. Resistors should be of the same type and manufacturer to ensure matched temperture coefficients. The source impedance must now be as low as possible since it adds to the resistor divider impedance.

Figure 14 shows how bipolar signals (-5V to +5V) on channel 0 are accommodated by referencing a resistor divider network to REFIN. The signal source must be capable of sinking 0.5mA with the resistor values shown. Refer to Figure 15 and Table 2 for the I/O transfer characteristic and transition points for this signal range. Output coding is offset binary with an LSB size of:

(FS)(1/4096) = (10/4096)V = 2.44mV.

To adjust bipolar zero error apply 1.22mx (+1/2LSB) to AIN0-AIN3 so that the ADC output switches between 1000 0000 0000 and 1000 0000 0001.

Power-Supply Decoupling

Power supplies to the MAX182 should be bypassed with either a 10µF electrolytic or tantulum capacitor in parallel with a 0.01µF disc ceramic capacitor for clean, high-frequency performance. Place all capacitors as close as possible to the MAX182 supply pins. Figure 16 shows preferred decoupling circuit.

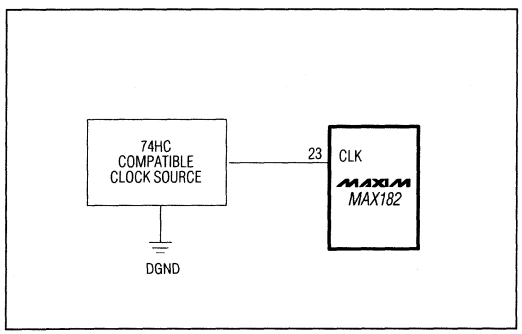


Figure 9. External Clock Operation

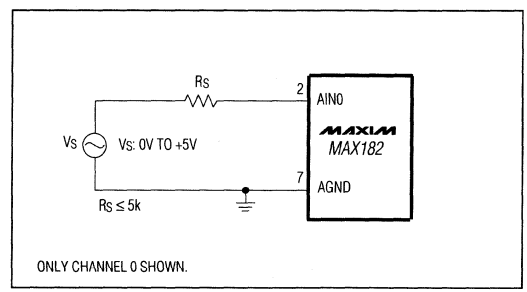


Figure 11. Unipolar 0V to +5V Operation

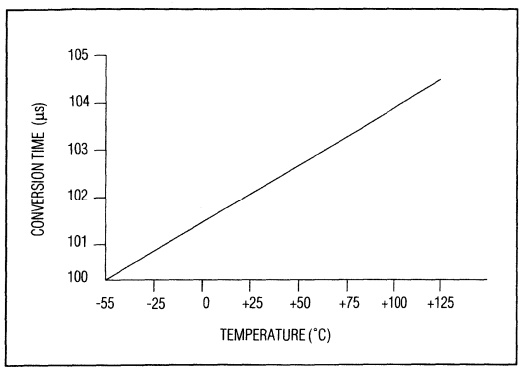


Figure 10. Typical Change in Conversion Time Variation vs. Temperature when Using Internal Clock

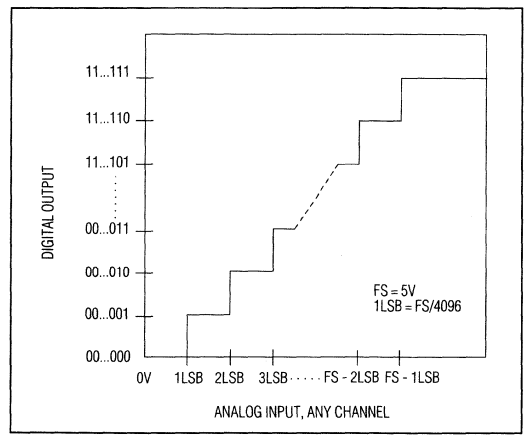


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Internal Reference

The internal reference (REFOUT) should be bypassed with a 1Ω resistor in series with a capacitor. The capacitor should be a 10µF electrolytic or tantalum in parallel with a 0.01µF disc ceramic (Figure 17). Figure 18 shows a circuit that allows input adjustment which is useful for trimming out initial (room temperature) error in the reference voltage.

Table 1. Transition Points for Unipolar 0V to +5V Operation

Analog Input (V)	Digital Output
0.00122	0000 0000 0001
0.00244	0000 0000 0010
. . .	. . .
2.49878	0111 1111 1111
2.50000	1000 0000 0000
2.50122	1000 0000 0001
. . .	. . .
4.99756	1111 1111 1110
4.99878	1111 1111 1111

Table 2. Transition Points for Bipolar -5V to +5V Operation

Analog Input (V)	Digital Output
-4.99878	0000 0000 0001
-4.99634	0000 0000 0010
. . .	. . .
-0.00122	1000 0000 0000
+0.00122	1000 0000 0001
. . .	. . .
+4.99389	1111 1111 1110
+4.99634	1111 1111 1111

External Reference Circuit

Figure 18 shows how to a MX584LH to generate a reference voltage of 5.00V. A typical adjustment range of 75mV is provided by R2. Over the commercial temperature range, the MX584LH contributes no more than ±1LSB of gain error.

During a conversion, transient currents flow at the REFIN input. To prevent dynamic errors, place either a 10µF electrolytic or tantalum smoothing capacitor in parallel with a 0.01µF disc ceramic from the REFIN pin to AGND.

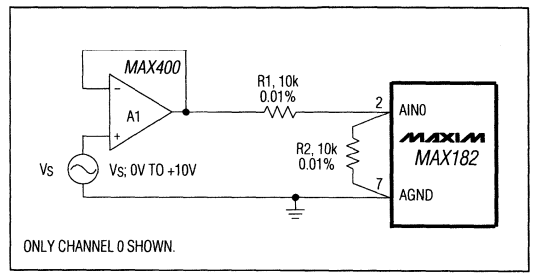


Figure 13. Unipolar 0V to +10V Operation

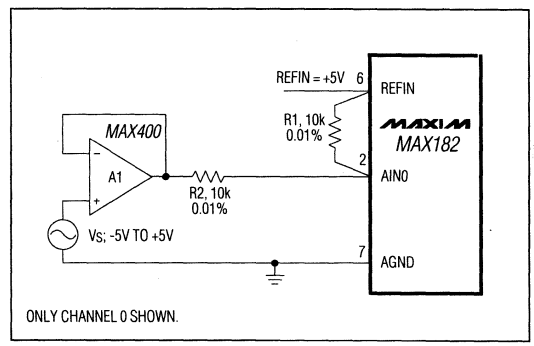


Figure 14. Bipolar -5V to +5V Operation

7

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Layout

When designing a layout for a printed circuit board, keep digital and analog signal lines separated whenever possible. It is critical that no digital line runs alongside an analog signal line or near the CAZ. Guard the analog inputs, the reference input and the CAZ input with AGND.

Establish a single-point analog ground (AGND) as close to the MAX182 as possible, isolated from the logic system. Connect the single-point analog ground to the digital system ground, which is attached to DGND at one point, as close as possible to the MAX182. The following should be returned to the analog ground point: input-signal common, input guards, the CAZ, and any bypass capacitors for the reference input and the analog supplies. Low-impedance analog and digital power-supply common returns with wide trace widths are essential for quiet operation of the MAX182.

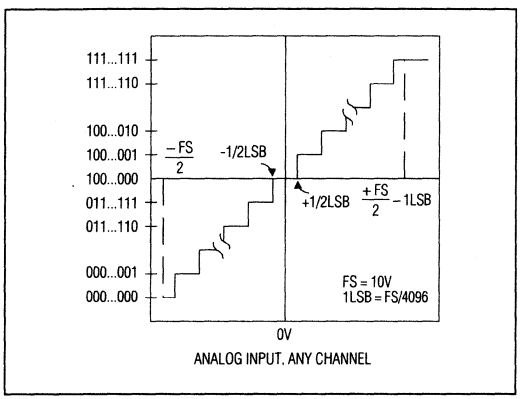


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

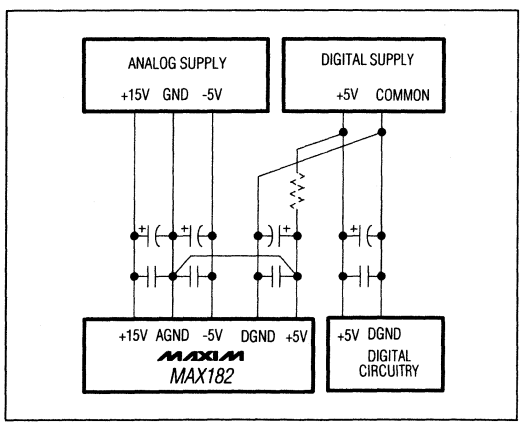


Figure 16. Power-Supply Grounding

Noise

To minimize input noise coupling, input signal leads to AIN and signal return leads from AGND should be kept as short as possible. A shielded cable between source and ADC is suggested in applications where longer leads are required. Also, care should be taken to reduce ground circuit impedances as much as possible since any potential difference in grounds between the signal source and ADC creates an error voltage in series with the input signal.

When interfacing to continuously busy and noisy µP buses, it is possible to get errors at the LSB level. These errors exist because of feedthrough from the bus to the integrated circuit through the package. The problem can be minimized in ceramic packaged chips by grounding the metal lid. Another solution is to isolate the MAX182 from the noisy µP bus using three-state buffers.

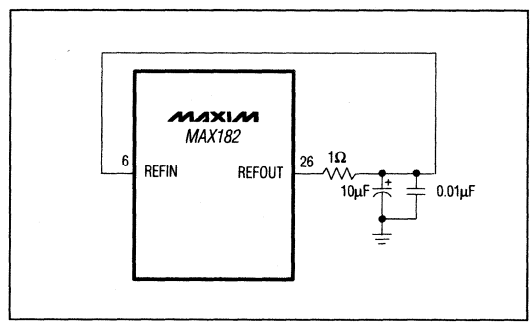


Figure 17. Internal Reference Hookup.

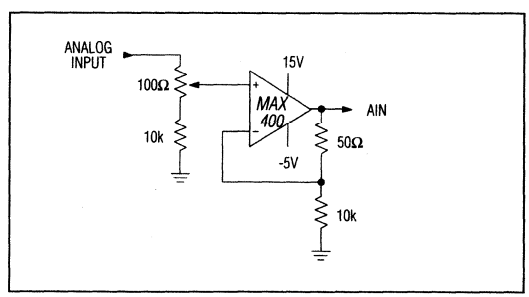


Figure 18. Adjusting Analog Input Gain to Trim Out Initial Reference Voltage Error

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Dynamic Performance

High-speed sampling capability and 14kHz throughput make the MAX182 ideal for wideband signal processing. To support these and other related applications, fast fourier transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity and differential non-linearity. Such parameters are widely accepted for specifying performance with DC and slowly varing signals but are less useful in signal-processing appications where the ADCs impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the signal-to-noise ratio (SNR). The output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as "signal-to-noise + distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can do no better than 74dB. Figure 20 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX182. An FFT plot of the output shows the output level in various spectral bands.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "effective number of bits" that the A/D provides: N = (SNR -1.76)/6.02.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is total harmonic distortion (THD). This is expressed as:

$$THD = 20Log[\sqrt{(V_2^2 + V_3^3 + V_4^2 + V_4^2 + \ldots + V_N^2)}/V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the peak harmonic or spurious noise. Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

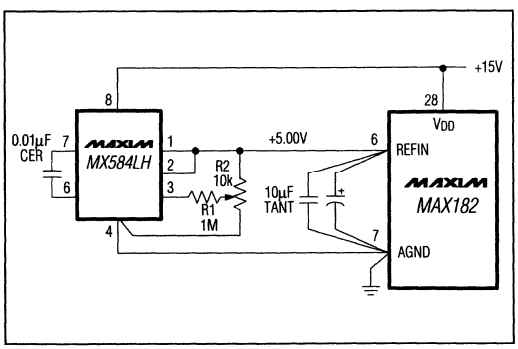


Figure 19. MX584LH as Reference Generator

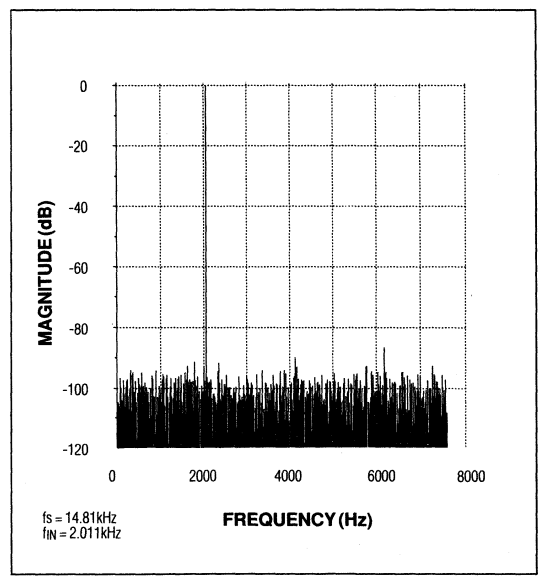
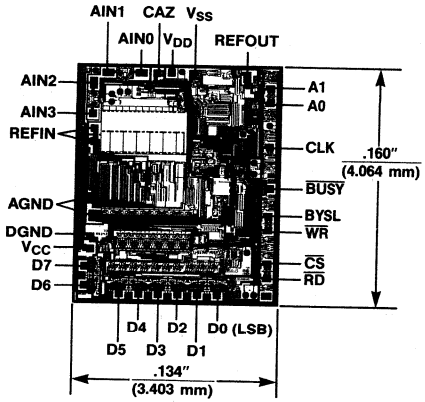


Figure 20. FFT Plot for the MAX182

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Chip Topography



MAX182

* Substrate internally connected to V_{DD}.

19-3127; Rev.0; 4/91

MAXIM

High-Speed 12-Bit A/D Converters With External Reference Input

General Description

The MAX183/184/185 are 12-bit, high-speed, BiCMOS, analog-to-digital converters (ADCs) that consume only 90mW of power while performing conversions in as little as 3µs. All three ADCs perform identically, except for conversion time: MAX183 - 3µs, MAX184 - 5µs, MAX185 - 10µs.

The MAX183/184/185 require an external -5V reference. A buffered reference input minimizes reference-current requirements and allows a single reference to drive several ADCs. External reference specs can be chosen to suit the accuracy of the application. The ADC clock can be driven from either a crystal or an external clock source, such as a microprocessor (µP) clock.

Analog input range is pin-selectable for 0 to +5V, 0 to +10V, or ±5V, making the ADCs ideal for data acquisition and analog input/output cards. A high-speed digital interface (100ns data access time) with three-state data outputs is compatible with most µPs.

The MAX183/184/185 are available in space-saving, 24-pin narrow plastic DIP, CERDIP, and wide SO packages.

Applications

Telecommunications

Sonar and Radar Signal Processing

High-Speed Data Acquisition Systems

Personal Computer I/O Boards

Features

- ♦ **12-Bit Resolution and Accuracy**
- ♦ **Fast Conversion Times:**
  MAX183 - 3µs
  MAX184 - 5µs
  MAX185 -10µs
- ♦ **Low 90mW Power Consumption**
- ♦ **Choice of +5V, +10V or ±5V Input Ranges**
- ♦ **Buffered Reference Input**
- ♦ **Fast 100ns Bus Access Time**
- ♦ **Operate with +5V, and -12V to -15V Supplies**
- ♦ **Available in 0.3" DIP or Wide SO Packages**

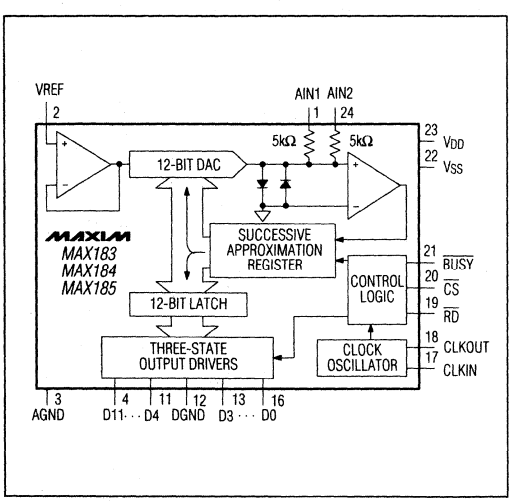
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
3µs Maximum Conversion Time			
MAX183ACNG	0°C to +70°C	24 Plastic DIP	±1/2
MAX183BCNG	0°C to +70°C	24 Plastic DIP	±1
MAX183ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX183BCWG	0°C to +70°C	24 Wide SO	±1
MAX183BC/D	0°C to +70°C	Dice*	±1

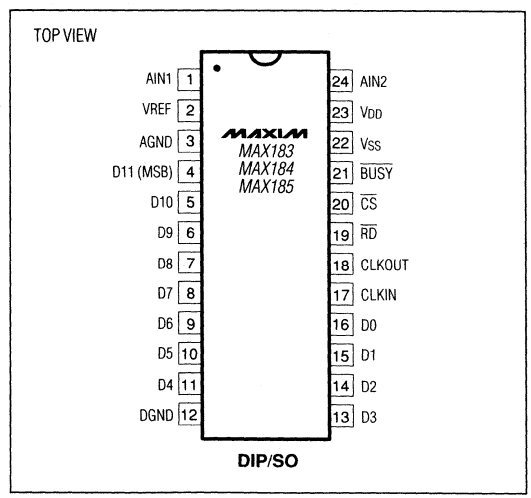
Ordering information continued on last page.

**Consult factory for dice specifications.*

Functional Diagram



Pin Configuration



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High-Speed 12-Bit A/D Converters With External Reference Input

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD}+0.3V
AIN1, AIN2 to AGND ..... -15V to +15V
VREF to AGND ..... V_{SS}-0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND
(CLKIN, $\overline{CS}$, $\overline{RD}$) ..... -0.3V to V_{DD}+0.3V
Digital Output Voltage to DGND
(D11-D0, $\overline{BUSY}$, CLKOUT) ..... -0.3V to V_{DD}+0.3V

Power Dissipation to +75°C (any package) 1000mW
Derate above +75°C by ..... 10mW/°C
Operating Temperature Ranges:
MAX18_AC/BC ..... 0°C to +70°C
MAX18_AE/BE ..... -40°C to +85°C
MAX18_AM/BM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -10.8V to -16.5V; VREF = -5V; Slow Memory Mode; f_{CLK} = 4MHz for MAX183, f_{CLK} = 2.5MHz for MAX184, f_{CLK} = 1.25MHz for MAX185; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 2)							
Resolution	N			12			Bits
Integral Nonlinearity	INL	Tested range ±5V	MAX18_AC/AE			±1/2	LSB
			MAX18_AM T_A = +25°C			±1/2	
			MAX18_AM			±3/4	
			MAX18_B			±1	
Differential Nonlinearity	DNL	12-Bits, no missing codes over temp.				±0.9	LSB
Unipolar/Bipolar Offset Error			T_A = +25°C			±3	LSB
			T_A = T_{MIN} to T_{MAX}			±4	
					±2		ppm/°C
Unipolar/Bipolar Gain Error			T_A = +25°C			±4	LSB
			T_A = T_{MIN} to T_{MAX}			±6	
					±2		ppm/°C
Conversion Time	t_{CONV}	Synchronous Clk (12.5 Clks)	MAX183			3.125	µs
			MAX184			5	
			MAX185			10	
		Asynchronous Clk (12 to 13 Clks)	MAX183	3.0		3.25	
			MAX184	4.8		5.2	
			MAX185	9.6		10.4	
ANALOG AND REFERENCE INPUTS							
Analog Input Current, AIN1 or AIN2		Unipolar input ranges 0V to +5V, 0V to +10V				3.5	mA
		Bipolar range ±5V				±1.75	
VREF Input Range (Note 3)				-5.1		-4.9	V
VREF Input Current						±3	µA
LOGIC INPUTS							
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, CLKIN				0.8	V
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, CLKIN		2.4			V
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$; V_{IN} = 0 to V_{DD}				±10	µA
		CLKIN; V_{IN} = 0 to V_{DD}				±20	
Input Capacitance (Note 3)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -10.8V to -16.5V; VREF = -5V; Slow Memory Mode; f_{CLK} = 4MHz for MAX183, f_{CLK} = 2.5MHz for MAX184, f_{CLK} = 1.25MHz for MAX185; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0, $\overline{BUSY}$, CLK OUT; I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0, $\overline{BUSY}$, CLK OUT; I_{SOURCE} = 200µA	4.0			V
Floating State Leakage Current	I_{LKG}	D11-D0; V_{OUT} = 0V to V_{DD}			±10	µA
Floating State Output Capacitance (Note 3)	C_{OUT}				15	pF
POWER REQUIREMENTS						
Supply Voltage (Note 1)	V_{DD}		4.75	5	5.25	V
	V_{SS}		-16.5	-12	-10.8	
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V $\overline{BUSY}$ = HIGH			7	mA
	I_{SS}				10	
Power Dissipation	PD	V_{DD} = +5V, V_{SS} = -12V		90	155	mW
Power-Supply Rejection, V_{DD} Only		FS Change, V_{SS} = -12V, V_{DD} = 4.75V to 5.25V		±1/4	±1	LSB
Power-Supply Rejection, V_{SS} Only		FS Change, V_{DD} = +5V, V_{SS} = -10.8V to -16.5V		±1/2	±1	LSB

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -10.8V to -16.5V; 100% production tested, T_A = T_{MIN} to T_{MAX}, unless otherwise indicated.) (Note 4, Figures 7, 9, 10)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX18_C/E			MAX18_M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time (Note 3)	t1		0			0			0			ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t2	CL = 50pF		70	120			150			180	ns
Data Access Time (Note 5)	t3	CL = 100pF		50	100			130			150	ns
$\overline{RD}$ Pulse Width (Note 3)	t4		t3			t3			t3			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 3)	t5		0			0			0			ns
Data Setup Time After $\overline{BUSY}$ (Note 5)	t6	CL = 100pF		40	70			90			100	ns
Bus Relinquish Time (Note 6)	t7			30	60			75			90	ns
Delay Between Read Operations	t8		200			200			200			ns
CLKIN to $\overline{BUSY}$ Delay (Note 3)	t9				120			150			180	ns
$\overline{RD}$ to CLKIN Setup/Hold Time (Notes 3, 7)	t10		25		100	25		100	25		100	ns

Note 1: Performance guaranteed over supply range by testing end-point errors (power-supply rejection) at the supply extremes.
Note 2: V_{DD} = +5V, V_{SS} = -12V, V_{REF} = -5V
Note 3: Guaranteed by design.
Note 4: All inputs are 0V to +5V swing with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 5: t3 and t6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross +0.8V or +2.4V.
Note 6: t7 is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 2.
Note 7: For predictable conversion times, $\overline{RD}$ to CLKIN falling edge must be outside this window.

High-Speed 12-Bit A/D Converters With External Reference Input

Pin Description

PIN	NAME	FUNCTION
1	AIN1	Analog Input
2	VREF	Voltage-Reference Input
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs. They are active when $\overline{CS}$ and $\overline{RD}$ are low. DB11 is the most significant bit.
12	DGND	Digital Ground
13-16	D3-D0	Three-State Data Outputs
17	CLKIN	Clock Input. Connect an external TTL-compatible clock to CLKIN. Alternatively, insert a crystal or ceramic resonator between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. When using an external clock, an inverted CLKIN signal appears on CLKOUT. See CLKIN description.
19	$\overline{RD}$	$\overline{READ}$ Input. Along with $\overline{CS}$, this active low signal enables the three-state drivers and starts a conversion.
20	$\overline{CS}$	$\overline{CHIP\ SELECT}$. Along with $\overline{RD}$, this active low signal enables the three-state drivers and starts a conversion.
21	$\overline{BUSY}$	$\overline{BUSY}$. Low while a conversion is in progress. $\overline{BUSY}$ indicates converter status.
22	V_{SS}	Negative Supply, -12V to -15V
23	V_{DD}	Positive Supply, +5V
24	AIN2	Analog Input

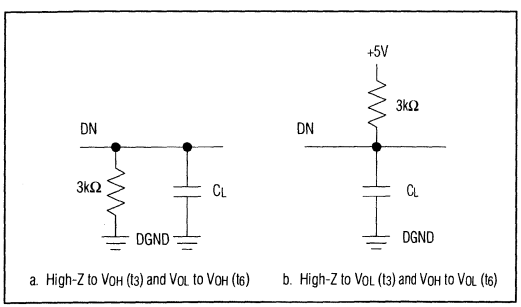

Figure 1. Load Circuits for Access Time

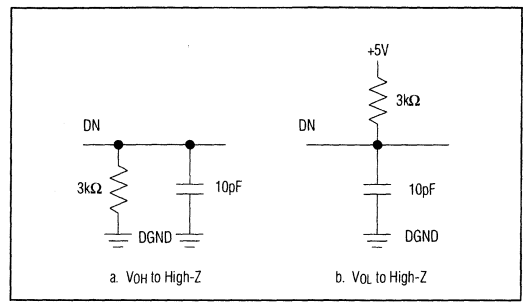

Figure 2. Load Circuits for Bus-Relinquish Time

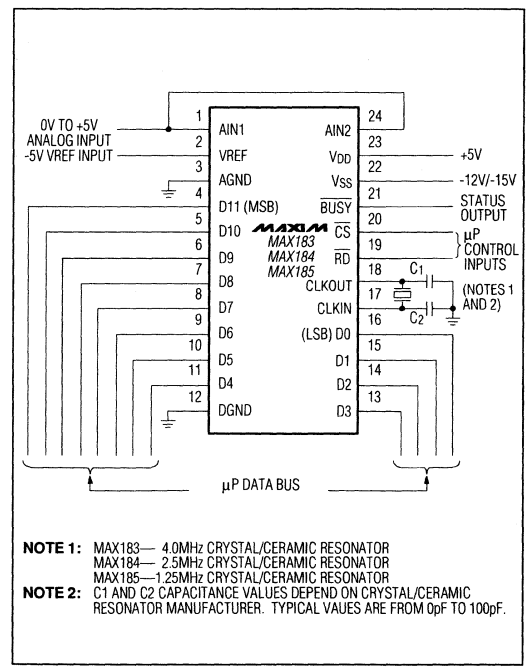

Figure 3. MAX183/184/185 Operational Diagram

High-Speed 12-Bit A/D Converters With External Reference Input

Detailed Description

Converter Operation

The MAX183/184/185 use a successive approximation technique to convert an analog input to a 12-bit digital output code. The control logic provides easy interface to most µPs (Figure 3).

Figure 4 shows the MAX183/184/185 analog-equivalent circuit. The internal D/A converter (DAC) is controlled by a successive approximation register (SAR), has an output impedance of 2.5kΩ, and connects directly to the comparator input. The analog inputs AIN1 and AIN2 connect to the same comparator input through 5kΩ resistors.

A conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ and cannot be restarted after initiation. The $\overline{BUSY}$ output goes low when the conversion starts and can be used to control an external sample-and-hold when measuring wide bandwidth input signals.

The SAR is set, asynchronously with the clock input, to half scale when $\overline{CS}$ and $\overline{RD}$ go low. At the second falling edge of CLKIN (or rising edge of CLKOUT) following a conversion start, the output of the comparator is latched into the SAR most significant bit (MSB/D11) (Figure 5). The MSB is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (D10) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. At conversion end, following a falling CLKIN signal, $\overline{BUSY}$ goes high and the SAR result is latched into three-state output buffers.

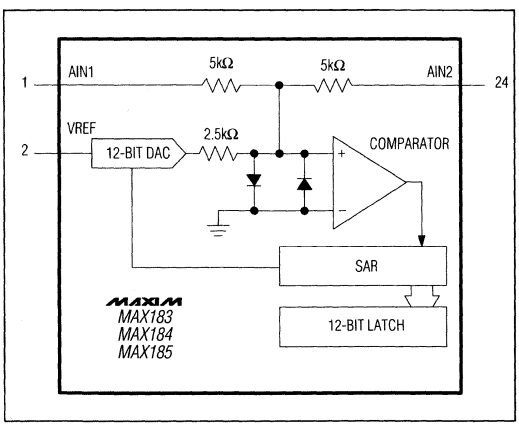

Figure 4. MAX183/184/185 AIN Inputs

Clock

Internal Clock Oscillator

Figure 6 shows the MAX183/184/185 clock circuitry. Minimize the capacitive load on the CLKOUT pin for low power dissipation and to avoid digital coupling of the CLKOUT buffer current to the comparator. CLKOUT should be left open if an external clock source is used to drive CLKIN. Connect a crystal/ceramic resonator between CLKOUT and CLKIN if the internal oscillator is used.

Control Inputs Synchronization

When $\overline{RD}$ is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). Use the following guidelines to ensure a fixed conversion time:

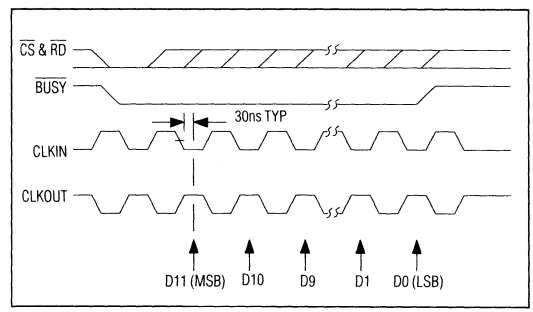

Figure 5. Operating Waveforms Using an External Clock Source for CLKIN

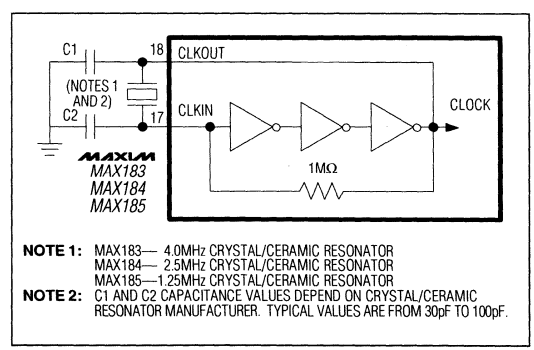

Figure 6. MAX183/184/185 Internal Clock Circuit

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High-Speed 12-Bit A/D Converters With External Reference Input

The MAX183/184/185 $\overline{RD}$ input should go low at the rising edge of CLKIN. In this case, the conversion lasts 12.5 clock cycles, and the conversion time is 3.125µs when f_{CLK} = 4MHz, 5µs when f_{CLK} = 2.5MHz, and 10µs when f_{CLK} = 1.25MHz. The delay from the falling edge of $\overline{RD}$ to the falling edge of CLKIN must not be less than 100ns to ensure the 12.5 clock cycle conversion time (Figure 7). This gives the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional 1/2 clock cycle of settling can be allowed for the sample-and-hold by having $\overline{RD}$ go low at the falling edge of CLKIN. This results in a 13 cycle conversion time (3.25µs, 5.2µs and 10.4µs).

Digital Interface

Timing and Control

$\overline{CS}$ and $\overline{RD}$ control conversion start and data-read operations. Figure 8 shows the logic equivalent for the conversion and the data-output control circuitry. A logic low at both inputs starts a conversion. Once a conversion is in progress, it cannot be restarted. The $\overline{BUSY}$ output remains low during the entire conversion cycle.

Figures 9 and 10 outline the two interface modes (slow memory and ROM). Slow memory mode is for µPs that can be forced into a wait state for periods as long as the MAX183/184/185 conversion time. ROM mode is for µPs that cannot be forced into a wait state. In both interface modes, a processor read operation to the ADC address starts the conversion. In the ROM mode, a second read operation accesses the conversion result.

Slow Memory Mode

The timing diagram in Figure 9 illustrates slow memory mode, which is designed for µPs with a wait state. $\overline{CS}$ and $\overline{RD}$ go low, triggering a conversion, and are kept low until the conversion is complete. $\overline{BUSY}$ responds by going low, and data from the previous conversion remains on the three-state data outputs. At conversion end, $\overline{BUSY}$ returns high, and the output latches transfer the new conversion results to the three-state data outputs. The µP completes the read operation by taking $\overline{CS}$ and $\overline{RD}$ high.

ROM Mode

The ROM mode avoids placing the µP into a wait state. A conversion begins with a read operation. While $\overline{CS}$ and $\overline{RD}$ are low, data from the last conversion is available on the data outputs. A second read operation reads the new data and begins the conversion process again. A delay at least as long as the MAX183/184/185 conversion times must be allowed between read operations. The data on the output bus is in a parallel format in either mode.

Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, coupling from the data pins to the ADC comparator may cause LSBs of error. Using slow memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, use three-state drivers to isolate the bus from the ADC.

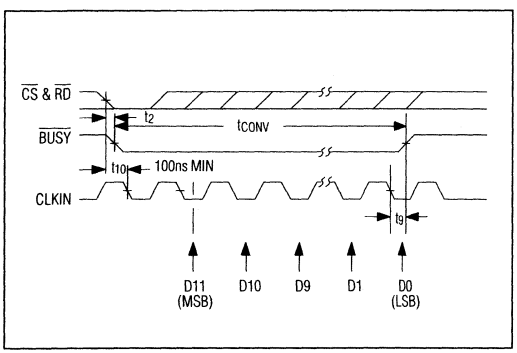


Figure 7. MAX183/184/185 $\overline{RD}$ and CLKIN for Synchronous Operation and Conversion Time of 12.5 Clock Cycles

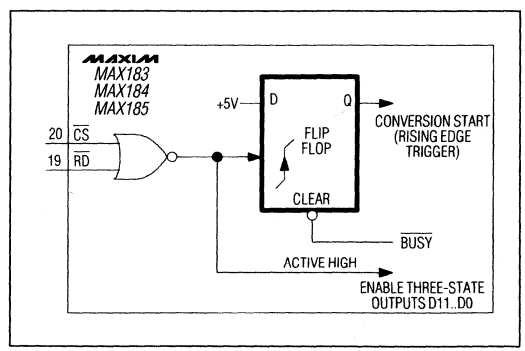


Figure 8. Logic for Control Inputs $\overline{CS}$ and $\overline{RD}$ Internal

High-Speed 12-Bit A/D Converters With External Reference Input

ROM Mode

Digital noise is generated in the ADC when $\overline{RD}$ or $\overline{CS}$ go high, and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a bit decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than 1 clock cycle. In other words, the $\overline{RD}$ and $\overline{CS}$ low pulse should be less than 250ns for the MAX183, 400ns for the MAX184, and 1µs for the MAX185. If this cannot be done, the $\overline{RD}$ or $\overline{CS}$ signal must go high at a rising edge of CLKIN since the comparator output is always latched at falling edges of CLKIN.

Physical Layout

For best system performance, printed circuit boards should be used for the MAX183/184/185; wire-wrap boards are not recommended. Separate the digital- and analog-signal lines as much as possible in the board layout. Do not run analog and digital lines parallel to each other or digital lines underneath the MAX183/184/185 package.

Grounding

Figure 11 shows the recommended system ground connections. Establish a single-point analog ground (star ground), separate from the logic ground, at AGND of the MAX183/184/185. Connect all other analog grounds and DGND of the MAX183/184/185 to this star ground (no other digital grounds should be connected to this point). For noise-free operation of the ADC, use a low-impedance ground return to the power supply from this star ground.

Power-Supply Bypassing

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog star ground with 0.1µF and 10µF bypass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10Ω-20Ω) resistor can be connected (Figure 11) to filter external noise.

Driving The Analog Input

The input signal leads to AIN and the input return leads to AGND should be as short as possible to minimize input noise coupling. Use shielded cables if the leads must be long.

The input impedance at each AIN is typically 5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is needed since the analog input current is modulated at the clock rate during a conversion (up to 4MHz for MAX183, 2.5MHz for MAX184, or 1.25MHz for the MAX185). The output impedance of the driving amplifier is equal to its open-loop output impedance divided by the loop gain at the frequency of interest.

MAX184/185 – The MAX184/185 maximum clock rate of 2.5MHz makes it possible to drive AIN with amplifiers like the OP42, AD711 or a Maxim OP27. A MAX400 or a Maxim OP07 can also be used up to 1.25MHz clock rate.

MAX183 – The MAX183, with a maximum 4MHz clock rate, might exhibit settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a Maxim OP27, an OP42, or an AD711 improves high-frequency output impedance.

Reference Input

VREF connects to an external -5V source. This may be either a precision negative reference, a positive reference (such as the MX584) connected as a two-terminal device to provide -5V (Figure 16), or an existing system reference. The allowed input range at REFIN is -5.1V to -4.9V. VREF (and AIN2 in bipolar input operation) should be bypassed to ground with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

If the external reference is biased from a power supply other than V_{SS}, then care must be taken to ensure that V_{SS} is applied to the ADC before VREF. If supply sequencing is in doubt, then connect a diode between V_{SS} and VREF, as shown in Figure 12. If the reference source is powered from the same supply as V_{SS}, then no diode is needed.

MAX183/184/185 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input-signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX183. A sample-and-hold should be used for higher bandwidth signals.

The $\overline{BUSY}$ output from the MAX183/184/185 may be used to provide the TRACK/$\overline{HOLD}$ signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the $\overline{BUSY}$ signal goes low, sample-and-hold transients caused by DAC switching may result in code-dependent errors due to sample-and-hold aperture delay. Adding a NAND (inverted AND) gate ensures that the sample-and-hold is switched to the hold mode BEFORE any disturbances (Figures 13 and 14). The NAND gate solution works only if the width of the $\overline{RD}$ pulse is wider than the $\overline{RD}$ to $\overline{BUSY}$ delay in the MAX183/184/185. If this is not the case, use a flip-flop, which is set by the falling edge of $\overline{RD}$ and reset by the rising edge of $\overline{BUSY}$.

High-Speed 12-Bit A/D Converters With External Reference Input

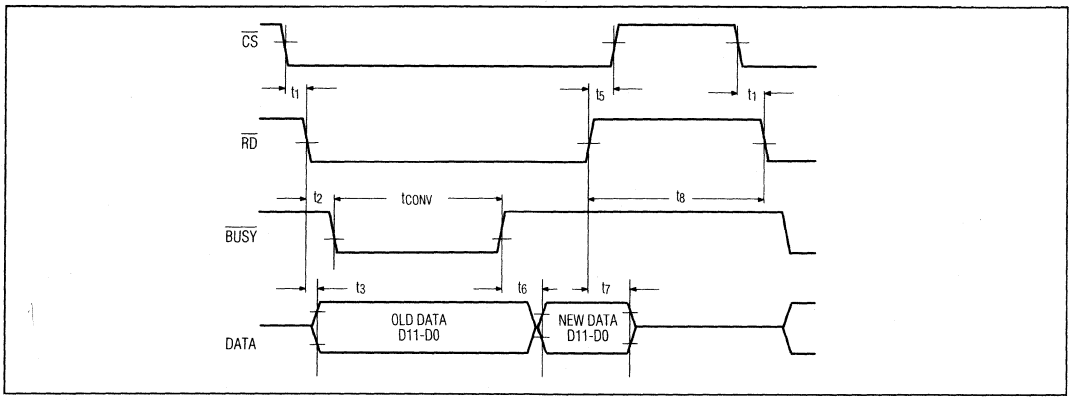


Figure 9. Slow Memory Mode Timing Diagram

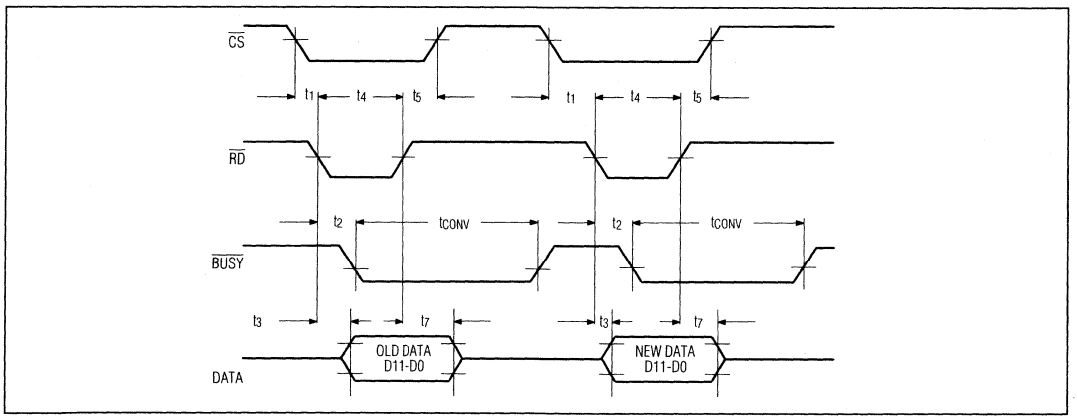


Figure 10. ROM Mode Timing Diagram

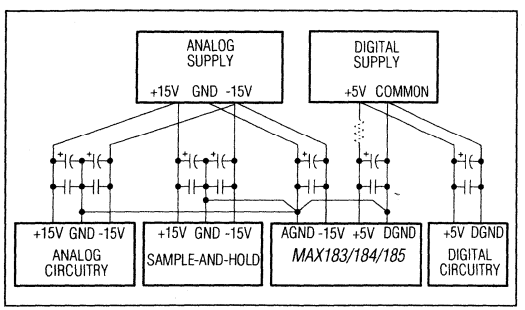


Figure 11. Power-Supply Grounding Practice

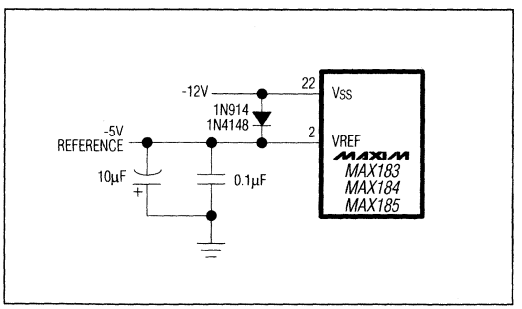


Figure 12. VREF/VSS Diode Clamp (See "Reference Input" Text).

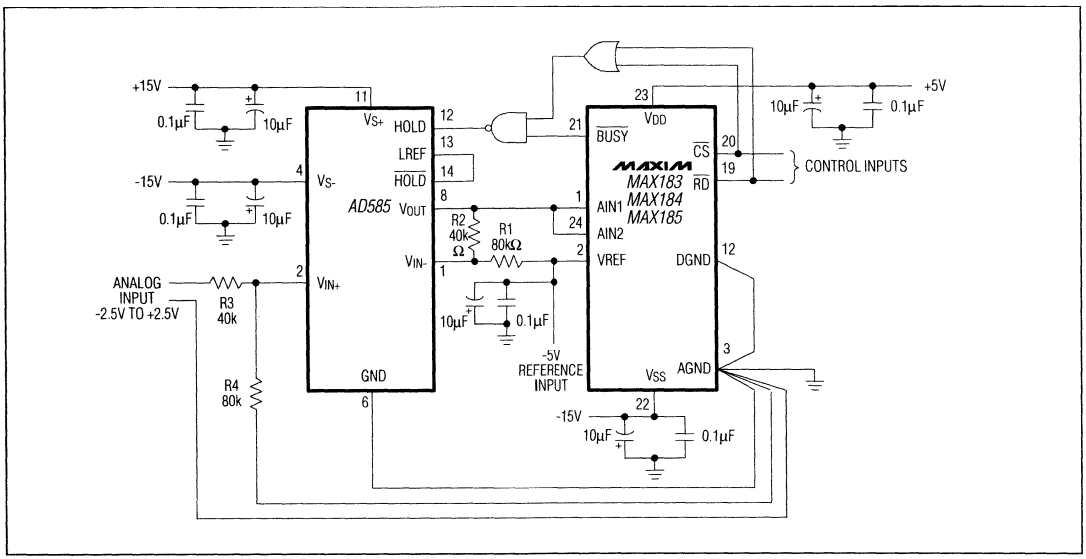


Figure 13. MAX183/184/185—AD585 Sample-and-Hold Interface

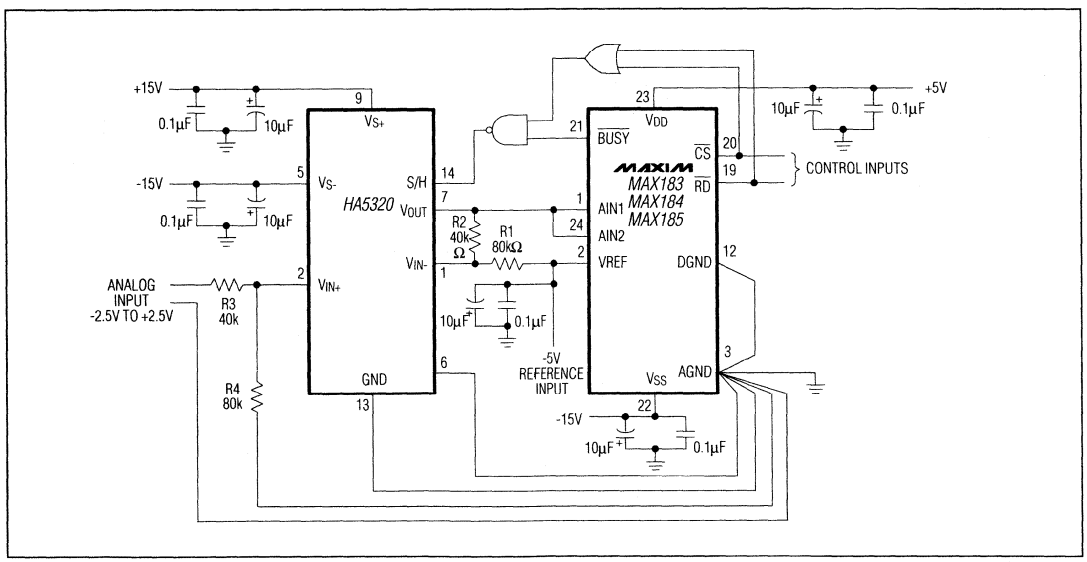


Figure 14. MAX183/184/185—HA5320 Sample-and-Hold Interface

High-Speed 12-Bit A/D Converters With External Reference Input

For synchronous $\overline{RD}$ and CLKIN, the hold settling time allowed for the sample-and-hold is 375ns (MAX183), 600ns (MAX184), and 1.5µs (MAX185).

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock, allowing for a 3µs sample-and-hold acquisition time.

Although this circuit works well for the 1MHz clock rate, a faster sample-and-hold amplifier, such as the HA5320, is recommended at a 2.5MHz clock rate.

MAX183 – Figure 14 is the MAX183 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock, which allows a 1.5µs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Analog Input Ranges

The MAX183/184/185 provides three selectable analog input ranges: 0V to +5V, 0V to +10V, and ±5V. Figure 15 shows the configuration for the two analog inputs (AIN1 and AIN2) for these ranges.

Unipolar Operation

Figure 16 shows unipolar operation using a MX584 voltage reference configured for -5V.

Figure 17 shows the nominal input/output transfer function of the MAX183/184/185. Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = Full Scale (FS)/4096. FS is either +5V or +10V, based on the analog input configurations.

Offset and Full-Scale Adjustment

In applications requiring offset and FS range adjustment, use the circuit in Figure 19. Note: The amplifier shown could also be a sample-and-hold. Offset should be adjusted first. Apply 1/2LSB (0.61mV) at the analog input (AIN1 or AIN2) and adjust the offset of the amplifier until

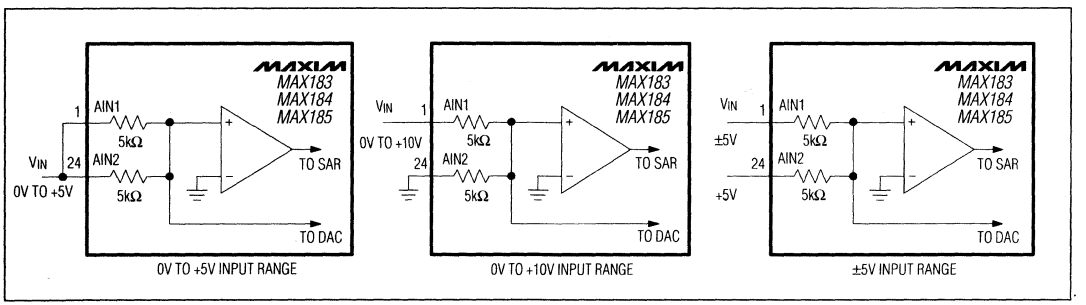


Figure 15. Analog Input Range Configurations

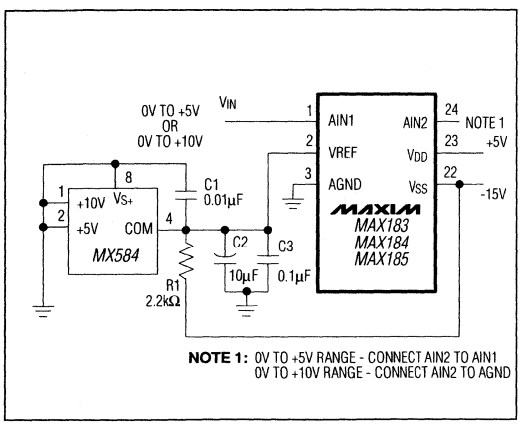


Figure 16. Unipolar Operation Using a MX584 Reference

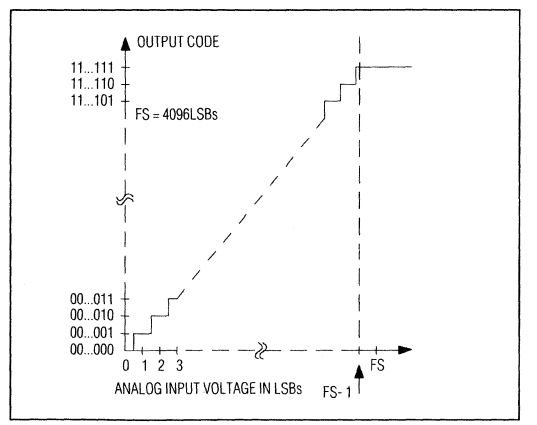


Figure 17. MAX183/184/185 Ideal Unipolar Transfer Function

the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

0V to +5V range: 1/2LSB = 0.61mV
0V to +10V range: 1/2LSB = 1.22mV

To adjust the full-scale range, apply FS-3/2LSB (last code transition) at the analog input and adjust R1 until the output code switches between 1111 1111 1110 and 1111 1111 1111.

0V to +5V range: FS-3/2LSB = 4.99817V
0V to +10V range: FS-3/2LSB = 9.99634V

Bipolar Operation

The bipolar input range is ±5V. V_{IN} is applied to AIN1, +5V to AIN2, and -5V to VREF. This requires two reference voltages: -5V for the VREF input and +5V for the AIN2 input. Figure 19 shows these reference voltages are produced from a MAX675 reference and a MAX400 op amp configured as an inverting amplifier.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 20. The LSB is 2.44mV (10V/4096).

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full-scale adjustments must be made in bipolar circuits. If low tolerances are used, larger value potentiometers must be used, which results in poor trim resolution and higher temperature drift.

Offset and Gain Adjustment

In bipolar operation, the offset is trimmed at negative full scale and should always be adjusted first. For offset, apply -FS/2 + 1/2LSB (-4.99878V) at V_{IN} and adjust the 10kΩ potentiometer (Figure 18) until the output code switches between 0000 0000 0000 and 0000 0000 0001.

Gain is adjusted at full scale or bipolar zero. For full scale adjustment, apply FS/2 - 3/2LSBs (4.99634V) to V_{IN} and adjust the 200Ω potentiometer until the output code switches between 1111 1111 1110 and 1111 1111 1111.

Alternatively, to adjust gain at bipolar zero, apply -1.22mV at V_{IN} and adjust the 200Ω potentiometer until the output code switches between 0111 1111 1111 and 1000 0000 0000.

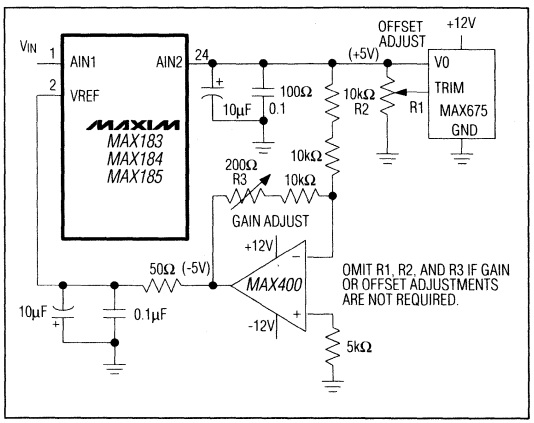


Figure 19. Bipolar Operation with Offset and Gain-Error Adjust

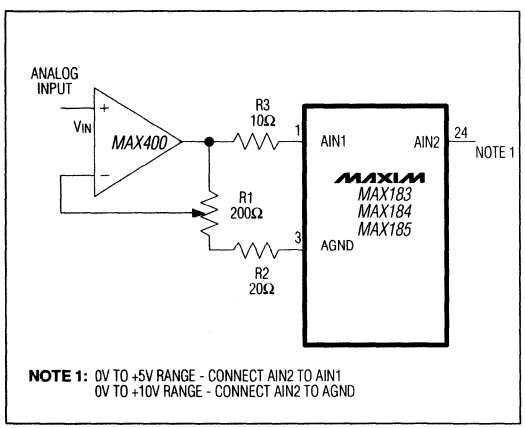


Figure 18. Unipolar Operation with Gain Adjust

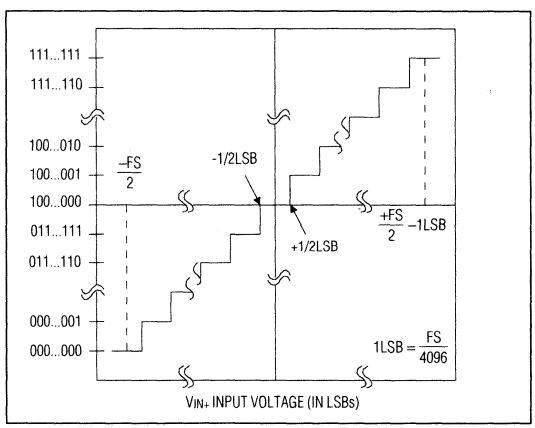


Figure 20. Ideal Input/Output Transfer Characteristic for Bipolar Operation

High-Speed 12-Bit A/D Converters With External Reference Input

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
MAX183AENG	-40°C to +85°C	24 Plastic DIP	±1/2
MAX183BENG	-40°C to +85°C	24 Plastic DIP	±1
MAX183AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX183BEWG	-40°C to +85°C	24 Wide SO	±1
5µs Maximum Conversion Time			
MAX184ACNG	0°C to +70°C	24 Plastic DIP	±1/2
MAX184BCNG	0°C to +70°C	24 Plastic DIP	±1
MAX184ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX184BCWG	0°C to +70°C	24 Wide SO	±1
MAX184BC/D	0°C to +70°C	Dice*	±1
MAX184AENG	-40°C to +85°C	24 Plastic DIP	±1/2
MAX184BENG	-40°C to +85°C	24 Plastic DIP	±1
MAX184AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX184BEWG	-40°C to +85°C	24 Wide SO	±1
MAX184AMRG	-55°C to +125°C	24 CERDIP**	±3/4
MAX184BMRG	-55°C to +125°C	24 CERDIP**	±1
10µs Maximum Conversion Time			
MAX185ACNG	0°C to +70°C	24 Plastic DIP	±1/2
MAX185BCNG	0°C to +70°C	24 Plastic DIP	±1
MAX185ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX185BCWG	0°C to +70°C	24 Wide SO	±1
MAX185BC/D	0°C to +70°C	Dice*	±1
MAX185AENG	-40°C to +85°C	24 Plastic DIP	±1/2
MAX185BENG	-40°C to +85°C	24 Plastic DIP	±1
MAX185AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX185BEWG	-40°C to +85°C	24 Wide SO	±1
MAX185AMRG	-55°C to +125°C	24 CERDIP**	±3/4
MAX185BMRG	-55°C to +125°C	24 CERDIP**	±1

** Consult factory for dice specifications.*

*** Contact factory for processing to MIL-STD-883.*

ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

Low Power Single-Supply 12-Bit Sampling ADC

General Description

The MAX190 is a complete monolithic CMOS 12-bit analog-to-digital converter (ADC) which features a differential input, track and hold (T/H), adjustable voltage reference, internal or external clock, and both parallel and serial µP interfaces. It has a conversion time of 12.5µs and tested sampling rate of 76kHz while requiring only 5mA from a single 5V supply. A 40µA power-down mode saves power in slow sampling rate applications.

No external components are needed other than decoupling capacitors for the power supply and reference. This ADC operates with an internal or external reference. The internal reference features an adjustment input for trimming system gain errors.

The MAX190 provides three interface modes. Two 8-bit parallel modes, and a serial interface mode that is compatible with common serial interface standards.

Applications

Battery-Powered Data Logging

High-Accuracy Process Control

Electro-Mechanical Systems

Data Acquisition Board for PCs

Automatic Testing Systems

Telecommunications

Digital-Signal Processing (DSP)

Features

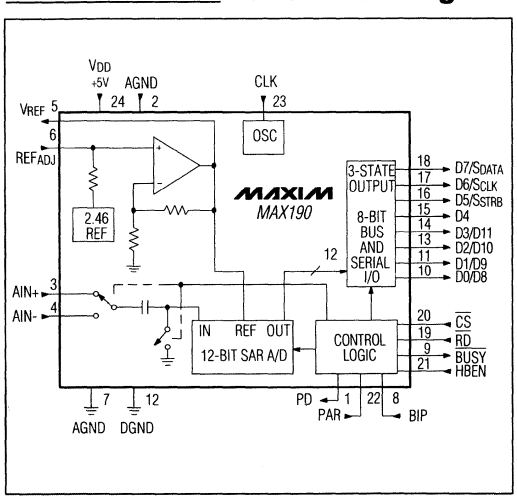
- **12-Bit Resolution, 1/2LSB Linearity**
- **Single +5V Operation 5mA max Current**
- **40µA Power-Down Mode**
- **Built-In Track-and-Hold**
- **12.5µs Conversion Time (Includes T/H Acquisition)**
- **Internal Reference with Adjustment Capability**
- **Serial and 8-Bit Parallel µP Interface**
- **24-Lead Narrow DIP and Wide SO Packages**

Ordering Information

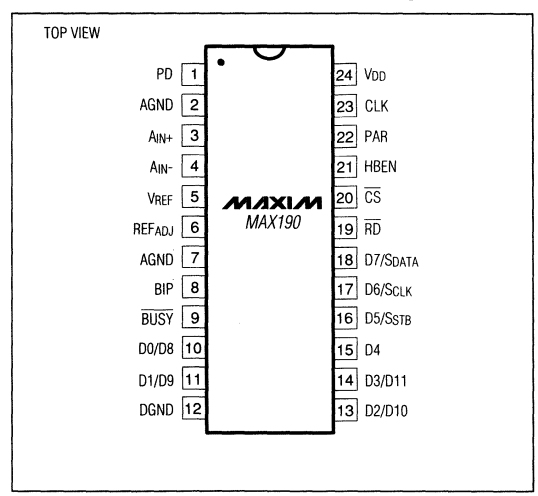
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX190ACNG	0°C to +70°C	24 Plastic DIP	±1/2
MAX190BCNG	0°C to +70°C	24 Plastic DIP	±1
MAX190ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX190BCWG	0°C to +70°C	24 Wide SO	±1
MAX190BC/D	-0°C to +70°C	24 Dice*	±1
MAX190AENG	-40°C to +85°C	24 Plastic DIP	±1/2
MAX190BENG*	-40°C to +85°C	24 Plastic DIP	±1
MAX190AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX190BEWG	-40°C to +85°C	24 Wide SO	±1
MAX190AMRG	-55°C to +125°C	24 CERDIP	±1/2
MAX190BMRG	-55°C to +125°C	24 CERDIP	±1

* *Contact factory for dice specifications.*

Functional Diagram



Pin Configuration



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ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

400ns µP-Compatible, 8-Bit ADC with Track/Hold

General Description

The MX7821 high-speed, microprocessor-compatible (µP), 8-bit A/D converter (ADC) is a pin-compatible upgrade to the industry-standard 7820. The MX7821 uses a half-flash technique, resulting in a 400ns conversion time vs. 1.36µs for the 7820. It has a 100kHz input-signal bandwidth vs. 6.4kHz for the 7820. A V_{SS} pin, not supplied by the 7820, supports dual power supplies and bipolar inputs.

The MX7821 has track-and-hold (T/H) functions capable of digitizing a 2MHz signal, and is static and dynamically tested. The converter-µP interface appears as a memory location or input/output (I/O) port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The MX7821 has an overflow output for cascading devices to attain higher resolution. The ADC's input/reference arrangement enables ratiometric operation.

Applications

Digital-Signal Processing

High-Speed Data Acquisition

Telecommunications

High-Speed Servo Loops

Audio Systems

Features

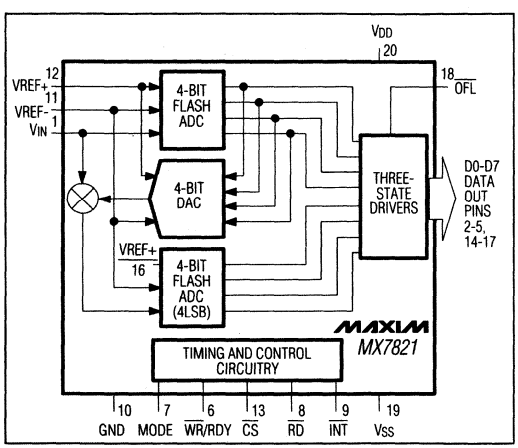
- ♦ **400ns Conversion Time**
- ♦ **20-Pin Narrow DIP Package**
- ♦ **No External Clock**
- ♦ **Pin-Compatible Upgrade for AD7820**
- ♦ **100kHz Input Signal Bandwidth**
- ♦ **Bipolar/Unipolar Inputs**
- ♦ **Single/Dual +5V Supplies**
- ♦ **Ratiometric Reference Inputs**
- ♦ **Static and Dynamically Tested**
- ♦ **Internal Track/Hold**

Ordering Information

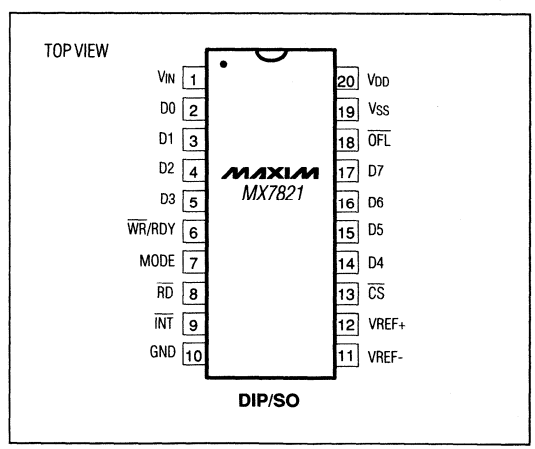
PART	TEMP. RANGE	PIN-PACKAGE
MX7821KN	0°C to +70°C	20 Plastic DIP
MX7821KCWP	0°C to +70°C	20 Wide SO
MX7821KP	0°C to +70°C	20 PLCC
MX7821KC/D	0°C to +70°C	Dice*
MX7821BQ	-40°C to +85°C	20 Plastic DIP
MX7821BEWP	-40°C to +85°C	20 Wide SO
MX7821TE	-55°C to +125°C	20 LCC**
MX7821TQ	-55°C to +125°C	20 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Functional Block Diagram



Pin Configurations



MAXIM

Video Products

VIDEO PRODUCTS ANALOG DESIGN GUIDE #8

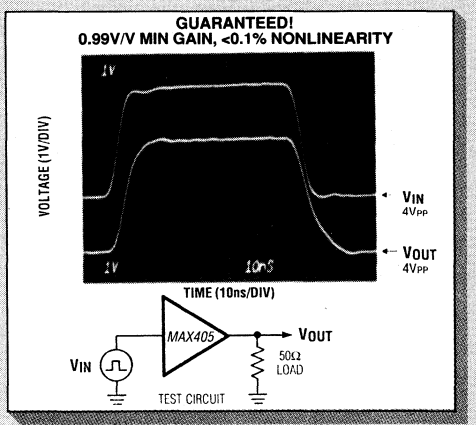
Data Sheets • Applications Notes • Free Samples

180MHz Video Buffer Guarantees 0.99V/V Gain Over Temperature

Truest Video Images: 0.01°/0.03% Differential Phase/Gain

The new MAX405 180MHz, precision buffer amplifier combines superior differential gain and phase with a 650V/µs slew rate while operating from ±5V supplies. Superior unadjusted DC gain is guaranteed to be greater than 0.99V/V over -40°C to +85°C with loads as low as 50Ω, a 7x improvement over the HA-5033 video buffer. The MAX405 comes in compact 8-pin DIP or SO packages and unlike existing buffers, access to the inverting input allows accurate gain adjustment from 0.99V/V to 1.1V/V which eliminates additional gain-adjusting components.

The MAX405, with a guaranteed 60mA continuous output current, directly drives three 50Ω loads to ±1V, or as many as four 150Ω loads (four 75Ω back-terminated loads) to ±2.25V. The MAX405's superior precision and speed make it the ideal choice as a 50Ω and 75Ω coaxial cable driver for NTSC, PAL and SECAM video signals.

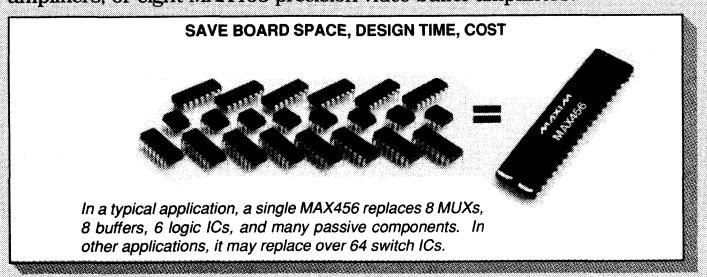


8x8 Video Crosspoint Switch Replaces 20 ICs

Digitally Controlled Matrix Connects Any Input to Any Output

The MAX456 is the **first** monolithic 8x8 video crosspoint switch that routes standard video signals (NTSC, PAL, SECAM). With a serial or parallel digitally controlled 8x8 switch matrix, control logic, and eight 35MHz, 250V/µs output buffer amplifiers, the MAX456 significantly reduces component count, board space and cost over discrete designs. In addition, a single package solution significantly reduces stray capacitance and increases the reliability over multi-chip alternatives. And with three-state outputs, multiple MAX456s can be paralleled to form larger switch networks without external buffering.

Each output buffer amplifier is capable of driving 400Ω and 20pF to ±1.3V. For applications that require 75Ω or 150Ω drive capability, the MAX456 outputs can be connected directly to four MAX457 (dual) 70MHz, unity gain stable video amplifiers, or eight MAX405 precision video buffer amplifiers.



In a typical application, a single MAX456 replaces 8 MUXs, 8 buffers, 6 logic ICs, and many passive components. In other applications, it may replace over 64 switch ICs.

8

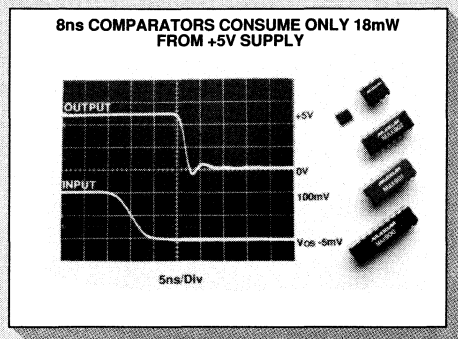
ANALOG DESIGN GUIDE

1	Multiplexers, Switches, Military
2	Interface Products
3	Op Amps
4	DC-DC Converters, Power Supplies
5	µP Supervisory
6	Analog Filters
7	A/D Converters
8	High Speed: Video, Comparators
9	D/A Converters

MAXIM

8ns, 18mW TTL Comparators Operate From a Single +5V Supply

First High-Speed Comparators With An Input Voltage Range That Extends to Ground



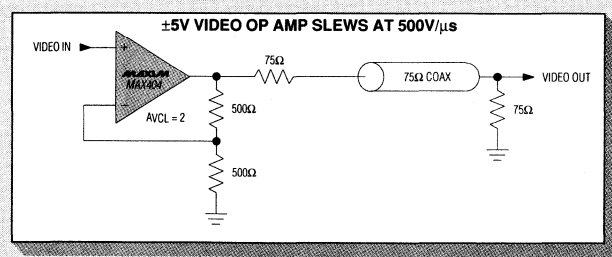
MAX900 series of high-speed, low-power comparators offer an 8ns response time while consuming only 18mW per comparator.

The MAX900/901/902/903 are the fastest low-power TTL compatible single, dual and quad high speed comparators with superior single supply performance. No other comparators offer the combination of an 8ns response time while drawing only 3.6mA (18mW) per comparator from a +5V supply. And since many low-power applications operate from a single supply, the MAX900-903's input voltage range (CMVR) extends all the way to ground to provide a wide common mode input voltage range without the need for a negative supply.

For noise sensitive applications, the MAX900-MAX903 can be powered from separate analog and digital supplies. The analog supply can range from 5V to 10V with the negative supply grounded, or from a dual ±5V supply.

80MHz Video Op Amp–0.01°/0.05% Diff Phase/Gain From ±5V Supplies

Stable While Driving Unlimited Capacitive Loads



Unlike current-feedback amplifiers, the MAX404 can be used in virtually all high-speed applications because of its fully differential input.

The MAX404 high-speed operational amplifier offers exceptional AC performance, output drive and stability while operating from ±5V power supplies. Optimized for video and other high-speed applications at a gain ≥ 2V/V, this op amp features a 500V/µs slew rate, an 80MHz gain-bandwidth, and superior differential phase and gain from ±5V supplies. The MAX404 is easy to use because it maintains stability while driving unlimited capacitive loads to make it less susceptible to oscillations typical in high-speed amplifier applications.

Unlike current-feedback amplifiers, the MAX404 can be used in virtually all high-speed op amp applications because it has a fully symmetrical differential input, a 70dB common-mode rejection ratio (CMRR), and a 66dB open-loop gain.

As a 75Ω back-terminated video coaxial cable driver (A_{VCL}=2, V_{OUT}=2V), full-power bandwidth is greater than 40MHz to ensure the NTSC, PAL, or SECAM video signal is well within the op amp's linear region. And with a guaranteed 50mA continuous output current, as many as three 150Ω loads can be driven to ±2.5V for video distribution applications. The MAX404 is available in an 8-pin DIP or SOIC package.

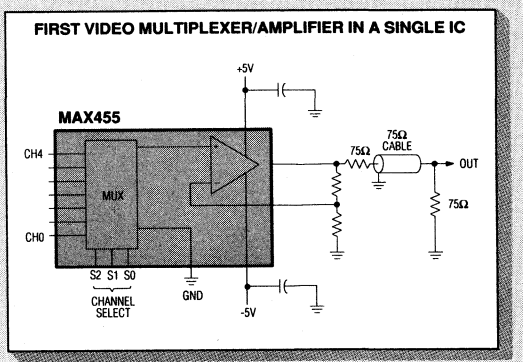
50MHz-8-Channel Video Mux/Amp Drives 75Ω Loads

First Video Mux/Amps Reduce Capacitance, Board Space and Cost

The MAX453/MAX454/MAX455 combine a video amplifier with a 2, 4, or 8-channel multiplexer in a single mini-DIP or SO package. The single IC solution dramatically reduces stray circuit capacitance, board space and cost over the discrete multiplexer and amplifier alternative.

Each mux/amp contains a 50MHz unity gain stable video amplifier that directly drives a 75Ω load or two 150Ω loads (75Ω back-terminated loads) to ±1V. The input of each mux/amp consists of a 2, 4 or 8-channel break-before-make multiplexer with an extremely low 7pF on-channel input capacitance and 70dB off isolation at 4MHz.

Typical applications include video signal multiplexing and video crosspoint switching for surveillance systems or consumer video systems.

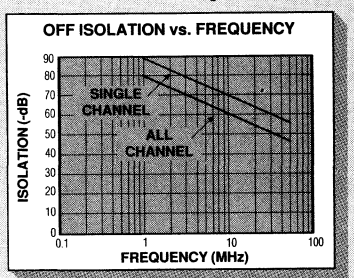


The MAX453/454/455 are 2-, 4-, and 8-channel multiplexers with an on-board 50MHz amplifier capable of driving 75Ω coaxial cable.

100MHz Video Multiplexers Offer 76dB Isolation

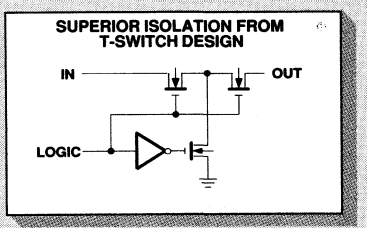
8-Channel Mux Operates from ±4.5V to ±18V Supplies

The MAX310 and MAX311 100MHz CMOS analog multiplexers have an enhanced series-shunt-series T structure to provide 76dB single channel "OFF" isolation at 5MHz, or when all channels are driven with the multiplexer disabled, isolation is 63dB at 5MHz.



The 100MHZ MAX310 and MAX311 offer the highest isolation of any CMOS video multiplexer.

The MAX310 is a single-ended eight-channel multiplexer and the MAX311 is designed as a four-channel differential multiplexer. Unlike other video multiplexers, these devices operate with standard supply voltages ranging from ±4.5V to ±18V. Break-before-make switching is guaranteed.



Superior isolation (76dB) is the result of this unique CMOS N-channel T-switch architecture.

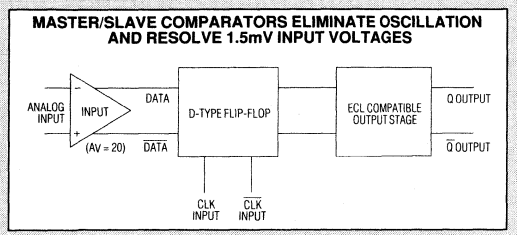
Applications include automatic test equipment, medical ultrasound phased array systems, data logging or any video multiplexing application.

8

ULTRA HIGH-SPEED ECL COMPARATORS ELIMINATE OSCILLATION

Unique Architecture Breaks the Input-to-Output Feedback Path

The MAX905 and MAX906 are the first ultra high-speed, precision, single and dual ECL comparators that eliminate oscillations caused by unwanted parasitic feedback. A master/slave, edge-triggered D-flip/flop architecture eliminates oscillations by breaking the feedback path between the input and the output of the comparator. And unlike other ECL comparators, this architecture makes it possible to resolve input voltages as small as 1.5mV. With a 2ns data-to-clock set-up time, input signals up to 500MHz may be distinguished without oscillation.



The MAX905/906 single and dual ECL comparators break the signal path between the input and output to eliminate oscillation due to parasitic feedback common in other high-speed comparators.

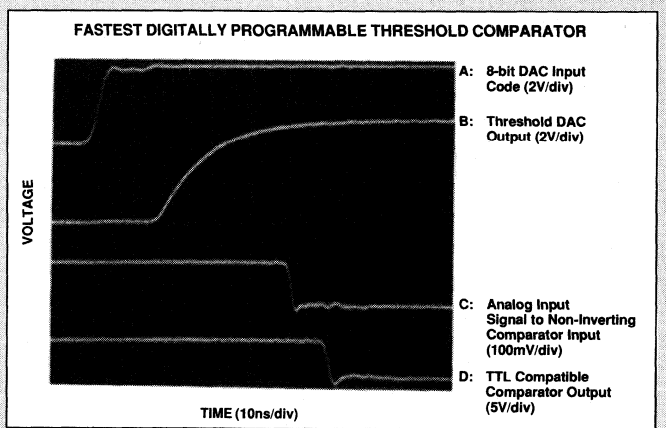
The MAX905/906 propagation delay is independent of input overdrive voltage. Whether the input overdrive is 5mV or 500mV, propagation delay is under 3ns.

The MAX905/906 have separate analog and digital supplies to isolate the noisy digital circuitry from the sensitive analog input section. The input common-mode voltage range extends all the way to the negative supply rail for a wide 7.9V input voltage range with ±5V supplies. The digital inputs and outputs are MECL 10K compatible.

8ns, PROGRAMMABLE THRESHOLD TTL COMPARATOR REPLACES 3 ICS

8-Bit Code Adjusts Input Threshold Voltage

The MAX910 is the first high-speed comparator to include an 8-bit DAC with voltage reference to set the input threshold voltage of the comparator. For high-speed comparator applications where the threshold voltage must be updated rapidly, such as automatic test equipment (ATE) or process control applications, the MAX910 provides a complete, single IC solution which significantly reduces stray capacitance, board space, design time, and cost. The comparator's 8-bit programmable input threshold voltage can be updated through its full-scale range in 50ns. Capable of recognizing input signals up to 100MHz, the MAX910 will respond to a change in the input within 8ns.



The MAX910's internal 8-bit DAC updates the input threshold voltage from -2.54V to +2.56V in 50ns. Comparator propagation delay is only 8ns.

For high-speed ECL systems, the MAX911 ECL-compatible comparator has a 2ns propagation delay with fully differential outputs.

Part Number	V_{OS} (mV) max	TCV_{OS} (µV/°C) max	I_{BIAS} (nA) max	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA) max	Features	Price† 1000-up ($)
MAX400	10 - 15µV	0.3	2	0.4	±3 to ±18	4	Ultra-low V_{OS} & drift non-chopper stabilized	5.16
MAX402	2	25	5	2	±5	75µA	High-speed, 7V/µs slew rate, micropower	1.98
MAX403	2	33	25	10	±5	375µA	High-speed, 40V/µs slew rate, micropower	2.75
MAX406	0.5 - 2.0	10	10pA	0.008-0.040	+2.5 to +10	1.2µA	Lowest-power, single supply, output swings rail-to-rail	2.54
MAX408/28/48	6 - 12	15 - 20	1.1µA	100 ($A_V \geq 3$)	±5	10/amp.	Single/dual/quad high-speed, high output current	3.02/4.06/6.74
MAX420/422	5 - 10µV	0.05	0.03 - 0.10	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 - 10µV	0.05	0.03 - 0.10	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/4.57
MAX425/426	5µV	0.05	10pA	0.35 - 12	±5	1.4	Lowest noise & drift, superior non-chopper error correction, no clock ripple noise	††
MAX430/432	5µV	0.05	0.1	0.125 - 0.5	±15	0.5 - 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX480	70µV	1.5	3	0.02	±0.8 to ±18 ±1.6 to ±36	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
ICL7611	2 - 15	10 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current	1.58
ICL7612	5 - 15	15 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current, CMVR > negative rail	1.81
ICL7614	2 - 15	15 - 25	0.05	0.48*	±1.0 to ±8	0.25	External compensation	0.95
ICL7616	2 - 15	15 - 25	0.05	0.044 - 1.4	±1.0 to ±8	0.02 - 2.5	Programmable quiescent current, CMVR > negative rail	1.62
ICL7621/7622	5 - 15	15 - 25	0.05	0.48	±1.0 to ±8	0.25	Dual low I_{BIAS} & I_{OS}	1.55/1.48
ICL7631/7632	5 - 20	15 - 30	0.05	0.044 - 1.4	±1.0 to ±8	0.022 - 2.5	Triple op amp, programmable quiescent current–ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 - 25	15 - 30	0.05	0.044 - 1.4	±1.0 to ±8	0.015 - 2.5	Quad op amp	1.70/1.91
ICL7650	5 - 10µV	0.05 - 0.10	0.01 - 0.02	2	±5	2	Industry-standard chopper stabilized	2.39
ICL7652	5 - 10µV	0.05	0.03	0.45	±5	2	Low noise industry-standard chopper stabilized	3.06

* External 39pF compensation capacitor added.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

Op Amps (continued)

Part Number	V_{OS} (μV)	TCV_{OS} (μV/°C) max	I_{BIAS} (nA) max	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA) max	Features	Price† 1000-up ($)
LT1001	15 - 60	0.6 - 1	2 - 4	0.8	±3 to ±18	2	Industry-standard precision	1.75
LT1028	40 - 80	0.8 - 1	90 - 180	75 ($A_V > 2$)	±4 to ±18	9.5 - 10.5	Lowest noise, high-speed	4.21
OP07	25 - 150	0.6 - 2.5	2 - 12	0.6	±3 to ±18	4	Industry-standard precision	0.97
OP27	25 - 100	0.6 - 1.8	40 - 80	8	±3 to ±18	4.6 - 5.6	Industry-standard low noise	††
OP37	25 - 100	0.6 - 1.8	40 - 80	63 ($A_V \geq 5$)	±3 to ±18	4.6 - 5.6	Industry-standard low noise	††
OP90	150 - 450	2 - 5	15 - 25	0.020	±0.8 to ±18 ±1.6 to ±36	15 - 20μA	Industry-standard micropower	1.65

High-Speed Comparators

Part Number	# Comps	Logic	Latched Outputs	Supply Current (mA) max	Tpd (ns) typ	Features	Price† 1000-up ($)
MAX900	4	TTL	YES	33	8.0	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, Internal pull-up resistors	7.01
MAX901	4	TTL	NO	33	8.0	MAX900 without output latch	5.98
MAX902	2	TTL	YES	17	8.0	Dual MAX900	††
MAX903	1	TTL	YES	8.5	8.0	Single MAX900	††
MAX905	1	ECL	YES	38	2.0	Edge Triggered Master/Slave architecture eliminates oscillations and resolves 1mV input voltages	††
MAX906	2	ECL	YES	38	2.0	Dual MAX905	††
MAX910	1	TTL	YES	60	5.0	High-speed TTL-compatible comparator with 8-bit digitally programmable input voltage threshold and on-board reference	††
MAX911	1	ECL	YES	62	2.0	MAX910 with differential ECL outputs	††
MAX9685	1	ECL	YES	54	1.3	Higher speed industry-standard	3.38
MAX9686	1	TTL	YES	45	6.0	Higher speed industry-standard	2.31
MAX9687	2	ECL	YES	114	1.4	Higher speed industry-standard	5.12

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Vos (mV) max	Output Current (mA) max	Supply Voltage (V)	IBIAS (nA) max	Features	Price† 1000-up ($)
VIDEO AMPLIFIERS								
MAX404	80 (Av ≥ 2)	500	8	50	±5	3µA	Broadcast quality video op amp 0.01°/0.05% diff phase/gain, symmetrical inputs, 70dB CMRR, 66dB AVOL	††
MAX408/28/48	100(Av ≥ 3)	90	6 - 12	50/amp	±5	1.1µA	Single, dual, quad op amps, high output drive	3.02/4.06/6.74
MAX452	50	300	5	14	±5	10	Unity gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	5	15	±5	1	Dual, unity gain stable, drives 75Ω coax cable	4.45
VIDEO BUFFERS								
MAX405	180	650	4	60	±5	2µA	Broadcast quality, 0.99V/V gain guaranteed over temp, 0.01°/0.03% diff phase/gain	4.25
MAX460	140	1500	5 - 10	100	±15	0.05 - 0.1	FET input, EL2005, LH0033 upgrade	19.78
LH0033	100	1400 - 1500	5 - 20	100	±15	0.1 - 0.5	FET input, improved industry-standard	13.67
LH0063/BB3553	300	2000	25 - 50	200	±15	0.2 - 0.5	FET input, industry-standard	23.51/24.99
VIDEO MULTIPLEXER/AMPLIFIER								
MAX453	50	300	5	14	±5	10	Video amplifier with 2-channel video mux	3.94
MAX454	50	300	5	14	±5	10	Video amplifier with 4-channel video mux	5.25
MAX455	50	300	5	14	±5	10	Video amplifier with 8-channel video mux	8.75

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Vos (mV) max	OFF Isolation (dB at 5MHz)	Crosstalk (dB at 5MHz)	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCH							
MAX456	35	250	5	80	70	8x8 crosspoint switch array with 8 output buffers, three-state capability	22.09

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future products – contact factory for pricing and availability.

APPLICATION NOTE

MAXIM

Designing With High-Speed, Low-Power Analog Integrated Circuits

The variety of high speed analog integrated circuits currently available is allowing circuit designers to incorporate increasingly complex functions into ever smaller packages. The growing complexity and decreasing size of these systems means that more high speed analog and digital signals must be routed at close proximity to each other on the circuit board. The potential for unwanted coupling between these signal paths increases as the distance between them decreases.

Optimize High Speed Performance With Careful Board Layout

In high frequency applications, ordinary circuit components such as conductors, resistors and capacitors, no longer behave as simple elements with no parasitic effects. Parallel circuit board traces and interconnecting cables become coupling capacitors, and the inductance of circuit board traces and component leads can no longer be neglected. Crosstalk, instability and decreased rise times of high speed signal edges are some of the problems that are caused by component parasitics.

Thoughtful integrated circuit design and pin assignment reduces the impact of component parasitics on system performance. For example, the MAX456 8 x 8 video crosspoint switch integrates 64 video switches, 8 output buffers and digital control logic into a 40 pin DIP or 44 pin PLCC package. Typical applications include microprocessor controlled video surveillance, medical imaging systems, or video editing systems.

The pin assignment of the MAX456 DIP and PLCC packages simplifies the task of printed circuit board layout. Examination of the pin configurations of this part, shown in Figure 1, reveals that no two input signals or output signals are located on adjacent pins. Also, the input signals are not located near any of the output signals or the most active digital control lines. The separation of these signals on the IC package allows the printed circuit board designer to minimize crosstalk in the system by inserting ground traces between all active signal paths.

To understand how ground traces cut down on unwanted signal coupling, refer to Figure 2. Figure 2a shows the representation of two parallel conductors located close to each other over a ground plane, with no ground trace between them. Figure 2b is the equivalent circuit of the capacitive coupling that takes place between signals on the two conductors[1].

In this model, V_{IN} represents the active signal on trace 1, C_{12} is the stray capacitance between the conductors, C_{1G} and C_{2G} are the respective capacitances between

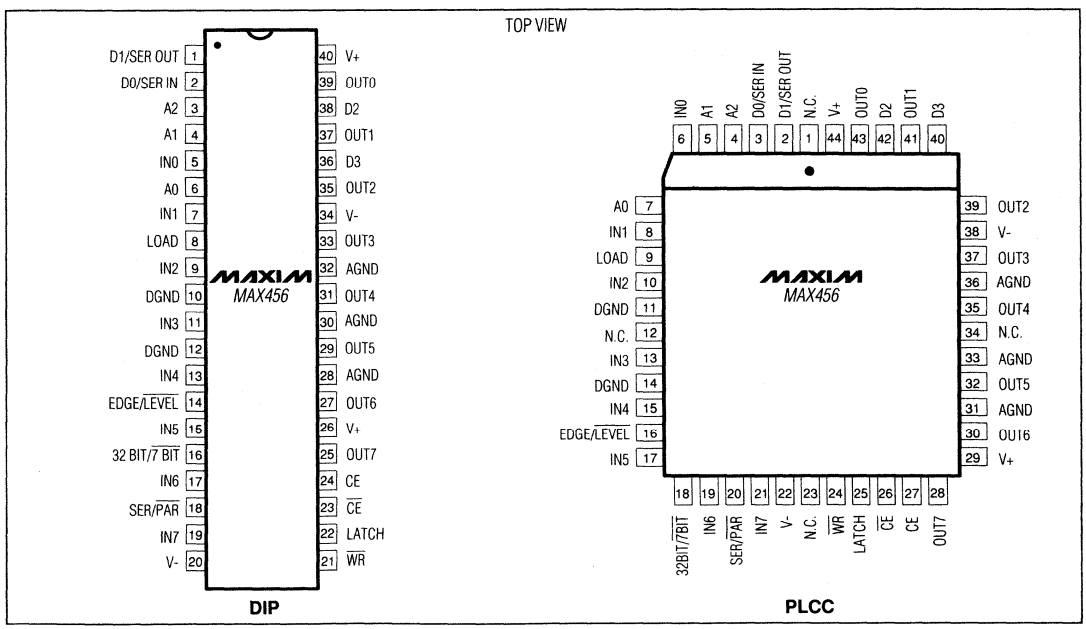


Figure 1

Designing With High-Speed, Low-Power Analog Integrated Circuits

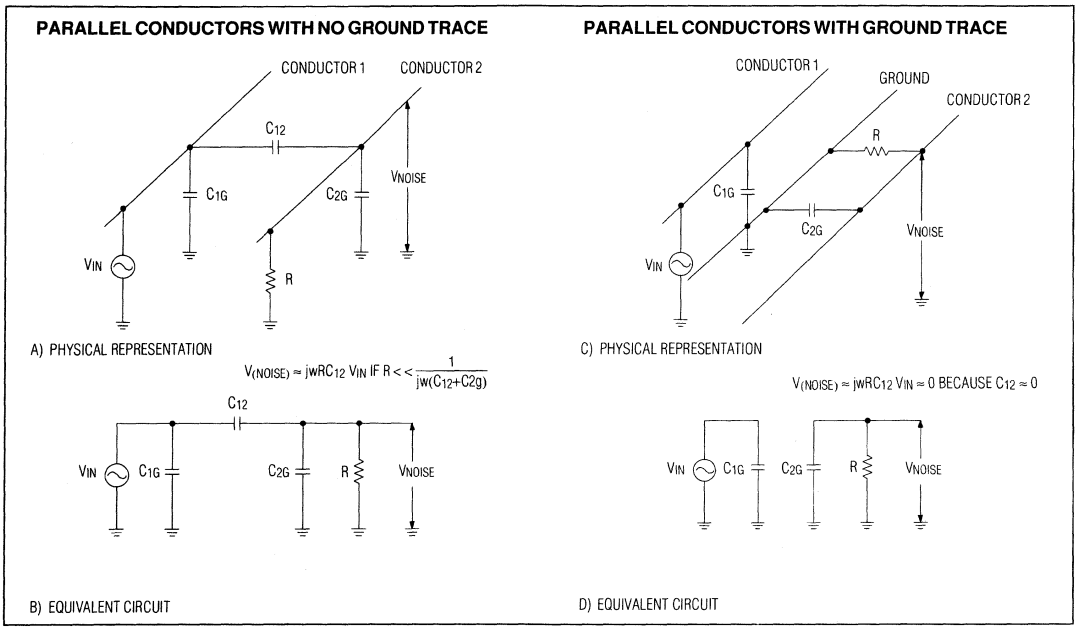


Figure 2

each conductor and the ground plane. R is the resistance from trace 2 to ground and V_{NOISE} represents the induced noise voltage, or crosstalk, on trace 2 due to capacitive coupling of the signal on trace 1.

For most practical applications, R will have a much lower impedance than the combined impedance of capacitance C_{12} and C_{2G}, in which case V_{NOISE} can be expressed as follows:

$$V_{NOISE} = jwRC_{12}\,V_{IN}$$

This equation shows that the induced noise voltage on trace 2 is proportional to the frequency and amplitude of the signal source on conductor 1 (V_{IN}), the capacitance between the conductors (C_{12}) and the resistance from conductor 2 to ground (R). Assuming that we have no control over the signal source, the induced noise voltage on conductor 2 can be reduced by one of two ways:

1) Reducing the capacitance between the conductors

2) Using the minimum value of resistance possible from conductor 2 to ground.

Capacitance between conductors can be reduced by orienting the conductors at 90° angles to each other or by separating them. Neither of these options is very practical for high-density circuit boards. Minimizing resistance values in high speed systems to limit parasitic effects is common practice and is strongly recommended.

When a ground trace is inserted between the two conductors, as shown in Figures 2C and 2D, the stray capacitance between adjacent conductors will effectively shunt any induced signal from trace 1 directly to

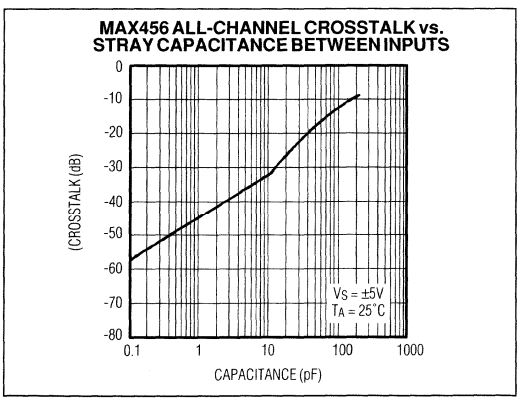


Figure 3

ground, and trace 2 will be relatively unaffected by signals on trace 1. The inverse of this statement also holds true.

For a practical representation of the effect of stray capacitance on crosstalk, see Figure 3. This figure is a plot of the isolation of one MAX456 input channel from all others versus the "stray" capacitance that is externally

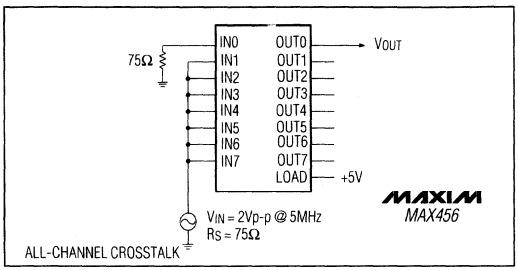


Figure 4

introduced between the selected channel and the unselected channels. This parameter is specified in the data sheet as "All-Channel Crosstalk" and is measured using the circuit configuration shown in Figure 4.

With no external capacitance between input channels, the typical specification for MAX456 All-Channel crosstalk (isolation between input channels) is 57dB with a 5MHz input signal. Figure 3 shows that this isolation is reduced to 32dB with only 10pF of external capacitance introduced between input channels. 10pF of capacitance could easily be introduced between input channels if proper layout practices are not followed[2].

Stray Capacitance and Stability in High Speed Amplifiers

Crosstalk through stray capacitance can also be troublesome to high frequency amplifier and comparator circuits. To prevent oscillation in op amp circuits, it is essential to isolate the non-inverting input terminal from the amplifier output terminal.

The circuit in Figure 5 has the MAX452 configured with a non-inverting gain of +2V/V (6dB). This circuit is commonly used to drive a back terminated 75Ω coaxial cable. This circuit configuration provides unity gain from the input of the MAX452 to the output of the cable, while eliminating signal reflections within the cable.

Figure 6 is a plot of the pulse response of this circuit to a 2Vp-p input square wave. This test circuit was constructed on a double sided copper clad board, with good isolation between signal traces and a ground plane on both sides of the board. The output square wave is a clean representation of the input waveform.

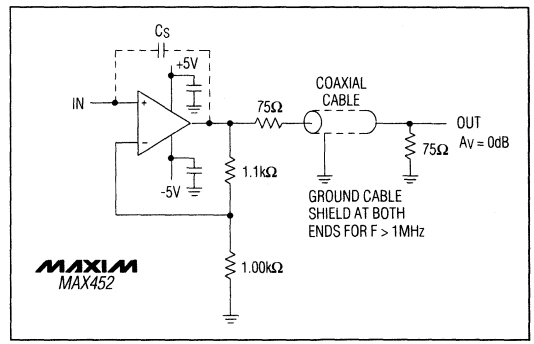


Figure 5. MAX452 Cable-Driving Circuit

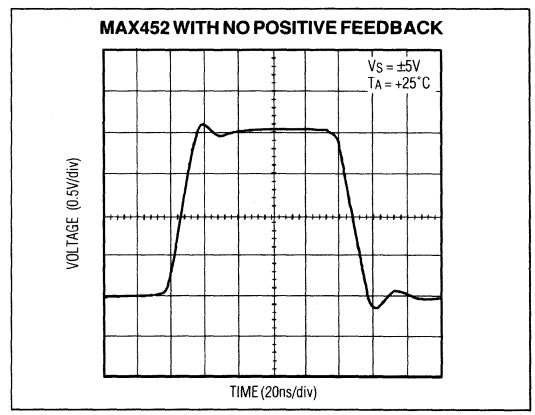


Figure 6

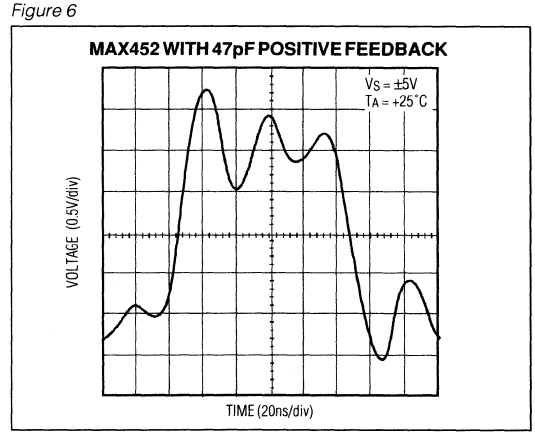


Figure 7

Designing With High-Speed, Low-Power Analog Integrated Circuits

To illustrate the effect of unwanted positive feedback due to stray capacitive coupling, a 47pF capacitor was introduced between the output of the MAX452 and the non-inverting input, represented as C_S in Figure 5. The output of the circuit under these conditions is plotted in Figure 7. Notice the severe oscillation that results when positive feedback is present in the circuit.

Stray Capacitance and Stability in High Speed Comparators

In high-speed comparator circuits, unwanted negative feedback is more troublesome than positive feedback. Positive feedback is often intentionally added to comparator circuits to provide hysteresis. This limits the amount of time that the comparator operates with its inputs in the linear region.

Comparators are designed for maximum open loop gain and minimum internal frequency compensation. High open loop gain increases the accuracy of a comparator by decreasing the amount of input overdrive that causes a level transition at the output. Minimizing frequency compensation reduces the response time of the comparator.

Unfortunately, these same attributes that maximize comparator performance also result in a strong tendency for oscillation if the comparator inputs are held in their linear region. Negative feedback in comparator circuits is undesirable for this reason.

The effects of negative feedback in comparator circuits can be compared in Figures 8 and 9. Figure 8 shows the input and output waveforms for the MAX9686 comparator operated with no feedback. The input waveform is a 50MHz sine wave. Compare the output waveform of Figure 8 (no feedback) with that of Figure 9, where negative feedback has been introduced into the circuit in the form of a 10pF capacitor from pin 3 (IN-) to pin 7 (OUT). An oscillating output signal is apparent when negative feedback is present.

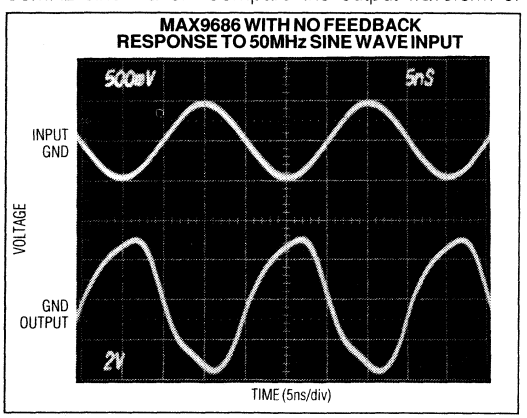


Figure 8

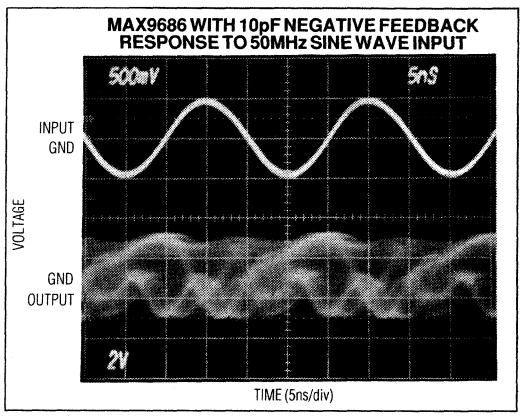


Figure 9

To reduce signal coupling through parasitics, ground planes should be used on both sides of the circuit board whenever possible. All areas of the circuit board that are not dedicated to a specific signal trace should be part of the ground plane. In addition, all sensitive circuit nodes such as non-inverting amplifier inputs, inverting comparator inputs, and any high impedance node in the circuit , where low level signals are present, should be encircled by a ground trace.

Power Supply Bypassing and Parasitic Inductance

An ideal power distribution system has zero impedance between the power source and the power supply connections to all of the circuit devices. Power supplies for high speed devices should have infinite DC impedance and zero AC impedance to ground (the characteristics of an ideal capacitor) when measured directly at the device power supply pins.

Unfortunately, no power distribution system is ideal. In fact, even at relatively low frequencies, the inductive reactance of a short (inch) power supply connection can be very significant. In addition to being a source of unwanted coupling, this inductance is also a source of circuit instability if it resonates with capacitance in the circuit.

Proper power supply bypassing and good PC board layout is the most effective means to limit parasitic induc-

Designing With High-Speed, Low-Power Analog Integrated Circuits

tance. When a component is properly bypassed, the AC load current to the device is supplied by the local bypass capacitor, effectively eliminating the common impedance between power supply connections to different devices.

For high current output devices, proper power supply decoupling should include a good energy storage capacitor (tantalum or aluminum electrolytic) in parallel and in very close proximity to a capacitor with good high frequency characteristics (a low inductance type such as ceramic). For high speed, low current applications, a ceramic capacitor alone should be sufficient.

MAX405 High Speed Buffer Amplifier

A typical video distribution system consists of several amplifiers, switches, multiplexers and other components cascaded together. Each of the components in the signal path contributes errors to the final output signal. The types of errors added by these components include:

1) DC gain error
2) Differential gain error
3) Differential phase shift

Amplifiers used in video systems are required to amplify wideband signals, usually at a low closed-loop gain such as 0dB or +6dB. To satisfy these requirements, video amplifiers are designed to maximize bandwidth, often at the expense of open-loop gain. The low open loop gain of video amplifiers, combined with losses in other components in the video signal path, result in significant gain or amplitude error in the output signal of the system.

The MAX405 high speed buffer amplifier is ideal for application as the output buffer amplifier for video systems. This device features a guaranteed minimum unadjusted gain of 0.99V/V when driving a 50Ω load over its full rated operating temperature range. Unlike other buffer amplifiers, the inverting input of the MAX405 is accessable to the user. This input can be connected to an external voltage divider to adjust the DC gain from 0.99V/V to 1.10V/V. The adjustable gain of this device allows calibration of the overall system gain in the output, instead of at each individual amplification stage in the system.

A typical application circuit that takes advantage of the adjustable gain of the MAX405 is the video distribution amplifier of Figure 10. This circuit will drive 4 150Ω loads (4 back terminated 75Ω coaxial cables) to ±2.25V. The receiving end of the cable will show a signal loss of -6dB due to the voltage divider formed by the 75Ω output load and the 75Ω back terminating resistor. The value of R1 should be selected to provide the desired signal amplitude at the output of the MAX405. The approximate

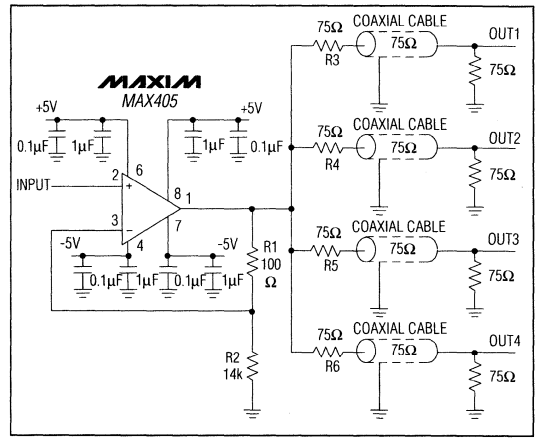


Figure 10. MAX405 Video Distribution Amplifier with Adjustable Gain

permissable range of values for R1 in this application would be from 0Ω to 1.4kΩ, which would correspond to signal gains of 0.99V/V to 1.10V/V.

The MAX405 will drive a 24MHz, 6Vp-p signal into a 50Ω load as shown in Figure 11. Other performance features of this part include a -3dB bandwidth of 180MHz, a 650V/µs slew rate and a settling time of 35ns to 0.1%. The MAX405 also features excellent differential gain and phase characteristics (0.03%, 0.01°) as discussed in the following section.

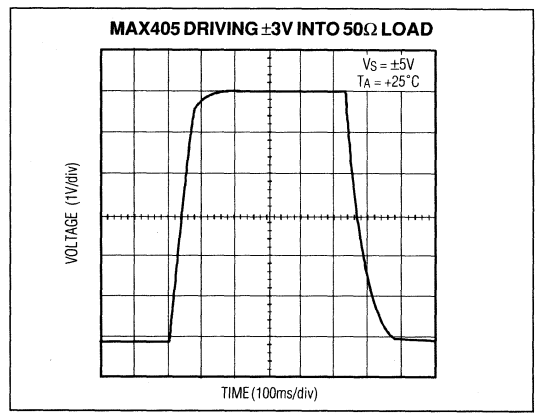


Figure 11

Differential Gain and Phase Error

A NTSC (National Television Standards Committee) color video signal consists of a 3.58MHz color subcarrier

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(chrominance signal) that is superimposed on the low frequency luminance (brightness) signal of a monochrome video system. Differential gain and phase error are non-linear signal distortions of the chrominance signal of a color video system. These error terms can be defined as follows:

1) Differential gain error is the change in the amplitude of the chrominance signal as the luminance signal is varied from the blanking level (0V, 0IRE) to the white level (0.714V, 100IRE).

2) Differential phase error is the change in the phase of the chrominance signal as the luminance signal is varied from the blanking level to the white level.

Differential gain and phase are measured using the modulated ramp waveform shown in Figure 12. The chrominance signal in this test waveform has a typical peak-to-peak amplitude of 40IRE (0.286V), and is centered around the luminance ramp.

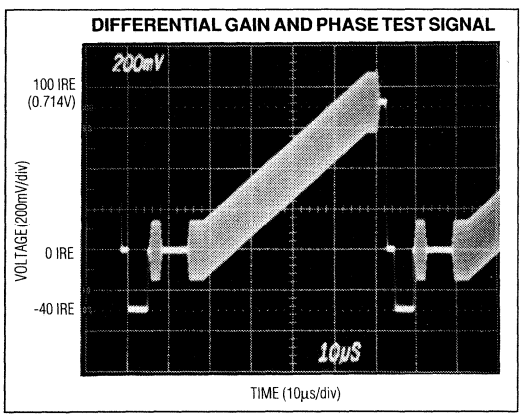

Figure 12

In color video applications, differential gain and phase error are critical specifications for an amplifier or buffer because they correspond to changes in the contrast and color of the displayed picture. For NTSC video systems, differential gain error of ±15% and differential phase shift of ±5° are the approximate error levels that are noticeable[3]. While this may seem to provide a large error budget for differential gain and phase of a video system, in practice the majority of these errors are due to the transmission of the video signal over the airwaves.

To prevent noticable errors in the transmitted color video signal requires that differential gain and phase errors for the transmitting and receiving ends the system be limited to a maximum of about 0.1% and 0.1°. These error specifications for broadcast quality color video systems mandate even more stringent requirements for the individual components in the system. The MAX405, with typical specifications for differential gain and phase error of 0.03% and 0.01° respectively at 25°C, is ideal for application in broadcast quality color video systems. The differential gain and phase performance of the MAX405 over its full operating temperature range is plotted in Figure 13.

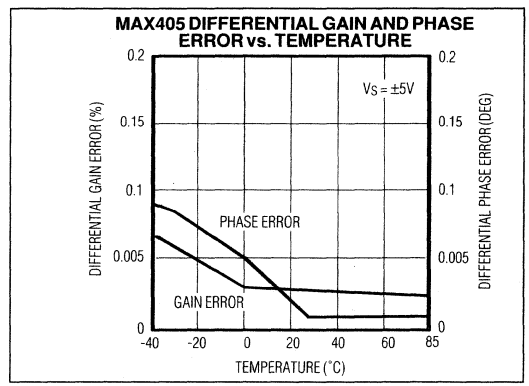

Figure 13

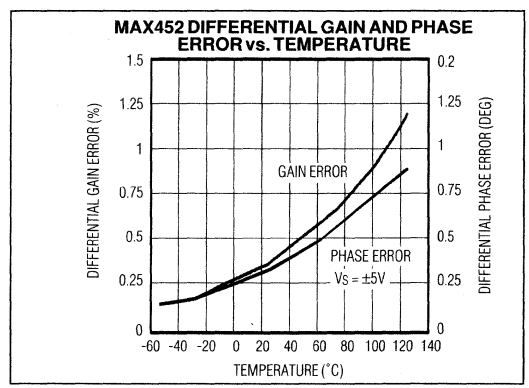

Figure 14

Many applications do not demand the same stringent level of differential gain and phase performance that is required of professional color video broadcast systems. Examples would include closed-circuit surveillance systems for security or medical applications and any monochrome video system. For this type of system, the MAX452 and MAX457 single and dual video amplifiers and the MAX453, MAX454 and MAX455 video multi-

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plexer/amplifiers provide excellent performance at low power and low cost. Figures 14 through 16 plot the differential gain and phase error of the MAX452, MAX453 and MAX457 video multiplexers/amplifiers over temperature.

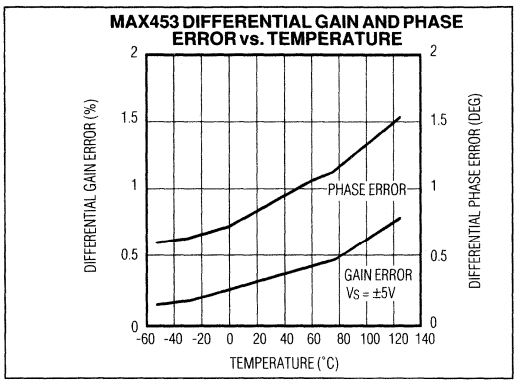

Figure 15

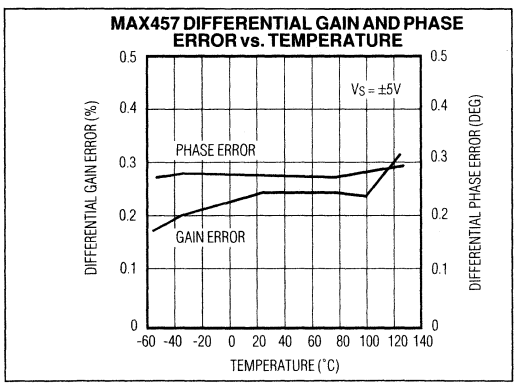

Figure 16

Comparators Combine Versatility and High-Speed Performance

For high-speed comparator applications requiring TTL or ECL output levels, Maxim provides a wide range of choices to meet most requirements. The MAX900/MAX901/MAX902/MAX903 TTL output comparators feature an unprecedented combination of high-speed, low-power performance. This device family features a typical propagation delay time of 8ns, while consuming only 18mW per comparator when operated with a +5V power supply. These parts, along with the MAX910 TTL output, threshold programmable comparator, will provide a valid TTL output signal when driven with a 100MHz, 20mVp-p sine wave, as shown in Figure 17.

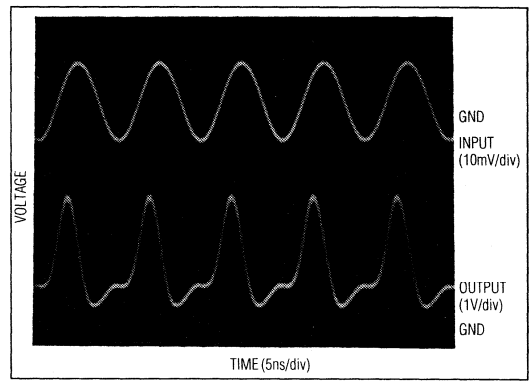

Figure 17

The MAX900-MAX903 comparators operate with a single supply voltage of +5V to +10V, or dual supplies of ±5V, with an input common mode range that includes the negative supply. These parts are available in several configurations including the MAX903 single, MAX902 dual and MAX900 quad comparator with latchable outputs. For higher density applications that do not require latched outputs, the MAX901 quad comparator eliminates the latch enable pins and is available in16 pin DIP and SO packages.

The MAX910/MAX911 comparators feature high-speed performance, programmable threshold voltages, and latched outputs. The MAX910 has a single ended TTL compatible output with a typical propagation delay of 8ns, while the MAX911 has a fully differential ECL-compatible output with a typical propagation delay of 2ns.

The threshold comparison voltage of the MAX910/MAX911 is set by an internal 8-bit DAC that has a pin selectable full-scale range of 2.55V or 5.10V. The data inputs to the DAC are latchable, so the threshold can be set once and then ignored until a different threshold voltage is required. The multiplying configuration of the internal DAC allows the use of an external reference input for applications requiring greater resolution for the threshold voltage.

The internal DAC in the MAX910 and MAX911 has a typical output settling time of 50ns. This fast settling time and the short propagation delays of the comparators allow a complete cycle of updating the threshold voltage, comparing it to an input voltage and receiving a valid output to be accomplished in less than 60ns.

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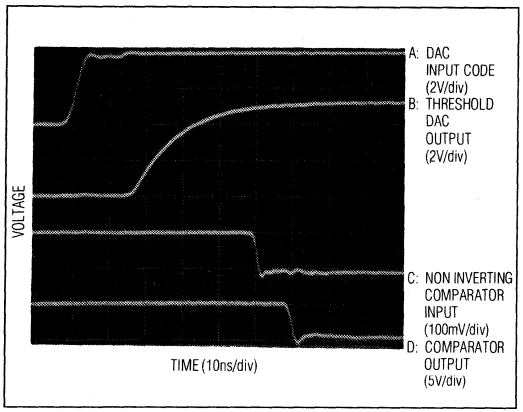


Figure 18

Figure 18 is a photograph of the response of a MAX910 during a complete cycle as described above. The time scale for all 4 of the traces in Figure 18 is 10ns/div. Trace A is the input signal to all 8 bits of the DAC as the input code is changed from all 0's to all 1's. The vertical scale for Trace A is 2V/div. Trace B is the DAC output waveform as it responds to the full-scale output transition (-2.54V to +2.56V) set by the changing input code shown in Trace A. Trace C is the signal on the non- inverting comparator input, which is switched from +2.6V to +2.5V, after waiting 50nS for the DAC output to settle. Trace D is the output transition of the comparator (+5V to 0V) which follows approximately 8nS after the input transition. The time required for the completion of the entire cycle is about 58ns.

The quick response of these comparators to threshold voltage changes make them excellent devices for use at the front end of multiple channel, high-speed data acquisition systems. In systems that require comparison of several input signals to different threshold voltages, the MAX910/MAX911 will replace many comparators and voltage references.

Separate Power Supply Connections and High-Speed Comparator Performance

The MAX900-MAX903 single, dual and quad high-speed comparators and the high speed, threshold programmable MAX910/MAX911 all provide separate power supply pins for the input (analog) and the output (digital) stages. An advantage of this configuration is the ability to isolate the analog and digital parts of the system by using separate power supply and ground connections to the comparator. This prevents crosstalk from a noisy digital ground plane to the sensitive comparator inputs, which can result in false output level transitions. Even if the same power supplies are used for the input and output stages, separate bypassing of the power supply connections optimizes the performance of the comparator.

Separate power supply connections can be used to level shift signals through the comparator. This feature is useful in applications where a bipolar input signal is compared to a reference and the output interfaces with TTL logic. Comparators that do not provide a separate ground connection for the output stage would require the addition of a level shifting circuit between the comparator output and the TTL logic. Level shifting of this type is accomplished in the MAX900-903 and MAX910 by simply connecting bipolar power supplies to the input and +5V and GND to the output power supply terminals.

Comparator Output Stages, Active vs. Open Collector

All Maxim TTL compatible comparators feature active output stages, which do not require external pull-up resistors. A standard comparator with an open collector output would require low value, power hungry pull-up resistors to achieve high speed performance. The MAX900 family's active output stages eliminate pull-up resistors, saving circuit board space and power.

REFERENCES

1) "Noise Reduction Techniques in Electronic Systems" by Henry W. Ott, Wiley and Sons, 2nd Edition, 1988.

2) "Grounding and Shielding Techniques in Instrumentation" by Ralph Morrison, Wiley and Sons, 3rd Edition, 1986.

3) "Television Engineering Handbook" edited by K. Blair Benson, McGraw-Hill, 1986.

General Description

Maxim's MAX310 and MAX311 are CMOS monolithic analog multiplexer/demultiplexers designed for use with signal frequencies ranging from DC through video. The MAX310 is a 1-of-8 multiplexer while the MAX311 is for 2-of-8 (4 channel differential) applications.

A key feature of the MAX310/311 is extremely high off isolation at high frequencies. The isolation of each off channel to the output is guaranteed to be -66dB at 5MHz. The input signal range is +12V to -15V with ±15V power supplies while power consumption is typically 1.1mW.

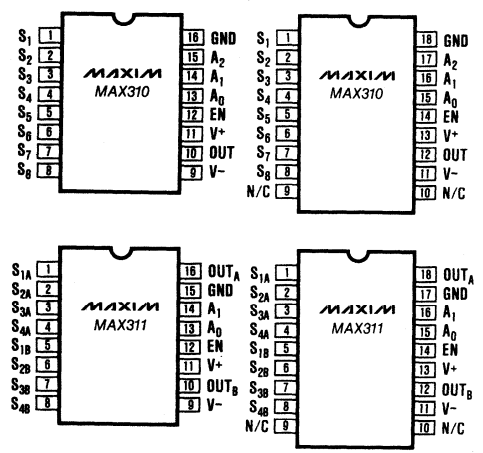
All control inputs are fully compatible with TTL and CMOS logic. Decoding is in standard BCD format and an Enable input is also provided to simplify cascading of devices. The MAX310 and MAX311 will operate with nearly any power supply combination which totals less than 36V ($V^+ - V^-$) including single supply operation at +12V, +15V, and +28V with V^- connected to GND.

Applications

Video Switching and Crosspoint Systems
Automatic Test Equipment
Medical Ultrasound Phased Array Systems
Data Logging of High Frequency Signals
Digital Signal Processing

Pin Configuration

Top View



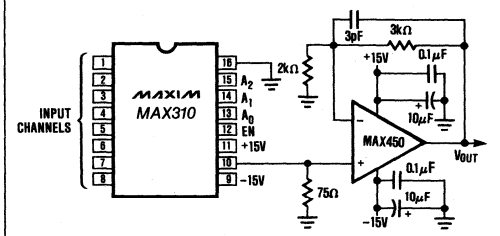
Features

- **-76dB Typical Off Isolation at 5MHz**
- **-63dB Typical "All Channel Off" Isolation at 5MHz**
- **Phase Shift Match Between Channels, <1° at 5MHz**
- **Break-Before-Make Switching**
- **Wide Supply Range, ±4.5V to ±16.5V and Single Supply**
- **Symmetrical, Bi-directional Operation**
- **Latch-Up Proof Construction**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX310C/D	0°C to +70°C	Dice
MAX310CPE	0°C to +70°C	16 Lead Plastic DIP
MAX310CWN	0°C to +70°C	18 Lead Wide SO
MAX310EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX310EWN	-40°C to +85°C	18 Lead Wide SO
MAX310EJE	-40°C to +85°C	16 Lead CERDIP
MAX310MJE	-55°C to +125°C	16 Lead CERDIP
MAX311C/D	0°C to +70°C	Dice
MAX311CPE	0°C to +70°C	16 Lead Plastic DIP
MAX311CWN	0°C to +70°C	18 Lead Wide SO
MAX311EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX311EWN	-40°C to +85°C	18 Lead Wide SO
MAX311EJE	-40°C to +85°C	16 Lead CERDIP
MAX311MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



No Insertion Loss, 8 Channel Mux

CMOS RF/Video Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage referenced to V⁻
- V⁺ ..... +36V
- GND ..... +24V
- Digital Inputs ..... V⁻ to V⁺

Input Current
- S and COMMON OUT ..... ±50mA
- All pins except S and COM. OUT ..... ±30mA

Lead Temperature ..... +300°C

Storage Temperature ..... -65°C to +150°C

Operating Temperature Range
- MAX310C, MAX311C ..... 0°C to +70°C
- MAX310E, MAX311E ..... -40°C to +85°C
- MAX310M, MAX311M ..... -55°C to +125°C

Power Dissipation (16-Pin packages)
- CERDIP (derate 10mW/°C above +75°C) 750mW
- Plastic DIP (derate 7.35mW/°C above +75°C) 550mW
- Small Outline (derate 9mW/°C above +75°C) 550mW

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Over Temperature, V^+ = +15V, V^- = -15V, GND = 0V unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range		V^+, V^- = ±15V V^+, V^- = ±5V	-15 -5		+12 +2	V
Channel ON Resistance	R_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA T_A = +25°C Over Temp.		150	250 300	Ω
ON Resistance Match	ΔR_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA		6		%
OFF Input Leakage Current	$I_{S(OFF)}$	Figure 10, T_A = +25°C Over Temp		0.4 3	10 100	nA
OFF Output Leakage Current	$I_{D(OFF)}$	Figure 11, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		0.8 20 10	10 100 50	nA
ON Channel Leakage Current	$I_{D(ON)}$	Figure 12, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		1 30 15	10 200 100	nA
Input Low Threshold	V_{AL}	V^+/V^- = ±15V, ±5V			0.8	V
Input High Threshold	V_{AH}	V^+/V^- = ±15V, ±5V	2.4			V
Input Current (Logic)	I_A	V_A = 0V or 5V			±10	µA
Access Time	t_{ACC}	Figure 7; T_A = +25°C Over Temp.		0.6	1.5 2.0	µs
Enable Delay ON or OFF	$t_{EN(ON/OFF)}$	Figure 8; T_A = +25°C Over Temp.		0.3	1.0 2.0	µs
Break-Before-Make Delay	t_{ON}-t_{OFF}	Figure 9	30	100		ns
OFF Isolation, Single Channel to OUT	ISO_{SC}	Figure 3; T_A = +25°C	-66	-76		dB
OFF Isolation, All Channels to OUT	ISO_{AC}	Figure 4, 5, T_A = +25°C MUX Disabled, EN = +0.8V MUX Enabled, EN = +2.4V		-63 -58		dB
Adjacent Channel Crosstalk	ISO_X	Figure 6, T_A = +25°C		-72		dB
Channel Input Capacitance OFF State ON State	 $C_{S(OFF)}$ $C_{S(ON)}$	T_A = +25°C, V_{IN} = 10mV_{RMS} 10 MHz		 5 45		pF
Channel Output Capacitance OFF State ON State	 $C_{D(OFF)}$ $C_{D(OFF)}$	T_A = +25°C; EN = +0.8V, MAX310 MAX311 EN = +2.4V, MAX310 MAX311		 38 20 57 40		pF
Charge Injection	Q	Figure 13, T_A = +25°C		110		pC
Supply Current; V^+ V^-	I^+ I^-	EN, A0, A1, A2 = 0V or +5V		75 0.1	200 100	µA
Supply Voltage Range		T_A = +25°C	±4.5		±16.5	V

Detailed Description

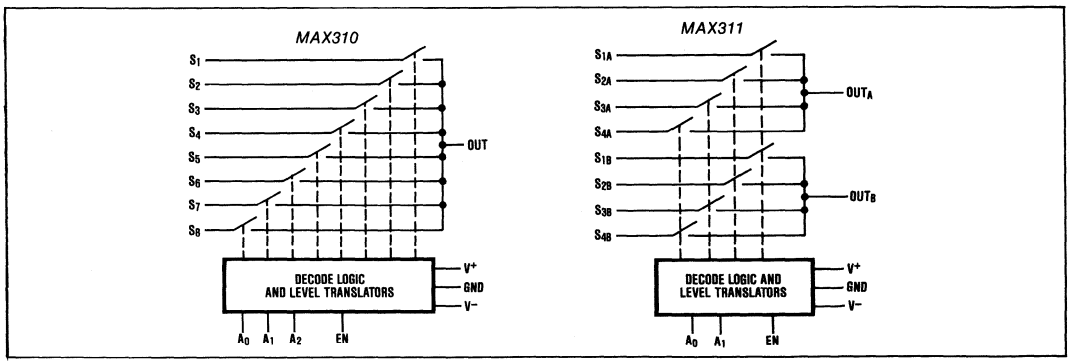


Figure 1. Functional Block Diagrams

The Maxim MAX310 and MAX311 contain 8 video switches combined with an address decoder and level translators (Figure 1). Each of the 8 video switches consists of 3 N-channel FETs configured as shown in Figure 2. This "T" configuration provides the high frequency OFF isolation required when switching wide-band video, audio, or digital signals.

N-channel FETs are used in the MAX310/311's "T" switches because of their low capacitance and consequently superior isolation characteristics. A side effect is that the N-channel ON resistance varies somewhat with the voltage difference between the analog input signal and V^+. This effect is shown in the Typical Operating Characteristics section.

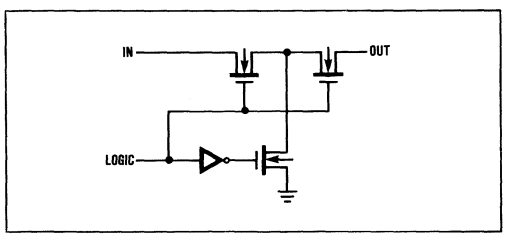


Figure 2. N-channel T Switch

Channel selection is performed by applying a binary input to the address inputs A_0, A_1 and A_2 (A_0 and A_1 only for MAX311). The address decoder selects channels as shown in the truth tables (Table 1). All digital inputs are compatible with TTL and CMOS logic levels.

Break-before-make switch timing is guaranteed for both multiplexers. This prevents momentary shorting of inputs when changing multiplexer channels.

The MAX310 and MAX311 are also fully bilateral and so can be used "backwards", as demultiplexers, with no loss in performance. Specifically, one input signal can be routed to one of several outputs.

TABLE 1. CHANNEL SELECTION INPUT CODES

MAX310					MAX311			
A_2	A_1	A_0	EN	ON Channel	A_1	A_0	EN	ON Channel
0	0	0	1	1	0	0	1	1A + 1B
0	0	1	1	2	0	1	1	2A + 2B
0	1	0	1	3	1	0	1	3A + 3B
0	1	1	1	4	1	1	1	4A + 4B
1	0	0	1	5	X	X	0	ALL OFF
1	0	1	1	6				
1	1	0	1	7				
1	1	1	1	8				
X	X	X	0	ALL OFF				

Application Hints

Maximizing Isolation

With all high frequency circuits, careful printed circuit board layout is essential for optimum performance. To maintain the high frequency isolation of the MAX310/311, signal paths should be of minimum length and ground plane should be used where possible, including between adjacent input pins. A ground or power supply trace between adjacent inputs will markedly improve isolation between channels.

Both V^+ and V^- should be bypassed to ground with 0.1μF ceramic capacitors. The leads of the capacitors should be kept as short as possible to minimize

series inductance. The bypass capacitors should also be located as physically close to the multiplexer as possible.

Input Capacitance

The capacitance of an input channel changes from about 5pF in the OFF state to around 45pF when ON. To minimize bandwidth reduction due to input capacitance, the inputs should be driven from a low impedance source. A 75Ω source impedance results in a 3dB frequency response of 47MHz when loaded with 45pF.

Charge Injection

With ±15V supplies, injected charge from the internal switch drive circuitry to the analog signal path is typically 110 picocoulombs. As shown in the Typical Characteristics graph, charge injection is relatively independent of the analog signal voltage.

Insertion Loss

With ±15V supplies and ±2V video signals, the 120Ω typical ON resistance of the MAX310/311 results in -8.3dB insertion loss when used with a 75Ω output load. This insertion loss is virtually constant from DC to over 20MHz.

TABLE 2. PHASE SHIFT AT 10MHz

INPUT CHANNEL MAX311	OUTPUT - INPUT PHASE SHIFT	
	R_L = 10kΩ	R_L = 75Ω
S_1	-22°	-12°
S_2	-21°	-11.5°
S_3	-20°	-11.5°
S_4	-20°	-11.2°
S_5	-20°	-11.2°
S_6	-20.5°	-11.4°
S_7	-20.7°	-11.5°
S_8	-20.4°	-11.5°

Test Conditions: V^+ = +15V, V^- = -15V, V_{IN} = 1.25V_{RMS} at 10MHz, OFF inputs terminated with 75Ω.

Operation with Power Supplies Other Than ±15V

Table 3 shows how different power supply voltages affect the MAX310/311's analog signal range and channel ON resistance (R_{ON}). This data is also shown graphically in the Typical Operating Characteristics section. Since N-channel FETs are used in the switches, R_{ON} is determined by the voltage difference between V^+ and the input voltage. For lowest R_{ON}, use a negative power supply (V^-) equal to the most negative input voltage, and a positive power supply (V^+) 30V above the negative supply. For example, if only positive signals need to be switched, use 0V for V^- and +30V for V^+ to achieve minimum R_{ON}. This also reduces ON resistance variation with analog signal level and input voltage dependent changes in insertion loss, which minimizes differential gain errors.

The digital input thresholds are nearly independent of V^+, remaining near +1.4V over the entire operating supply voltage range of ±4.5V to ±18V (9V to 36V single supply).

The MAX310/311 switching delay times vary somewhat with power supply voltage. Access time (see Figure 2) increases from typically 600ns with ±15V supplies to 3μs with ±5V supplies. Other switching times are also proportionately longer with ±5V power supplies.

Propagation Delay and Phase Shift

In Table 2, the typical phase shift for each channel is shown. Note that both the phase shift and the phase shift difference between channels are reduced with a 75Ω output load. At 10MHz, the channel-to-channel match is better than 1° with a 75Ω load and improves as the frequency is reduced.

Phase shift measurements for the MAX311 are similar to those in Table 2. The data for the MAX310 channels 1 to 4 corresponds to MAX311 channels 1A to 4A, Channels 5 to 8 correspond to MAX311 channels 1B to 4B.

TABLE 3. SIGNAL RANGE AND R_{ON} vs SUPPLY VOLTAGE

SUPPLY VOLTAGE		SIGNAL RANGE	TYPICAL R_{ON} AT V_{IN}	
V^-	V^+		NEGATIVE	POSITIVE
-15	+15V	-15V to +12V	104Ω at -10V	265Ω at +10V
		-5V to +5V	115Ω at -5V	150Ω at +5V
GND	+15V	0V to +12V	120Ω at 0V	150Ω at +5V
GND	+30V	0V to +27V	90Ω at 0V	100Ω at +5V
-5V	+5V	-5V to +2V	240Ω at -2V	480Ω at +2V
-10V	+10V	-10V to +7V	140Ω at -5V	220Ω at +5V
-5V	+15V	-5V to +12V	115Ω at -5V	150Ω at +5V

OFF Isolation Measurements

Figure 3 is used to test and specify the MAX310/311's single channel OFF isolation. In the case illustrated, channel S_1 has signal applied while all other inputs are grounded through 75Ω except for the ON channel (S_2 in Figure 3). This is shorted directly to ground to prevent pickup from external wiring. Each channel meets this test to an isolation limit of -66dB at 5MHz.

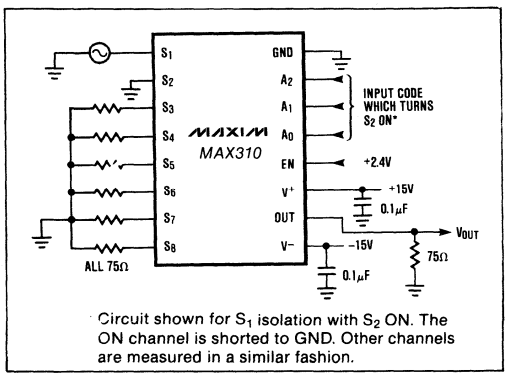


Figure 3. Single Channel OFF Isolation (ISO_{SC}) Test Circuit

Figure 4 shows the test circuit for OFF isolation with all channels driven. The impedance of the source connected to the selected channel (in this case, S_4) significantly affects feedthrough. With a 75Ω source impedance the typical measured OFF isolation is -58dB at 5MHz. This increases to -63dB if the source impedance is reduced to 10Ω or less. OFF isolation also increases with decreasing frequency. For example, when the frequency is reduced from 10MHz to 1MHz the isolation improvement is typically -20dB. Figure 5 shows a similar circuit for testing all-channel isolation with the multiplexer disabled (EN low).

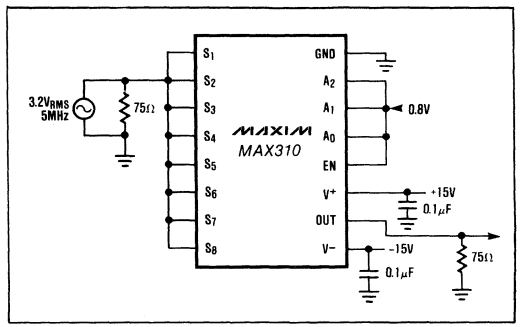


Figure 4. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Disabled)

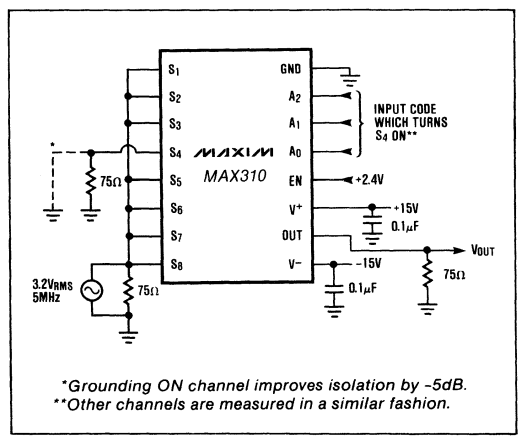
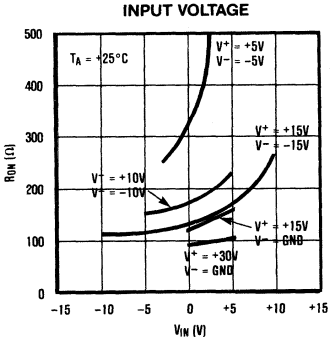


Figure 5. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Enabled)

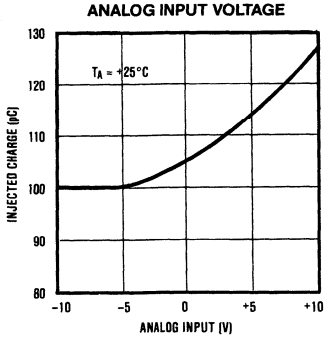
Typical Operating Characteristics

8

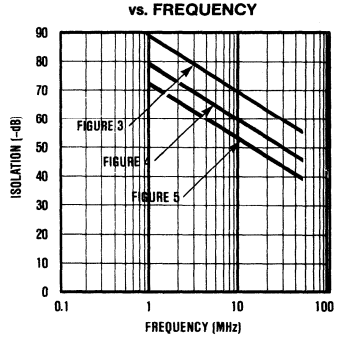
RON vs. SUPPLY VOLTAGE AND INPUT VOLTAGE



CHARGE INJECTION vs. ANALOG INPUT VOLTAGE



OFF ISOLATION vs. FREQUENCY



CMOS RF/Video Multiplexers

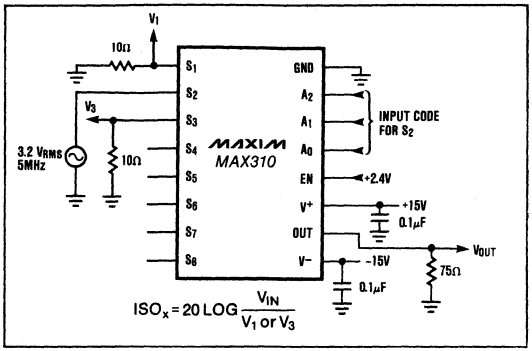


Figure 6. Adjacent Channel Crosstalk (ISO_X) Test Circuit

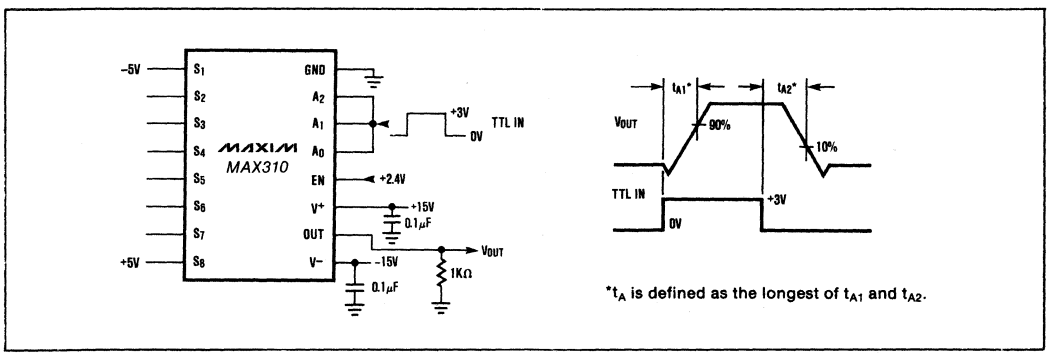


Figure 7. Access Time (t_A) Test Circuit.

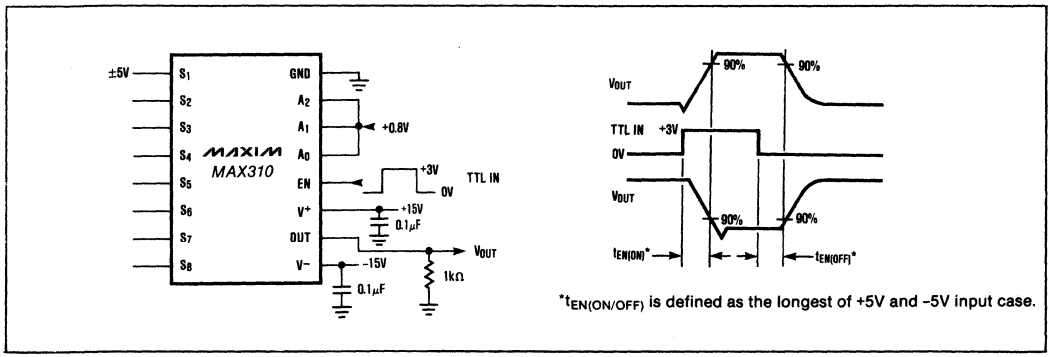


Figure 8. Enable Delay ($t_{EN(ON/OFF)}$) Test Circuit.

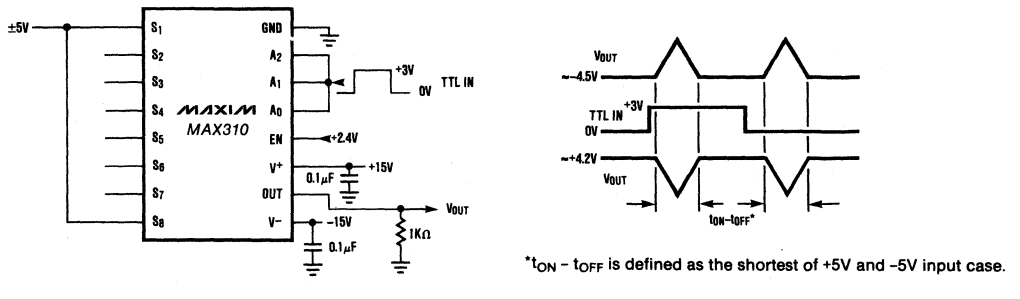


Figure 9. Break-Before-Make Delay (t_{ON}-t_{OFF}) Test Circuit.

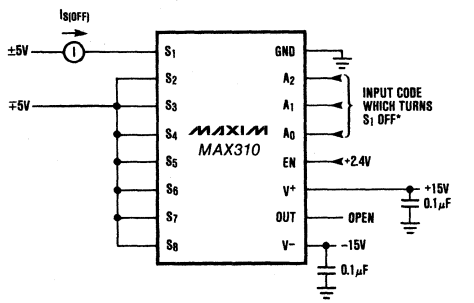


Figure 10. OFF Input Leakage Current Test Circuit.

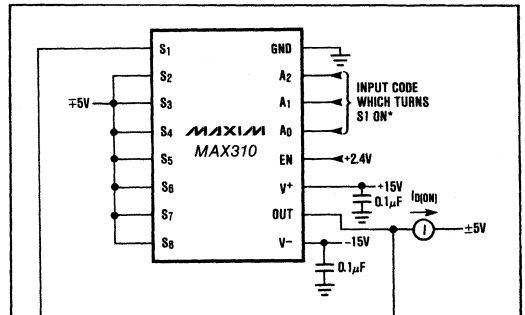


Figure 12. ON Output Leakage Current Test Circuit.

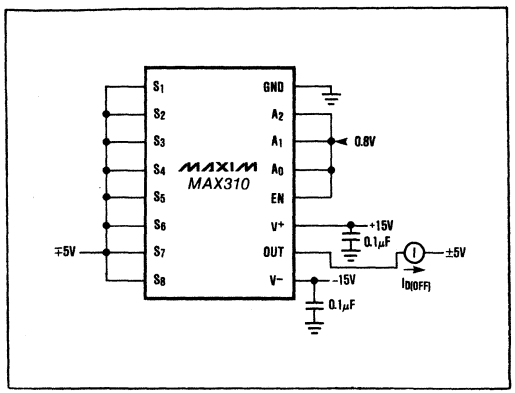


Figure 11. OFF Output Leakage Current Test Circuit.

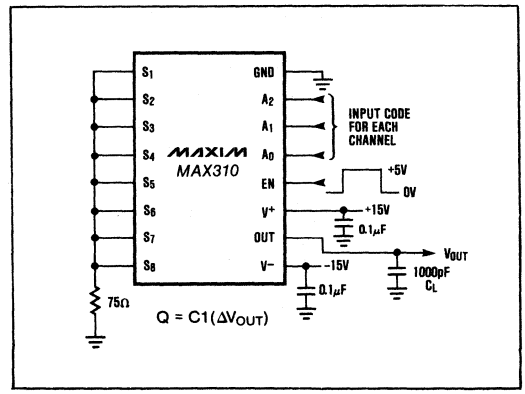


Figure 13. Charge Injection (Q) Test Circuit

CMOS RF/Video Multiplexers

Typical Applications

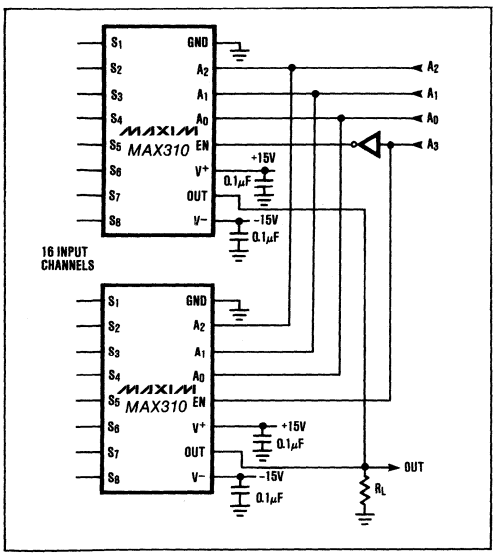


Figure 14. Cascading 2 MAX310s For 1 of 16 Multiplexer

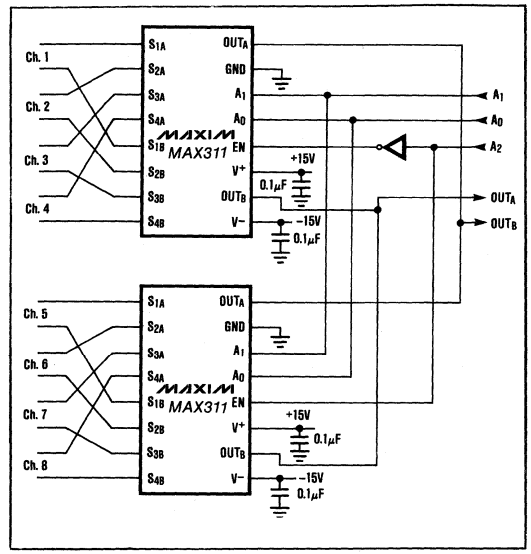
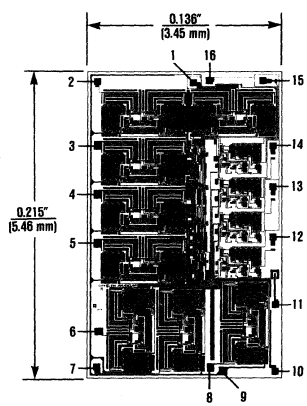


Figure 15. Cascading 2 MAX311s For 1 of 8 Differential Multiplexer.

Chip Topography



(See Pin Configurations for MAX310 and MAX311 pin functions)

ADVANCE INFORMATION
Data Sheet in Preparation

MAXIM

Video Operational Amplifier

General Description

TheMAX404 is a high-speed operational amplifier optimized for exceptional AC performance, output drive and stability while operating from ±5V power supplies. Featuring 80MHz gain-bandwidth, 500V/µs slew rate and 0.01°/0.05% differential phase and gain, this amplifier is ideal for video and other high-speed applications.

The MAX404 remains stable while driving unlimited capacitive loads. As a result, flash A/D converter inputs, long distance coaxial cables, and other large or varying capacitive loads can be driven without output oscillations or ringing.

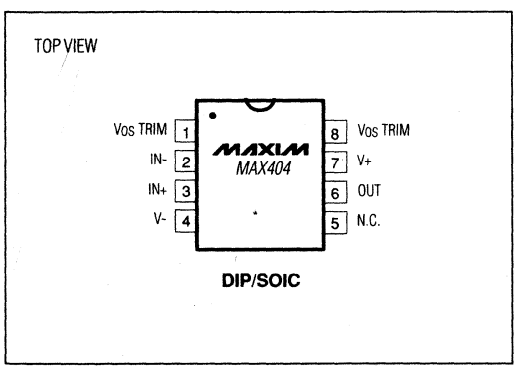
Unlike current-feedback amplifiers, the MAX404 can be used in virtually all high-speed op amp applications because it has fully symmetric differential inputs, 70dB common-mode rejection ratio (CMRR), and 66dB of open-loop gain.

The MAX405 guarantees 50mA continuous output current and ±3V swing into 100Ω. Stable for gains of 2V/V or greater, the amplifier is optimized for applications such as 50Ω and 75Ω coaxial cable drivers in video test equipment, radar displays, medical imaging, and RGB systems.

Applications

Video Coax Line Drivers
Video Distribution
Flash A/D Converter Input Amplifier
High-Speed Signal Processing
Pulse & RF Amplifiers
High Resolution Video
Medical Imaging

Pin Configuration



Features

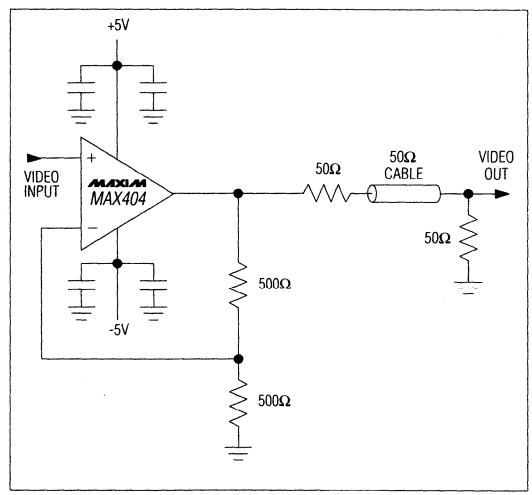
- ♦ **0.01°/0.05% Differential Phase/Gain**
- ♦ **80MHz Gain Bandwidth**
- ♦ **500V/µs Slew Rate**
- ♦ **50mA Continuous Output Current**
- ♦ **Stable With Any Capacitive Load**
- ♦ **66dB Open-Loop Gain**
- ♦ **70dB CMRR**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX404CPA	0°C to +70°C	8 Lead Plastic DIP
MAX404CSA	0°C to +70°C	8 Lead SO
MAX404C/D	0°C to +70°C	Dice*
MAX404EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX404ESA	-40°C to +85°C	8 Lead SO

** Dice are tested at 25°C only*

Typical Application Circuit



Video Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Voltage at any pin ..... (V- -0.3V) to (V+ +0.3V)
OUT short-circuit to ground ..... 60 sec
Power Dissipation
  Plastic DIP (derate 9.0mW/°C above +70°C) 725mW
  SO (derate 6mW/°C above +70°C) 470mW

Operating Temperature (T_{AMIN}-T_{AMAX})
  MAX404CPA, CSA, C/D ..... 0°C to +70°C
  MAX404EPA, ESA ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, -3V < V_{IN} < +3V, R_L = 100Ω, C_L = 15pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{AMIN} to T_{AMAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	T_A = +25°C		±1	+8				mV
		0°C to +70°C						±10	
		-40°C to +85°C						±12	
Input Offset Voltage Tempco	Δ V_{OS}/Δ T			±20					mV/°C
Input Bias Current (Note 1)	I_{IN+}, I_{IN-}	T_A = +25°C		±1	±3				µA
		0°C to +70°C						æ5	
		-40°C to +85°C						±8	
Input Resistance (Common Mode)	R_{IN}	Gain = 1V/V DC		1					MΩ
Input Capacitance	C_{IN}			3					pF
Input Common Mode Voltage Range	V_{IN}		±3	±3.5		±3			V
Open Loop Voltage Gain	A_{VOL}	V_{OUT} = 6V_{P-P}	54	66		54			dB
Min. Output Voltage Swing	V_{OUT}	R_{LOAD} = 100Ω	±3.0	±3.5		±3.0			V
		R_{LOAD} = 50Ω	æ2.5	±3.0		±2.5			
Output Current Continuous Short Circuit	I_{OUT}	R_{LOAD} = 50Ω	æ50			±50			mA
		R_{LOAD} = 0Ω		æ90					
Output Resistance	R_{OUT}	Gain = 2V/V		30					mΩ
Power Supply Rejection Ratio	PSRR	| V+, V- | = 4.75 to 5.25V	40	50		40			dB
Common Mode Rejection Ratio	CMRR	V_{IN} = -3V to +3V	60	70		60			dB
Supply Current	I+, I-	T_A = +25°C	25	30	35				mA
		0°C to +70°C				20		45	
		-40°C to +85°C				15		50	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V, -3V < V_{IN} < +3V, R_L = 100Ω, CL = 15pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{AMIN} to T_{AMAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC SPECIFICATIONS									
Gain Bandwidth	GBW	Gain = 10V/V		80					MHz
Slew-Rate	SR	3V step		500					V/µs
Full-Power Bandwidth		V_{OUT} = $6V_{P-P}$		13					MHz
Closed Loop Bandwidth	BW	Gain = 2V/V		60					MHz
Differential Phase (Note 2)	DP	Gain = 2V/V		0.01					deg
Differential Gain (Note 2)	DG	Gain = 2V/V		0.05					%
Settling Time to 0.1%	t_S	Gain = -1V/V, 3V step		70					ns

Note 1: V_{IN} = 0V DC
Note 2: Input test signal: 3.58MHz sine wave of amplitude superimposed on a linear ramp (0 to 100 IRE). 140 IRE = 1.0V.

19-3819; Rev. 0, 6/91

MAXIM

Precision Video Buffer Amplifier

General Description

The MAX405 high-speed, precision buffer amplifier guarantees a minimum gain of 0.99V/V over -40°C to +85°C, with loads as low as 50Ω. It operates from ±5V power supplies and drives ±3V signals into 50Ω loads, or ±2.25V into four 150Ω loads. The MAX405 features 180MHz bandwidth, 650V/µs slew rate, and 35ns settling time to 0.1%. Precision characteristics include 0.01° differential phase, 0.03% differential gain, and guaranteed 0.1% nonlinearity over temperature. Unlike other buffer amplifiers, the MAX405's inverting input can be used to increase the gain.

The MAX405 is ideal as a 50Ω and 75Ω coaxial cable driver for color video signals. Guaranteed 60mA continuous output current eliminates the need for multiple buffers, external power-booster circuits, or expensive hybrid modules common in video distribution applications. Greater PC-layout densities are provided by compact 8-pin DIP and SO packages.

Applications

Video Distribution

Flash A/D Input Buffers

Coaxial Line Drivers

Fast Sample-and-Hold Buffers

Features

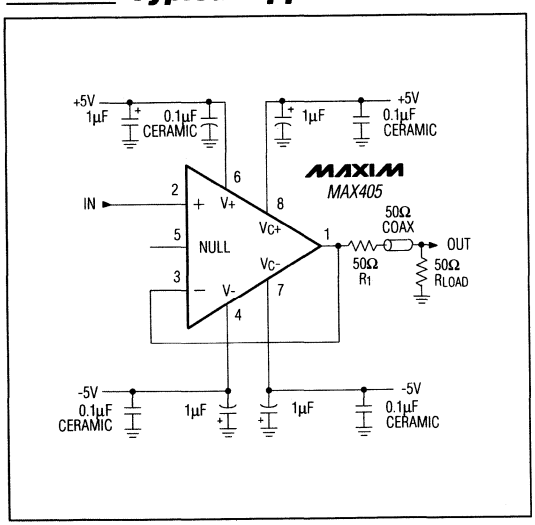
- ♦ **0.99V/V Min DC Gain (R_L = 50Ω) Over Temp**
- ♦ **0.01° Differential Phase**
- ♦ **0.03% Differential Gain**
- ♦ **0.1% Nonlinearity Over Temperature**
- ♦ **180MHz Bandwidth**
- ♦ **650V/µs Slew Rate**
- ♦ **60mA Continuous Output Current**
- ♦ **0.01Ω R_{OUT}**
- ♦ **0.6pF Input Capacitance**
- ♦ **Drives Four 150Ω Loads**
- ♦ **Adjustable Gain Control**

Ordering Information

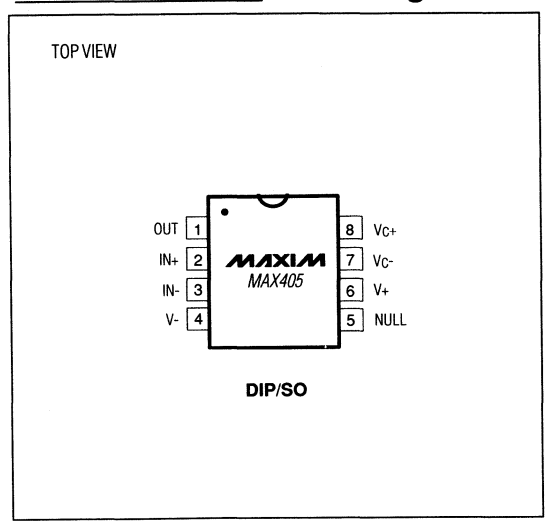
PART	TEMP. RANGE	PIN-PACKAGE
MAX405CPA	0°C to +70°C	8 Plastic DIP
MAX405CSA	0°C to +70°C	8 SO
MAX405C/D	0°C to +70°C	Dice*
MAX405EPA	-40°C to +85°C	8 Plastic DIP
MAX405ESA	-40°C to +85°C	8 SO

Contact factory for dice specifications.

Typical Application Circuit



Pin Configuration



8

Precision Video Buffer Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Voltage at Any Pin ..... (V- -0.3V) to (V+ +0.3V)
Output Current (I_{OUT}) 250mA
Short-Circuit Duration (I_{OUT}) ..... 10 sec
Continuous Power Dissipation
Plastic DIP (derate 8.3mW/°C above +70°C) 660mW
SO (derate 6mW/°C above +70°C) 470mW

Operating Temperature Ranges:
MAX405C_A ..... 0°C to +70°C
MAX405E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

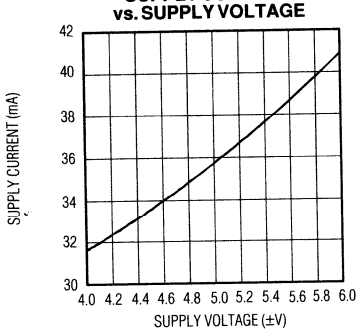
($V+ = V_{C+} = 5V$, $V- = V_{C-} = -5V$, $R_L = 50\Omega$, $C_L = 15pF$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = +25°C$			$T_A = T_{MIN}$ to T_{MAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	A_V	Unadjusted	0.9910	0.9940	1	0.9900		1	V/V
		Adjusted			1.1			1.1	
Offset Voltage	V_{OS}		-5.0	±2.0	5.0				mV
		T_A = 0°C to +70°C				-6.5		6.5	
		T_A = -40°C to +85°C				-8.0		8.0	
Offset Voltage TC	TCV_{OS}						25		µV/°C
Input Bias Current	I_B(IN+)	V_{IN} = 0V	-2		2	-4		4	mA
	(IN-)			10					
Input Resistance	R_{IN}			2.5					MΩ
Input Capacitance	C_{IN}			0.6					pF
Output Voltage Swing	V_{OUT}		-3.0	±3.4	3.0	-3.0		3.0	V
Output Current	I_{OUT}	Continuous	60			60			mA
		Short-circuit (Note 1)	90	180		90	180		
Output Impedance	R_{OUT}	At DC		0.01					Ω
Power-Supply Rejection Ratio	PSRR	ΔV_S = ±5%	48	54		47			dB
Nonlinearity (Note 2)		±2V signal	-1.5	±1.0	1.5				mV
		T_A = 0°C to +70°C				-2.0		2.0	
		T_A = -40°C to +85°C				-2.5		2.5	
Supply Voltage (Note 3)	V+, V-		±4.75	±5	±5.25	±4.75	±5	±5.25	V
Supply Current (Note 3)	IQ	V+, V- = ±5V		±35	±40			±43	mA
AC SPECIFICATIONS (NOTE 1)									
-3dB Bandwidth	BW	$V_{IN} = IV_{RMS}$	125	180		110			MHz
Full-Power Bandwidth	FPBW	$V_{OUT} = 6V_{p-p}$	24	34		18			MHz
Slew Rate	SR	V_{OUT} = 3V step	450	650		350			V/µs
Settling Time	t_S	t = 0.1%, V_{OUT} = 3V step		35	50			70	ns
Rise/Fall Time	$t_{R/F}$	V_{OUT} = 3V step		8	12			16	ns
Differential Phase				0.01					°
Differential Gain				0.03					%

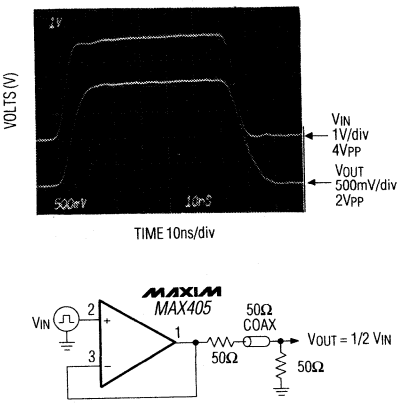
Note 1: Guaranteed by design.
Note 2: Nonlinearity is deviation from end-point line.
Note 3: $V_{C+} = V$, $V_{C-} = V-$. Current is for both supply pins.

Typical Operating Characteristics

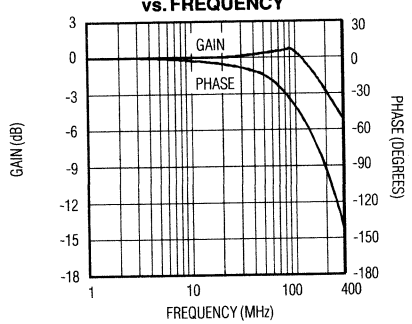
SUPPLY CURRENT vs. SUPPLY VOLTAGE



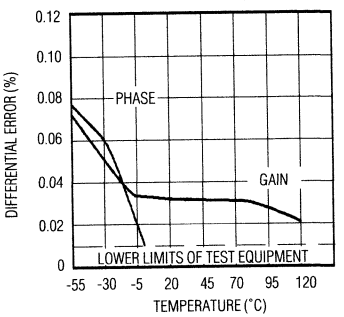
PULSE RESPONSE INTO 50Ω BACK-TERMINATED LOAD



GAIN AND PHASE vs. FREQUENCY



DIFFERENTIAL GAIN AND PHASE ERROR vs. TEMPERATURE



8

Precision Video Buffer Amplifier

Pin Description

PIN	NAME	FUNCTION
1	OUT	Buffer-Amplifier Output
2	IN+	Buffer-Amplifier Noninverting Input
3	IN-	Buffer-Amplifier Inverting Input. For unadjusted operation, connect to OUT. Connect to resistive divider from OUT (Figure 3) to adjust gain to exactly 1.0000V/V. IN- CANNOT be used as a conventional op-amp inverting input (see *Gain Trim* section).
4	V-	Negative Supply. Connect to -5V.
5	NULL	Voltage Offset Adjust. Leave open normally. Connect to arm of 1kΩ potentiometer (Figure 2) to null input offset voltage. One end of the potentiometer should be connected to V+. The other end should be connected to a 9kΩ resistor to V-.
6	V+	Positive Supply. Connect to +5V.
7	VC-	Output Stage (Collector) Negative Supply. Connect to -5V.
8	VC+	Output Stage (Collector) Positive Supply. Connect to +5V.

Detailed Description

Circuit Overview

The main circuit elements of the MAX405 are an input stage and a bipolar output stage with separate power-supply connections (Figure 1). This allows separate bypassing to improve high-frequency response while keeping high-frequency transients in the output stage from feeding back to the input. The MAX405 employs an unusual buffer configuration. The inverting input pin allows the gain to be increased above its initial value. In addition, input offset voltage may be trimmed externally.

Zero-Offset Trim

Offset voltage is the difference between IN+ and OUT when IN+ is 0V. The MAX405 is laser trimmed for offset voltage less than ±5mV. Offset voltage can be further reduced by connecting a 1kΩ trim potentiometer and a 9.1kΩ fixed resistor as shown in Figure 2. This circuit's offset nulling range is approximately ±25mV.

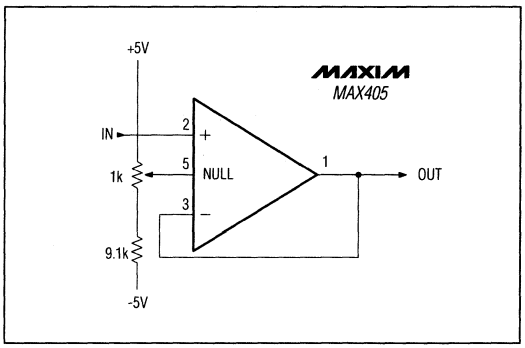


Figure 2. Zero-Offset Trim Circuit

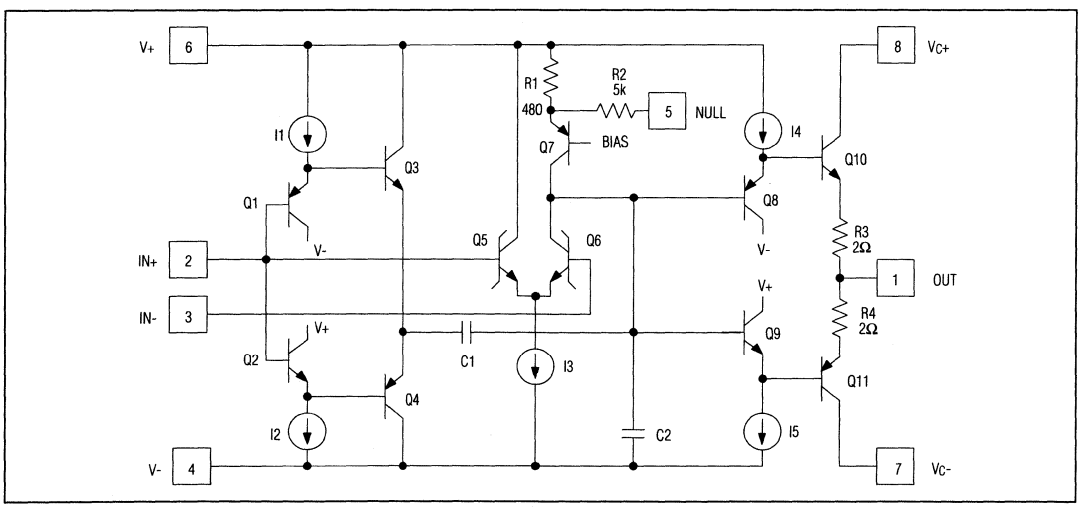


Figure 1. MAX405 Simplified Schematic

Gain Trim

The MAX405 drives 50Ω loads at a 0.9940V/V factory-set gain with no external components.

Unlike other buffer amplifiers, the MAX405 has an inverting input (IN-) that can be connected to an external voltage divider to increase the gain. Figure 3 shows a circuit in which a variable voltage divider trims the buffer to exactly 1.0000V/V. The gain can be adjusted to a maximum of 1.10V/V. Higher gain may produce nonlinearities and instability. Care must be exercised to minimize stray circuit capacitance in the feedback network.

When both offset and gain trims are used, the zero-offset trim should be set first, with 0mV applied to IN+. Next, gain should be adjusted with the full-scale voltage applied to IN+.

Input Capacitance

The MAX405 input capacitance is typically 0.6pF. IN+ is located between the IN- and OUT pins, which are at the same potential. This forms a high-frequency guard for the IN+ pin and minimizes input capacitance. When no gain trim is used, the printed circuit-board layout should include a guard ring (circular trace) around IN+, which is driven from OUT. It should form a complete circle on both sides of the board. The guard ring must be broken on the side of the board that has the input trace, or stretched to enclose the input component solder pad (Figure 4).

Source Impedance

To realize the benefits from the precision MAX405, source impedance must be kept low. Both DC and AC sources contribute errors.

The DC voltage errors are developed from two sources:
1) the input bias current through the source resistance,
2) the voltage divider formed by the source resistance and the finite input resistance (typically 2.5MΩ).

The AC error increases with frequency. It is caused by the action of a lowpass RC filter, consisting of the source (series) resistance and amplifier input (shunt) capacitance (0.6pF).

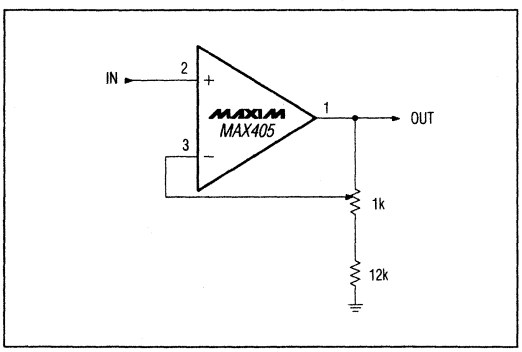


Figure 3. Gain-Trim Circuit

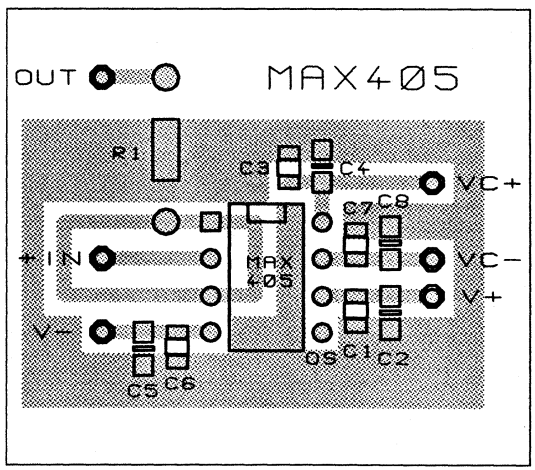


Figure 4. Typical Board Layout (see Typical Application Circuit)

Precision Video Buffer Amplifier

Output Stage

The MAX405 is stable while driving capacitive loads up to 100pF. Figure 5 shows how larger capacitive loads can be driven if they are isolated with a series resistor.

The OUT pin is protected against accidental short circuits. Internal current limiting keeps continuous output current at safe values at room temperature. Typical values of output short-circuit current are 180mA for positive polarity and 150mA for negative polarity when using ±5V supplies. Continuous short-circuit protection at elevated temperatures T_A > 50°C requires additional external circuitry connected to V_{C+} and V_{C-}. Figure 6 shows a typical circuit.

Coaxial Driver

The MAX405 is ideal as a 50Ω and 75Ω coaxial cable driver. With a guaranteed 60mA continuous output current, the MAX405 directly drives ±3V into 50Ω. Common applications include a back-termination resistor to match the cable impedance. The MAX405 is capable of driving up to four 150Ω (four 75Ω back-terminated loads) loads to ±2.25V.

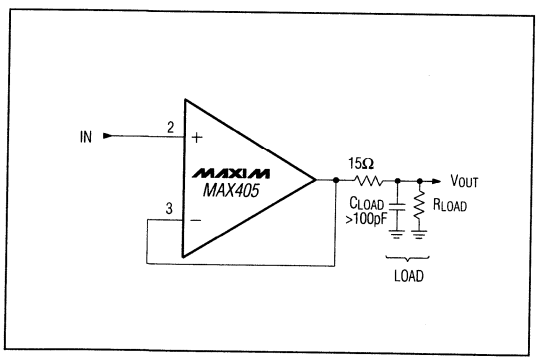


Figure 5. Driving Large Capacitive Loads

Bypassing

Good high-frequency performance demands careful layout, ground planes, and good bypassing. The input and output stages have separate power-supply pins for isolation. Even though the two positive (V+, V_{C+}) and two negative (V-, V_{C-}) supply pins may be connected together, they should have separate bypass capacitors located as close to the pins as possible. Each supply pin should have a 0.1µF ceramic and a 1µF tantalum capacitor connected to ground. Surface-mount chip capacitors (Figure 4) are recommended because they have extremely low impedance at high frequencies.

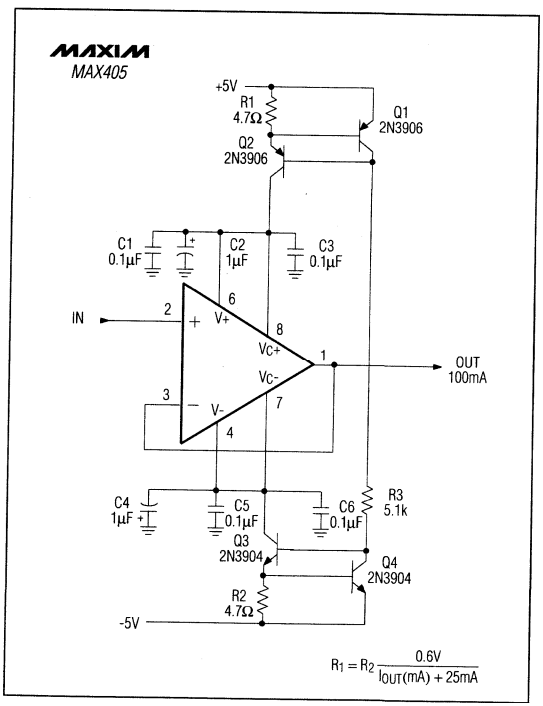
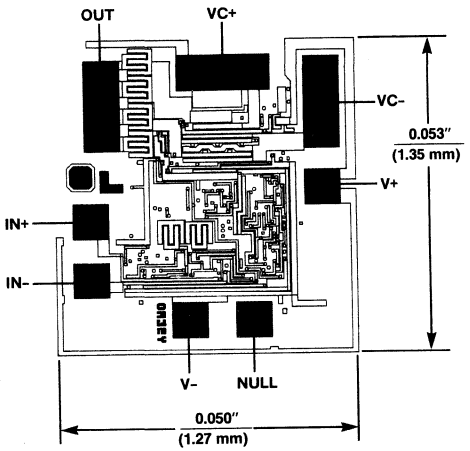


Figure 6. Continuous Output Short-Circuit Protection at Elevated Temperatures (T_A > 50°C)

Chip Topography



MAXIM

CMOS Video Multiplexer/Amplifier

General Description

The MAX452 is a unity-gain stable, 50MHz video amplifier capable of driving a 75 ohm load directly. The MAX453, MAX454, and MAX455 combine the 50MHz video amplifier, of the MAX452, with an on-board multiplexer offering 2, 4, or 8 channels respectively. All of the MAX452 family devices operate from ±5V supplies and typically consume only 250mW.

Optimized for video applications, these amplifiers will directly drive a 150 ohm load to ±2V, and will swing ±1V into a 75 ohm load. All amplifiers are unity-gain stable and do not require external frequency compensation components. The MAX453/454/455 operate as positive-gain amplifiers, gain being set by two external resistors. Since they are connected as non-inverting amplifiers, their minimum closed-loop gain is 0dB. In most applications the amplifier's closed-loop gain will be set at 0dB or +6dB (1 V/V or 2 V/V), which guarantees a minimum bandwidth of 25MHz.

Applications

Video signal multiplexing

75 ohm cable drivers

Driving flash converters

Video Crosspoint Switches

Features

- ◆ **Unity-gain bandwidth of 50MHz typ.**
- ◆ **Low input capacitance: 7pF typ.**
- ◆ **No frequency-compensation required**
- ◆ **Low power operation: 250mW typ.**
- ◆ **Low bias current: 10pA typ.**
- ◆ **Directly drives 75 ohm cable**
- ◆ **70 dB typical OFF isolation at 4 MHz**

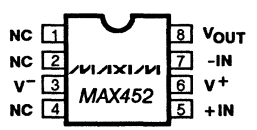
Ordering Information

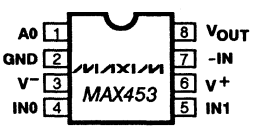
PART	TEMP. RANGE	PACKAGE
MAX452CPA	0°C to +70°C	8 lead plastic DIP
MAX452CSA	0°C to +70°C	8 lead small-outline
MAX452C/D	0°C to +70°C	Dice
MAX452EPA	-40°C to +85°C	8 lead plastic DIP
MAX452EJA	-40°C to +85°C	8 lead CERDIP
MAX452MJA	-55°C to +125°C	8 lead CERDIP
MAX453CPA	0°C to +70°C	8 lead plastic DIP
MAX453CSA	0°C to +70°C	8 lead small-outline
MAX453EPA	-40°C to +85°C	8 lead plastic DIP
MAX453EJA	-40°C to +85°C	8 lead CERDIP
MAX453MJA	-55°C to +125°C	8 lead CERDIP
MAX454CPD	0°C to +70°C	14 lead plastic DIP
MAX454CSD	0°C to +70°C	14 lead small-outline
MAX454EPD	-40°C to +85°C	14 lead plastic DIP
MAX454EJD	-40°C to +85°C	14 lead CERDIP

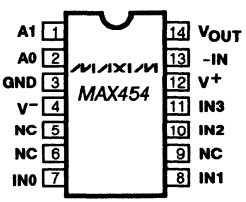
(Ordering Information Continued on Last Page.)

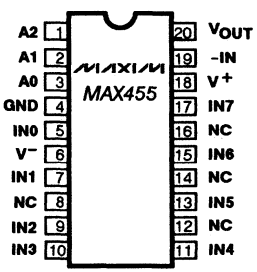
Pin Configurations

Top View









8

CMOS Video Multiplexer/Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 12 V
Positive Supply Voltage, V^+ (rel. GND) ..... +12V
Negative Supply Voltage, V^- (rel. GND) ..... -12V
Analog Input Voltage ..... (V^+) + 0.3 V to (V^-) -0.3 V
Digital Input Voltage ..... -0.3 V to (V^+) + 0.3 V
Storage Temperature Range ..... -65°C to +160°C
Operating Temperature Range
MAX452C,MAX453C,
MAX454C,MAX455C ..... 0°C to +70°C
MAX452E,MAX453E,
MAX454E,MAX455E ..... -40°C to +85°C
MAX452M,MAX453M,
MAX454M,MAX455M ..... -55°C to +125°C

Lead temperature (Soldering, 10 sec) ..... 300°C
Duration of Output Short-Circuit to ground ..... Indefinite
Input Current, power on or off
Digital Inputs ..... +20 mA
All other pins ..... ±50 mA
Continuous Total Power Dissipation (T_A = +70°C)
8 Pin CERDIP (derate 8.0mW/°C above 70°C) 640mW
14 Pin CERDIP (derate 9.5mW/°C above 70°C) 760mW
20 Pin CERDIP (derate 11.1mW/°C above 70°C) 890mW
8 Pin Plastic DIP (derate 8.3mW/°C above 70°C) 660mW
14 Pin Plastic DIP (derate 10.0mW/°C above 70°C) 800mW
20 Pin Plastic DIP (derate 11.1mW/°C above 70°C) 890mW
8 Pin Small-Outline (derate 5.9mW/°C above 70°C) 320mW
14 Pin Small-Outline (derate 8.7mW/°C above 70°C) 480mW
20 Pin Small-Outline (derate 10.0mW/°C above 70°C) 550mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS MAX452/3/4/5

(V^+ = +5V, V^- = -5V, -2V ≤ Vin ≤ +2V, Output Load Resistor = 150Ω, T_A = +25°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
Input Voltage Range	V_{IN}	Over Temperature Range (Note 2)	-2		2	V
Input Offset Voltage	V_{OS}			2	5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(Note 5)		20	100	µV/°C
Input Bias Current	I_B	T_A = +25°C (Note 1)		0.01	10	nA
		Over Temperature Range (Notes 1,2) C		1	10	
		E		3	30	
		M		50	500	
Input Resistance	R_{IN}			10^{11}		Ω
Open-Loop Voltage Gain	A_{VOL}	R_L = 1000Ω	180	260		V/V
		R_L = 150Ω	45	70		
		R_L = 75Ω	25	38		
Open-Loop Gain Drift	$\Delta A_{VOL}/\Delta T$	R_L = 150Ω		0.5		%/°C
Common-Mode Rejection Ratio	CMRR	-2V ≤ V_{IN} ≤ +2V	60	80		dB
Power Supply Rejection Ratio	PSRR	±4.5V to ±5.5V	54	66		dB
Slew Rate	SR	(Note 5)	150	300		V/µs

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.
Note 2: Operating temperature range for "C" devices is 0°C to 70°C, for "E" devices is -40°C to +85°C, and for "M" devices is -55°C to +125°C.
Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.
Note 4: Guaranteed over the voltage range, $V^- < V_{IN} < V^+$.
Note 5: Guaranteed by design.

(Continued on next page)

ELECTRICAL CHARACTERISTICS MAX452/3/4/5 (Continued)

($V^+ = +5V$, $V^- = -5V$, $-2V < Vin < +2V$, Output Load Resistor = 150Ω, $T_A = +25°C$ unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
-3dB Bandwidth	GBW1	$A_V = 0dB$, $R_L = 75Ω$ (Note 5)	30	50		MHz
-3dB Bandwidth	GBW2	$A_V = 6dB$, $R_L = 150Ω$ (Note 5)	25	40		MHz
Differential Phase Error	DP	MAX452 (Notes 3, 5) MAX453/4/5 (Notes 3, 5)		0.2 1.2		deg
Differential Gain Error	DG	(Notes 3, 5)		0.5		%
Settling-Time to 1%	t_S	$\Delta V = 1V$, $R_L = 150Ω$, $A_V = 6dB$		50		ns
Output Impedance	R_{OUT}	$f = 100kHz$, $A_V = 0dB$		2		Ω
Full-Scale Output Current	I_{OUT}	$R_L = 150Ω$	±14	±20		mA
Output Voltage Swing	V_{OUT}	$R_L = 150Ω$	±2.1	±3.0		V
Input Noise, dc to 40MHz	Vn	(Note 5)		0.15	0.5	mV_{rms}
Operating Supply Voltage	V^+, V^-		±4.5		±5.5	V
Supply Current	I_S	$V_{IN} = 0V$	20	25	30	mA
MULTIPLEXER (MAX453/4/5)						
Input Voltage Range	V_{IN}	Over Temperature	-2		2	V
OFF Input Leakage Current	I_{OFF}	$T_A = +25°C$ (Note 4) Over Temperature C Range (Notes 2, 4) E M		0.01 1 3 50	10 10 30 500	nA
Logic Low Threshold	V_{IL}				0.8	V
Logic High Threshold	V_{IH}		2.4			V
Input Pullup/down Current	$I_{IL/IH}$			5	20	µA
Turn-ON Time	t_{ON}	(Note 5)		75	120	ns
Turn-OFF Time	t_{OFF}	(Note 5)		25	60	ns
Break-Before-Make Delay	t_D	(Note 5)	10	50		ns
Channel "ON" Capacitance	C_{ON}	(Note 5)		7	15	pF
Channel "OFF" Capacitance	C_{OFF}	(Note 5)		3.5	12	pF
Channel "OFF" Isolation	OIRR	$f_{IN} = 4MHz$, $R_S = 75Ω$ (Note 5) Channel 2 to Channel 3 All other Channels	45 60	55 70		dB

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.

Note 2: Operating temperature range for "C" devices is 0°C to 70°C, for "E" devices is -40°C to +85°C, and for "M" devices is -55°C to +125°C.

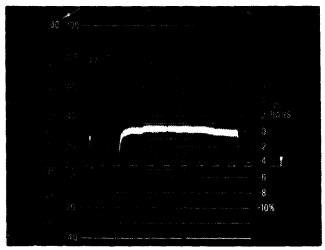
Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

Note 4: Guaranteed over the voltage range, $V^- < V_{IN} < V^+$.

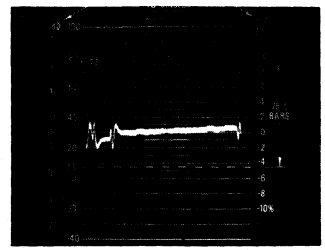
Note 5: Guaranteed by design.

CMOS Video Multiplexer/Amplifier

MAX452 AND MAX455 DIFFERENTIAL GAIN

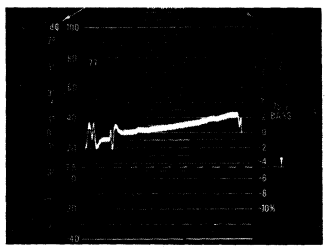


MAX452 DIFFERENTIAL PHASE

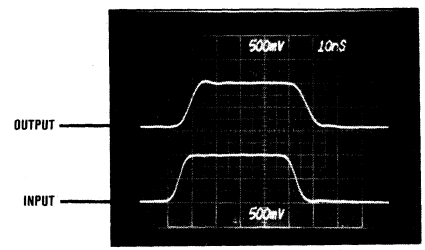


Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

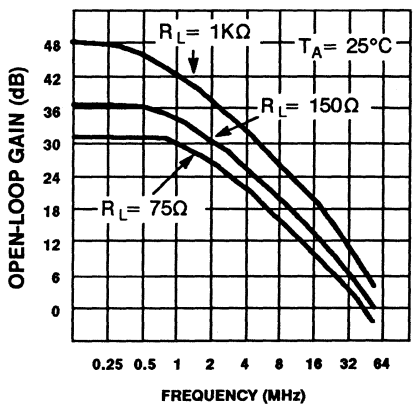
MAX455 DIFFERENTIAL PHASE



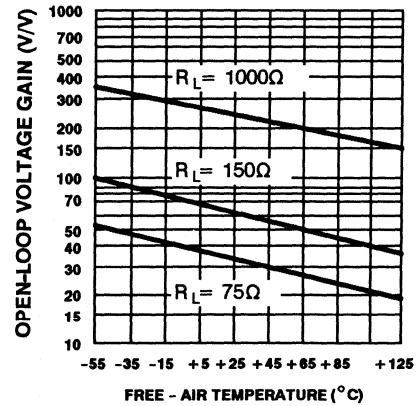
MAX455 PULSE RESPONSE



OPEN-LOOP GAIN vs. FREQUENCY



OPEN-LOOP GAIN vs. TEMPERATURE



Pin Description

PIN NAME	PIN NUMBER				FUNCTION
	MAX452	MAX453	MAX454	MAX455	
V^+	6	6	12	18	Positive Supply, +5V
V^-	3	3	4	6	Negative Supply, -5V
V_{OUT}	8	8	14	20	Amplifier output
-IN	7	7	13	19	Amplifier's inverting input
+IN	5	-	-	-	Amplifier's non-inv. input
IN0	-	4	7	5	Analog input, channel 0
IN1	-	5	8	7	Analog input, channel 1
IN2	-	-	10	9	Analog input, channel 2
IN3	-	-	11	10	Analog input, channel 3
IN4	-	-	-	11	Analog input, channel 4
IN5	-	-	-	13	Analog input, channel 5
IN6	-	-	-	15	Analog input, channel 6
IN7	-	-	-	17	Analog input, channel 7
A2	-	-	-	1	Channel select, MSB
A1	-	-	1	2	Channel select
A0	-	1	2	3	Channel select, LSB
GND	-	2	3	4	Logic Ground

Detailed Description

The video amplifier is a low gain, wideband op-amp optimized for driving low impedance loads. Open-loop gain is about 40V/V with a 75 ohm load which introduces a small gain error. However, this can readily be trimmed by adjusting the gain-setting resistors.

The MAX452/3/4/5 series are unity-gain stable when driving resistive loads. They are optimized for driving 75 ohms at unity gain or 150 ohms at a gain of 2V/V with no frequency compensation components required. Generally, for the best transient response, the load resistance should be (in ohms) 75 x GAIN(V/V). Thus, at a gain of +6dB (2V/V), the amplifier's optimal load is 150 ohms. If a higher resistive load is used, the amplifier will show peaking near its -3dB frequency. If a capacitive load is being driven, such as the input to a flash converter, the load should be "isolated" by a series resistor to limit amplifier ringing, see Figure 4.

The bandwidth of the amplifier is affected by both the closed-loop gain and the load resistor. Table 1 lists the -3dB rolloff frequency for a MAX453/4/5 with different gains and optimal resistive loads. The MAX452, which doesn't have the input multiplexer, runs about 20% higher in bandwidth.

Table 1.
Gain and Load Resistor Selection

GAIN (V/V)	f-3dB (MHz)	R1 (Ω)	R2 (Ω)	R_{load} (Ω)
1	50	0	∞	75
2	40	1k	1k	150
5	30	4k	1k	390
10	18	9k	1k	750

The multiplexers feature break-before-make switches to insure that no two channels are ever connected together. Low DC offset voltage and high bandwidth allow the MAX455 to be cascaded to form a 64 channel system while retaining video signal fidelity.

Figure 1 shows a typical application of the MAX455. The circuit is being used to drive a back terminated 75 ohm cable. R3 and R4 terminate the cable at both ends. R3 also attenuates the signal by a factor of two, so to make up for the signal loss, the amplifier is run at a gain of 2V/V. This arrangement provides unity gain from signal input to

CMOS Video Multiplexer/Amplifier

cable output. Amplifier closed-loop gain is set by R1 and R2 giving,

$$\frac{V_{OUT}}{V_{IN}} = \frac{G \times (R1 + R2)}{(G \times R2) + (R1 + R2)}$$

Where G is the open-loop gain of the amplifier, about 70V/V with a 150 ohm load. Capacitors C1 and C2 are power supply bypass capacitors.

Multiplexer channels are selected by the A0, A1, and A2 pins. These logic pins are compatible with either TTL or CMOS logic. The GND pin (which is a logic ground, NOT an analog ground) should be connected to digital ground. Table 2 shows selected channels for the different states of the control lines. If A0, A1, and A2 are left floating, internal pullup/pulldown sources will hold A0 and A1 low, and A2 high. Thus, channel 0 is the default channel for the MAX453 and MAX454, while channel 4 is the default channel for the MAX455. Pullup/pulldown currents are typically around 5µA.

Table 2.
Channel Selection

MAX453		MAX454			MAX455			
A0	Channel	A1	A0	Channel	A2	A1	A0	Channel
L	0*	L	L	0*	L	L	L	0
H	1	L	H	1	L	L	H	1
		H	L	2	L	H	L	2
		H	H	3	L	H	H	3
					H	L	L	4*
					H	L	H	5
					H	H	L	6
					H	H	H	7

*Default channel if selection pins are left floating.

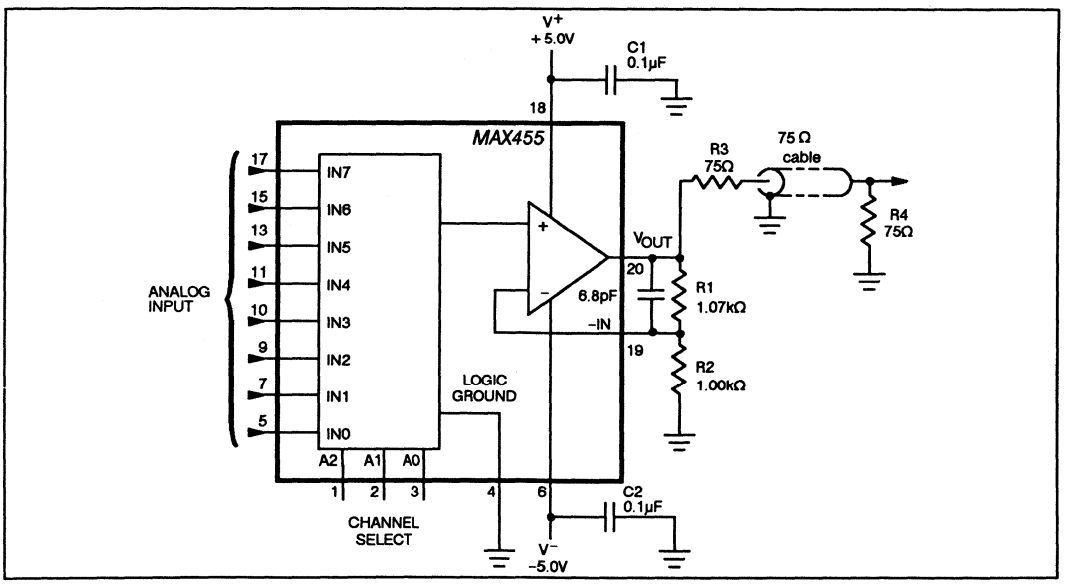


Figure 1. Typical Application

Typical Applications

Figure 2 shows the connections for a unity-gain amplifier. R1 and R2 adjust the gain to be nominally 1.00V/V. R3 is a 75 ohm load resistor. If precise unity-gain is not needed, R1 and R2 can be omitted and -IN can be connected directly to V_{OUT}.

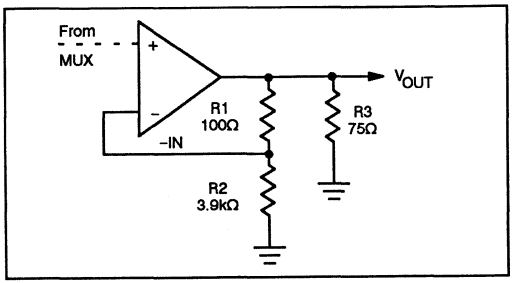


Figure 2. Unity-Gain Connections

Figure 3 shows how 64 channels can be multiplexed together. Eight MAX455s select 8 out of 64 channels, and a final MAX455 selects one of the 8 intermediate channels. The first eight MAX455s are connected as unity-gain amplifiers with 150 ohm load resistors. This results in a voltage gain of about 0.99V/V. The 150 ohm loads will also cause these unity-gain amplifiers to peak around 40MHz which tends to cancel the rolloff of the final amplifier running at a gain of 2V/V. The overall gain is adjusted by R1. The -3dB frequency is about 35MHz.

Figure 4 shows the amplifier driving a capacitive load. The 27 ohm resistor provides isolation between the capacitive load and the amplifier output. This minimizes signal peaking at high frequencies. As a rule, the resistor should be chosen such that the RC product is 10ns or longer. This scheme shouldn't be used if R is greater than 150 ohms (or C is less than 100pF). The amplifier can drive 100pF directly without an isolation resistor.

The video amplifier is similar to a transconductance amplifier in that the output is a current proportional to the difference of the input voltage and the feedback voltage. Gm is about 0.5 mA/mV. The output impedance of the amplifier is around 1k ohms. This gives an unloaded voltage gain of,

$$Gm \times Ro = 500\ V/V$$

or about 54 dB.

Video signals are often of one polarity, e.g., ranging from 0 to +1V full scale. When amplifying these signals, phase distortion can be reduced by biasing the output stage of the video amplifier as shown in Figure 5. Here a signal is driven 0 to +2V into a 150 ohm load. R2 provides 6.5 mA of drive to the load at mid scale (1V). The amplifier, instead of supplying 0 to 13mA, supplies a more symmetric ±8mA which reduces phase distortion to about 1 degree at 4 MHz. Because of the amplifier's finite gain of 0.5mA/mV, the current from R2 introduces an offset voltage. Adding R1 compensates for this offset. R3 and R4 set the closed-loop gain of the amplifier.

Care should be taken in laying out the printed circuit board connections to minimize cross-talk between channels. This can be augmented by using ground traces between the signal paths.

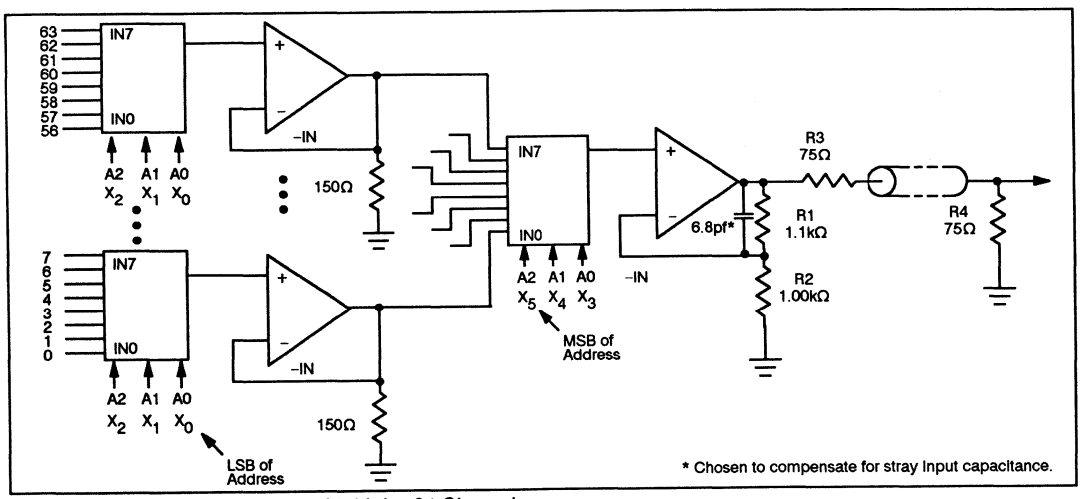


Figure 3. Nine MAX455s Used to Multiplex 64 Channels.

CMOS Video Multiplexer/Amplifier

Power supply voltages should be maintained to within ± 5% of the nominal ± 5.00V values for optimum performance.

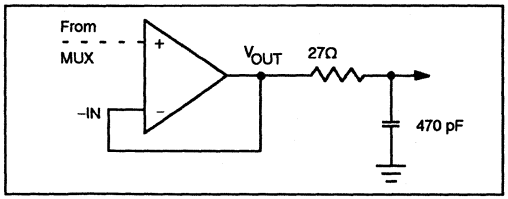


Figure 4. Isolating a Large Capacitive Load.

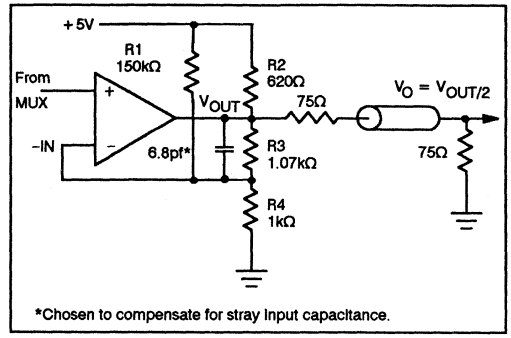
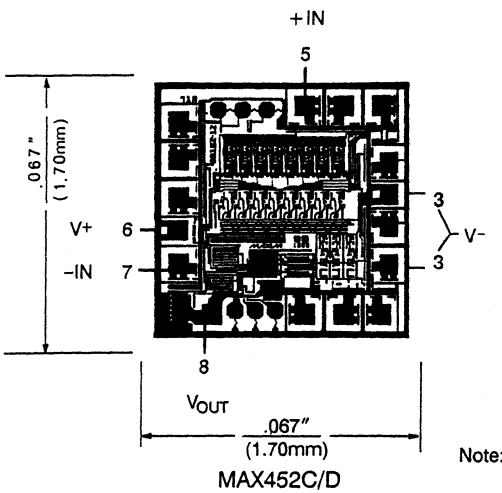


Figure 5. Minimizing Phase Distortion

Ordering Information (continued)

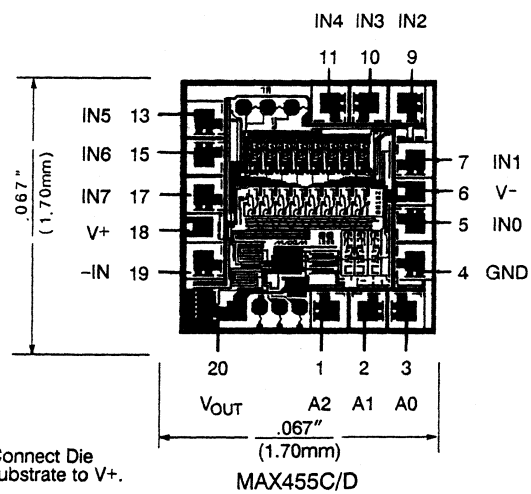
PART	TEMP. RANGE	PACKAGE
MAX454MJD	-55°C to +125°C	14 lead CERDIP
MAX455CPP	0°C to + 70°C	20 lead plastic DIP
MAX455CWP	0°C to + 70°C	20 lead small-outline
MAX455C/D	0°C to + 70°C	Dice
MAX455EPP	-40°C to +85°C	20 lead plastic DIP
MAX455EJP	-40°C to +85°C	20 lead CERDIP
MAX455MJP	-55°C to +125°C	20 lead CERDIP

Chip Topographies



MAX452C/D

Note: Connect Die Substrate to V+.



MAX455C/D

ADVANCE INFORMATION
FIRST PAGE OF DATA SHEET IN PREPARATION

MAXIM
Crosspoint Video Switch

General Description

The MAX456 features a 64 T-switch matrix arranged for 8 input channels and 8 output channels. Each of the 8 matrix outputs drives an internal video amplifier that is capable of driving a load of 400Ω and 20pF to ±1.2V. Configuration data is entered into the MAX456 by a 7-bit parallel word, a 7-bit serial word, or a 32-bit serial stream. This data controls the T-switches, which allow each of the 8 output channels to be connected to any one of the 8 input analog channels.

The MAX456 pin out is arranged in a straight-through architecture. The analog inputs are on one side, and the outputs are on the other side with either a power-supply line or a "quiet" digital logic line positioned between each channel to minimize crosstalk. Furthermore, the outputs line up with 4 MAX457s (dual-video amplifiers), which drive 75Ω cables.

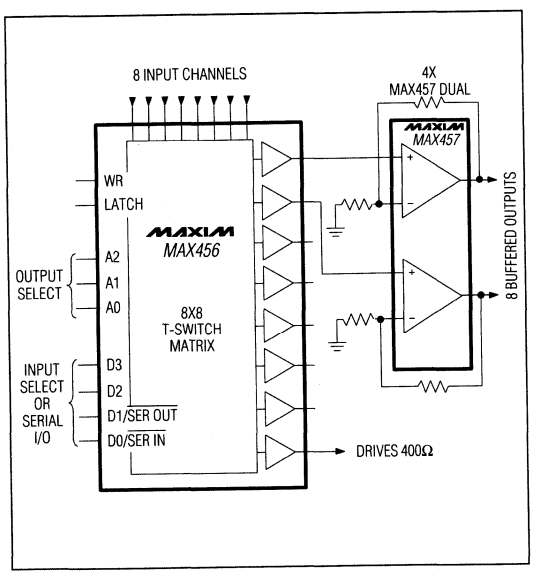
Features

- ♦ **Programmability**
- ♦ **3 Interface Modes - Serial or Parallel Digital Interface**
- ♦ **250V/µs Slew Rate**
- ♦ **Internal 400Ω Load Terminations**
- ♦ **0.3° Diff. Phase**
- ♦ **60dB Off Isolation at 5MHz**

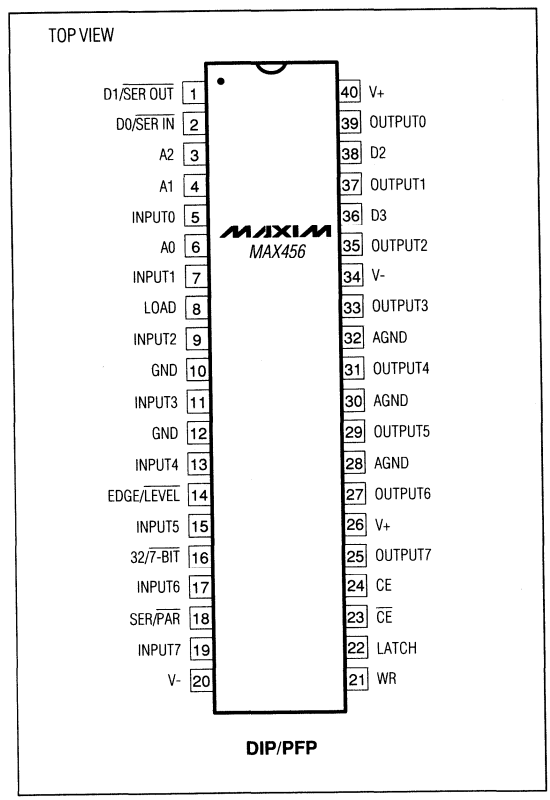
Applications

Video Test Equipment
Video Security Systems
Video Editing

Functional Diagram



Pin Configuration



DIP/PFP

MAXIM

Dual CMOS Video Amplifier

General Description

The MAX457 contains two unity-gain stable video amplifiers that are capable of driving 75Ω loads with a -3dB bandwidth of 70MHz. The amplifiers operate from ±5V supplies and together consume about 350mW of power. Closed loop gain is set by two external resistors. The pinout of the MAX457 follows that of conventional 8-pin, dual op amps.

The amplifiers require no external compensation and because of the CMOS process offer low input bias current of typically 100pA. The isolation between the amplifiers is typically 72dB at 5MHz and differential phase and gain are 0.2 degrees and 0.5% respectively.

Features

- **Unity-Gain Bandwidth of 70MHz**
- **Low Input Capacitance: 4pF**
- **No Frequency Compensation Required**
- **Low Input Bias Current: 100pA**
- **Directly Drives 75Ω Cables**
- **High Isolation Between Amplifiers: 72dB at 5MHz**
- **Low Offset Voltage: 2mV**

Applications

75Ω Cable Drivers

Output Amplifiers for Video Crosspoint Switches

High Speed, Low Gain Applications

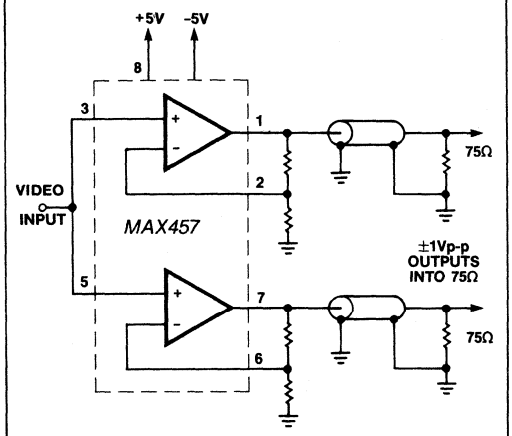
Driving Flash Converters

Video Distribution Amplifiers

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX457CPA	0°C to +70°C	8 Lead Plastic DIP
MAX457CSA	0°C to +70°C	8 Lead SO
MAX457C/D	0°C to +70°C	Dice
MAX457EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX457EJA	-40°C to +85°C	8 Lead CERDIP

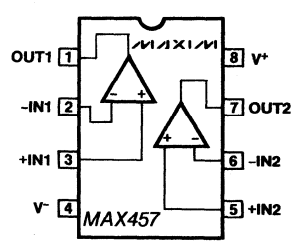
Typical Operating Circuit



MAX457 Dual Video 70MHz Distribution Amplifier

Pin Configuration

Top View



Dual CMOS Video Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 12V
Analog Input Voltage ..... (V^+ +0.3V) to (V^- -0.3V)
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
MAX457CPA, MAX457CSA,
MAX457C/D ..... 0°C to +70°C
MAX457EPA, MAX457EJA ..... -40°C to +85°C

Lead temperature (Soldering 10 sec) ..... +300°C
Duration of Output Short Circuit to Ground ... Indefinite
Input Current, power on or off ..... ±50mA
Continuous Total Power Dissipation at 70°C
Plastic DIP (derate 8.3mW/°C above 70°C) 660mW
CERDIP (derate 8.0mW/°C above 70°C) 640mW
Small Outline (derate 5.9mW/°C above 70°C) ... 470mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

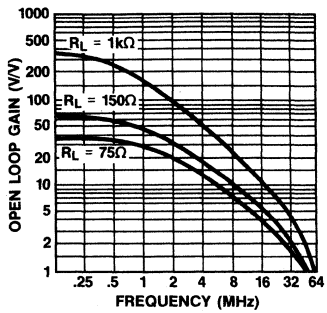
(V^+ = +5V, V^- = -5V, -2V ≤ V_{IN} ≤ +2V, Output Load Resistor = 150Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Over Temperature Range	-2		+2	V
Input Offset Voltage	V_{OS}		-5	±2	+5	mV
Offset Voltage Drift	dV_{OS}/dT			20	100	µV/°C
Input Bias Current	I_B	T_A = +25°C T_A = +70°C T_A = +85°C		0.1 5 15	1 40 100	nA
Input Resistance	R_{IN}	T_A = +25°C		10		GΩ
Input Capacitance	C_{IN}	Plastic Package		4		pF
Open Loop Voltage Gain	A_{VOL}	R_L = 1000Ω R_L = 150Ω R_L = 75Ω	200 45 25	300 65 35		V/V
Open Loop Gain Drift Temperature Coefficient	dA_{VOL}/dT	R_L = 150Ω		-0.6		%/°C
Common Mode Rejection Ratio	CMRR	-2V ≤ V_{IN} ≤ +2V	54	66		dB
Power Supply Rejection Ratio	PSRR	±4.5V to ±5.5V	54	66		dB
Slew Rate	SR	(Note 1)	150	300		V/µs
-3dB Bandwidth	GBW1	A_V = 0dB, R_L = 75Ω (Note 1)	50	70		MHz
-3dB Bandwidth	GBW2	A_V = 6dB, R_L = 150Ω (Note 1)	35	50		MHz
Differential Phase Error	DP	(Notes 1, 2)		0.2		deg
Differential Gain Error	DG	(Notes 1, 2)		0.5		%
Settling Time to 1%	t_S	R_L = 150Ω, A_V = 6dB		50		ns
Output Impedance	R_{OUT}	f = 100kHz, A_V = 0dB		2		Ω
Full Scale Output Current	I_{OUT}	R_L = 150Ω	±15	±20		mA
Output Voltage Swing	V_{OUT}	R_L = 150Ω	±2.1	±2.5		V
Input Noise, DC to 50MHz	V_N	(Note 1)		0.15	0.5	mV_{RMS}
Isolation Between Amplifiers	ISOL	f = 5MHz (Note 1)	60	72		dB
Operating Supply Voltage	V^+, V^-		±4.5		±5.5	V
Supply Current	I_S	T_A = +25°C T_A = +85°C Both Amplifiers	30 34	35 39	42 50	mA

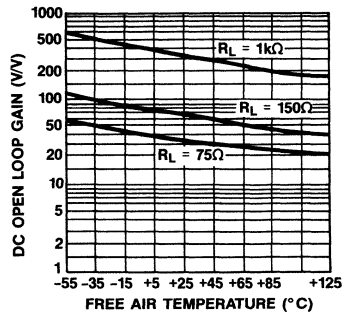
Note 1: Guaranteed by design.
Note 2: Input test signal: 3.58MHz sine wave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150Ω load. 140 IRE = 1.0V.

Typical Operating Characteristics

OPEN LOOP GAIN vs FREQUENCY



DC OPEN LOOP GAIN vs TEMPERATURE



Detailed Description

The MAX457's dual video amplifiers are similar in design to the MAX452 single video amplifier, however, improvements have been made in gain linearity and bandwidth. The MAX457 video amplifier is similar to a transconductance amplifier that has an output current proportional to the difference of the voltages at the input terminals. That is,

$$I_{OUT} = Gm \times [(V_{IN}^{+}) - (V_{IN}^{-})]$$

where Gm is about 0.6 amps/V. The output impedance of the amplifier is about 1.1kΩ. This gives an unloaded voltage gain of Gm × R_{OUT} = 660V/V. This open loop gain is drastically reduced when driving conventional loads of 75 or 150Ω.

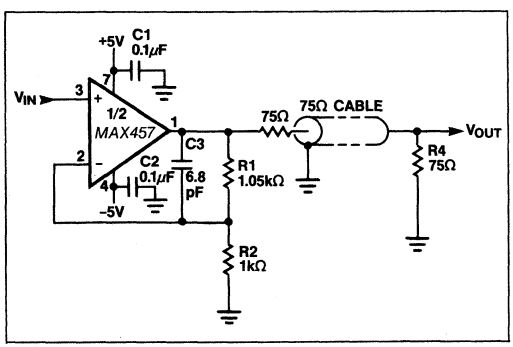


Figure 1. Typical Application

Figure 1 shows a typical application of one of the amplifiers of a MAX457 being used to drive a doubly terminated 75Ω cable. The closed loop gain of the amplifier is 2.00V/V. R1 is 1.05kΩ instead of 1kΩ to make up for the low open loop gain of the MAX457. R1 can be calculated from the following equation:

$$R1 = [(AG + A - G)/(G - A)] \times R2$$

where A is the closed loop gain of the amplifier, and G is the open loop gain of the amplifier (approximately equal to Gm × R_{LOAD}). In this particular example, Gm is 0.6, R_{LOAD} is about 124Ω [(R_{OUT} paralleled with (R1 + R2) paralleled with 150Ω load)], and R2 is 1kΩ. Thus, G is 0.6 × 124 = 74.4V/V, and A is 2V/V (the targeted closed loop gain value). This gives a value of 1.05kΩ for R1. C1 and C2 are power supply bypass capacitors. C3 helps prevent peaking at high frequencies. This peaking results from the input capacitance of the amplifier which is driven by the relatively high impedance of the feedback resistors, R1 and R2. At 50MHz, the feedback resistors cause a substantial phase delay. Adding C3 eliminates this delay. At higher closed loop gains (about 5V/V or more), C3 serves little purpose and should be omitted.

The MAX457 is unity gain stable when driving a 75Ω load. To insure that the amplifier doesn't oscillate, the load resistor should be nominally 75 × A_{VCL}, where A_{VCL} is the closed loop gain of the amplifier. Following this rule will result in a minimum amount of ringing or overshoot. Higher values may be used, but peaking of the output signal may occur in the 30 to 60MHz range. It is generally safe to use loads less than 150 × A_{VCL}. Table 1 gives suggested loads for various closed loop gains. R2 is arbitrarily chosen to be 1kΩ. R1 is calculated to give the nominal closed loop gain with the specified load. Note that the gain-bandwidth product increases as R_{LOAD} increases.

Table 1. Gain and Load Resistor Selection

GAIN (V/V)	f-3dB (MHz)	R1 (Ω)	R2 (Ω)	R_{load} (Ω)
1	70	39	1000	75
2	50	1050	1000	150
5	40	4170	1000	390
10	25	9420	1000	750

Dual CMOS Video Amplifier

If the MAX457 is used to drive a capacitive load, such as the input to a flash converter, the load capacitance should be isolated by a series resistor to limit amplifier ringing. Figure 2 shows how this is done. As a rule, the resistor should be chosen such that the RC product is 10ns or longer. This scheme needn't be used if C_{LOAD} is less than 100pF.

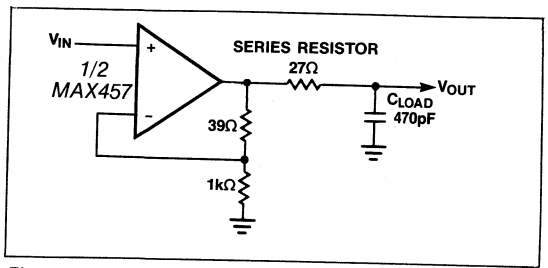
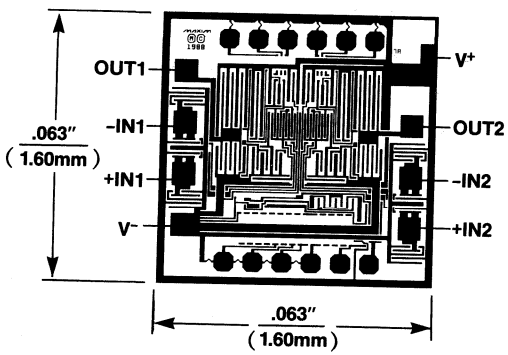


Figure 2. Isolating a Capacitive Load

Chip Topography



19-2887; Rev. 2; 7/91

MAXIM

High-Speed, Low-Power Voltage Comparators

General Description

The MAX900-903 high-speed, low-power, single/dual/quad voltage comparators feature differential analog inputs and TTL logic outputs with active internal pull-ups. Fast propagation delay (8ns typ at 5mV overdrive) makes the MAX900-903 ideal for fast A/D converters and sampling circuits, line receivers, V/F converters, and many other data-discrimination applications.

All comparators can be powered from separate analog and digital power supplies or from a single combined supply voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. The MAX900-903 consume 18mW per comparator when powered from +5V.

The MAX900-903 are equipped with independent TTL compatible latch inputs. The comparator output states are held when the latch inputs are driven low. The MAX901 provides the same performance as the MAX900, MAX902, and MAX903 with the exception of the latches.

Applications

High-Speed A/D Converters
High-Speed V/F Converters
Line Receivers
Threshold Detectors
Input Trigger Circuitry
High-Speed Data Sampling
PWM Circuits

Features

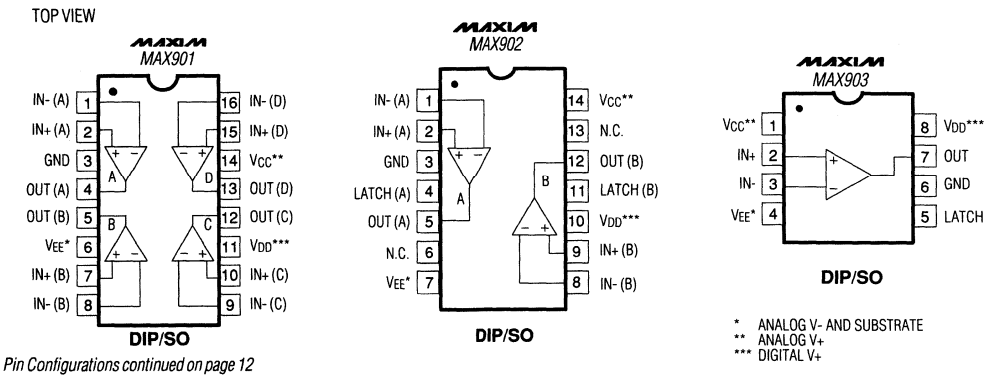
- ♦ **8ns Typ Propagation Delay**
- ♦ **18mW/Comparator Power Consumption (Typ at +5V)**
- ♦ **Separate Analog and Digital Supplies**
- ♦ **Flexible Analog Supply: +5V to +10V or ±5V**
- ♦ **Input Range Includes Negative Supply Rail**
- ♦ **TTL Compatible Outputs**
- ♦ **TTL Compatible Latch Inputs (Except MAX901)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX900ACPP	0°C to +70°C	20 Plastic DIP
MAX900BCPP	0°C to +70°C	20 Plastic DIP
MAX900ACWP	0°C to +70°C	20 Wide SO
MAX900BCWP	0°C to +70°C	20 Wide SO
MAX900BC/D	0°C to +70°C	Dice*
MAX900AEPP	-40°C to +85°C	20 Plastic DIP
MAX900BEPP	-40°C to +85°C	20 Plastic DIP
MAX900AEWP	-40°C to +85°C	20 Wide SO
MAX900BEWP	-40°C to +85°C	20 Wide SO
MAX900AMJP	-55°C to +125°C	20 CERDIP
MAX900BMJP	-55°C to +125°C	20 CERDIP

Ordering information continued on page 11.
* *Contact factory for dice specifications.*

Pin Configurations



Pin Configurations continued on page 12

High-Speed, Low-Power Voltage Comparators

ABSOLUTE MAXIMUM RATINGS (Note 1)

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{DD} to GND) ..... +7V
Differential Input Voltage ..... [V_{EE}-0.2V] to [V_{CC}+0.2V]
Common-Mode Input Voltage ..... [V_{EE}-0.2V] to [V_{CC}+0.2V]
Latch Input Voltage (MAX900/902/903 only) -0.2V to [V_{DD}+0.2V]
Output Short-Circuit Duration
to GND ..... Indefinite
to V_{DD} ..... 1 min
Internal Power Dissipation 500mW
Derate above +100°C ..... 10mW/°C

Operating Temperature Ranges:
MAX900-903_C_ _ ..... 0°C to +70°C
MAX900-903_E_ _ ..... -40°C to +85°C
MAX900-903_M_ _ ..... -55°C to +125°C
Junction Temperature (Tj) ..... -65°C to +160°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	V_{CM} = 0V, V_O = 1.4V		0.5	1.0		1.0	4.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}		3	6		4	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V		50	250		100	500	nA
Input Voltage Range	V_{CM}	(Note 2)	V_{EE}-0.1		V_{CC}-2.25	V_{EE}-0.1		V_{CC}-2.25	V
Common-Mode Rejection Ratio	CMRR	-5V<V_{CM}<+2.75, V_O = 1.4V (Note 3)		50	150		75	250	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)		50	150		100	250	µV/V
Output High Voltage	V_{OH}	V_{IN}>250mV, I_{SRC} = 1mA	2.4	3.5		2.4	3.5		V
Output Low Voltage	V_{OL}	V_{IN}>250mV, I_{SINK} = 8mA		0.3	0.4		0.3	0.4	V
Latch Input Voltage High	V_{LH}	(Note 4)		1.4	2.0		1.4	2.0	V
Latch Input Voltage Low	V_{LL}	(Note 4)	0.8	1.4		0.8	1.4		V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V (Note 4)		1	20		1	20	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V (Note 4)		1	20		1	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Analog Supply Current	I_{CC}	(Note 8)		10	15		5	8		2.5	4	mA
Negative Analog Supply Current	I_{EE}	(Note 8)		7	12		3.5	6		2	3	mA
Digital Supply Current	I_{DD}	(Note 8)		4	6		2	3		1	1.5	mA
Power Dissipation	P_D	V_{CC} = V_{DD} = +5V, V_{EE} = 0V		70	105		35	55		18	28	mW

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input-to-Output High Response Time	t_{pd+}	V_{OD} = 5mV, C_L = 15pF, I_O = 2mA (Note 5)		8	10		8	10		8	10	ns
Input-to-Output Low Response Time	t_{pd-}	V_{OD} = 5mV, C_L = 15pF, I_O = 2mA (Note 5)		8	10		8	10		8	10	ns
Difference in Response Time Between Outputs	Δt_{pd}	(Notes 5, 6)		0.5	2.0		0.5	2.0		0.5	2.0	ns
Latch Disable to Output High Delay	$t_{pd+}(D)$	(Notes 4, 7)		10			10			10		ns
Latch Disable to Output Low Delay	$t_{pd-}(D)$	(Notes 4, 7)		12			12			12		ns
Minimum Setup Time	t_s	(Notes 4, 7)		2			2			2		ns
Minimum Hold Time	t_h	(Notes 4, 7)		1			1			1		ns
Minimum Latch Disable Pulse Width	$t_{pw}(D)$	(Notes 4, 7)		10			10			10		ns

Note 2: The input common-mode voltage and input signal voltages should not be allowed to go negative by more than 0.2V below V_{EE}. The upper end of the common-mode voltage range is typically V_{CC}-2V, but either or both inputs can go to a maximum of V_{CC}+0.2V without damage.

Note 3: Tested for +4.75V<V_{CC}<+5.25V, and -5.25V<V_{EE}<-4.75V with V_{DD} = +5V, although permissible analog power-supply range is +4.75V<V_{CC}<+10.5V for single-supply operation with V_{EE} grounded.

Note 4: Specification does not apply to MAX901.

Note 5: Guaranteed by design. Times are for 100mV step inputs (see propagation delay characteristics in Figures 2 and 3).

Note 6: Maximum difference in propagation delay between any of the four comparators in the MAX900/901/902/903.

Note 7: See Timing Diagram (Figure 2). Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in a production environment. Typical specifications listed are taken from measurements using a high-speed test-jig.

Note 8: I_{CC} tested for +4.75V<V_{CC}<+10.5V with V_{EE} grounded. I_{EE} tested for -5.25V<V_{EE}<-4.75V with V_{CC} = +5V. I_{DD} tested for +4.75V<V_{DD}<+5.25V with the worst-case condition of all four comparator outputs at logic low.

High-Speed, Low-Power Voltage Comparators

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High; T_A = Full Operating Temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	V_{CM} = 0V, V_O = 1.4V		1	2		2	6	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}		4	10		6	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V		100	500		200	800	nA
Input Voltage Range	V_{CM}	(Note 2)	V_{EE}-0.1		V_{CC}-2.25	V_{EE}-0.1		V_{CC}-2.25	V
Common-Mode Rejection Ratio	CMRR	-5V<V_{CM}<+2.75V, V_O = 1.4V (Note 3)		80	250		120	500	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)		100	250		150	500	µV/V
Output High Voltage	V_{OH}	V_{IN}>250mV, I_{SRC} = 1mA	2.4	3.5		2.4	3.5		V
Output Low Voltage	V_{OL}	V_{IN}>250mV, I_{SINK} = 8mA		0.3	0.4		0.3	0.4	V
Latch Input Voltage High	V_{LH}	(Note 8)		1.4	2.0		1.4	2.0	V
Latch Input Voltage Low	V_{LL}	(Note 8)	0.8	1.4		0.8	1.4		V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V (Note 8)		2	20		1	20	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V (Note 8)		2	20		1	20	µA

PARAMETER	SYMBOL	CONDITIONS	MAX900A/MAX901A MAX900B/MAX901B			MAX902			MAX903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Analog Supply Current	I_{CC}	(Note 8)		10	25		5	12		2.5	6	mA
Negative Analog Supply Current	I_{EE}	(Note 8)		7	20		3.5	10		2	5	mA
Digital Supply Current	I_{DD}	(Note 8)		4	10		2	5		1	2.5	mA
Power Dissipation	P_D	V_{CC} = V_{DD} = +5V, V_{EE} = 0V		70	105		35	55		18	28	mW

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, LE1-LE4 = Logic High, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX900A/901A			MAX900B/901B/902/903			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input-to-Output High Response Time	t_{pd+}	V_{OD} = 5mV C_L = 15pF I_O = 2mA (Note 5)		10	15		10	15	ns
Input-to-Output Low Response Time	t_{pd-}	V_{OD} = 5mV C_L = 15pF I_O = 2mA (Note 5)		10	15		10	15	ns
Difference in Response Time Between Outputs	Δt_{pd}	(Notes 5, 6)		1	3		1	3	ns

Note 2: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.2V below V_{EE}. The upper end of the common-mode voltage range is typically V_{CC}-2.0V, but either or both inputs can go to a maximum of V_{CC}+0.2V without damage.

Note 3: Tested for +4.75V<V_{CC}<+5.25V, and -5.25V<V_{EE}<-4.75V with V_{DD} = +5V, although permissible analog power-supply range is +4.75V<V_{CC}<+10.5V for single-supply operation with V_{EE} grounded.

Note 4: Specification does not apply to MAX901.

Note 5: Guaranteed by design. Times are for 100mV step inputs (see propagation delay characteristics in Figures 2 and 3).

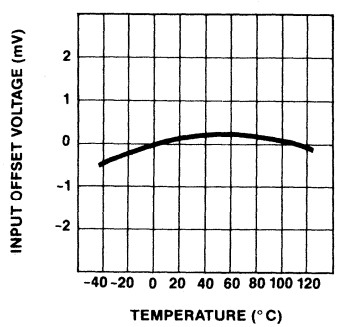
Note 6: Maximum difference in propagation delay between any of the four comparators in the MAX900/901/902/903.

Note 7: See Timing Diagram (Figure 2). Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in a production environment. Typical specifications listed are taken from measurements using a high-speed test-jig.

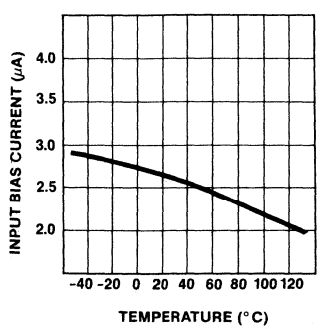
Note 8: I_{CC} tested for +4.75V<V_{CC}<+10.5V with V_{EE} grounded. I_{EE} tested for -5.25V<V_{EE}<-4.75V with V_{CC} = +5V. I_{DD} tested for +4.75V<V_{DD}<+5.25V with the worst-case condition of all four comparator outputs at logic low.

Typical Operating Characteristics

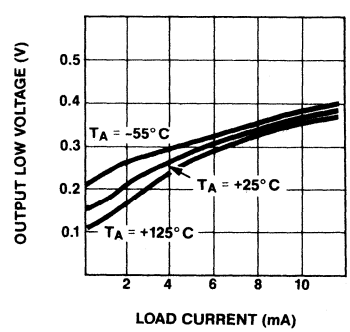
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE

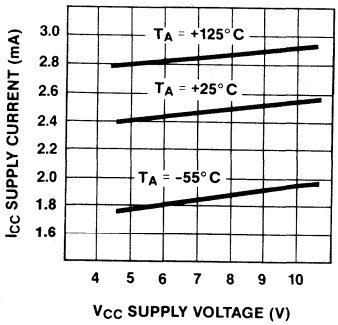


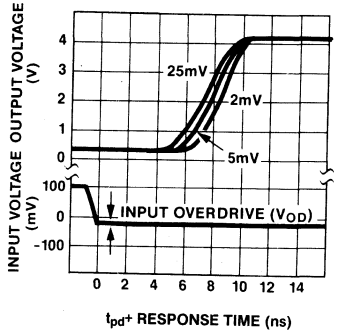
OUTPUT LOW VOLTAGE (V_{OL}) vs. LOAD CURRENT

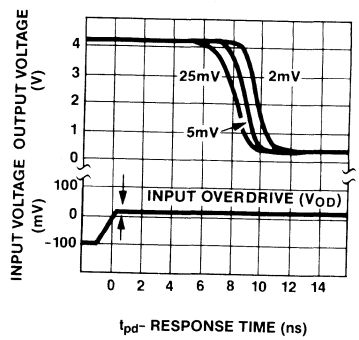


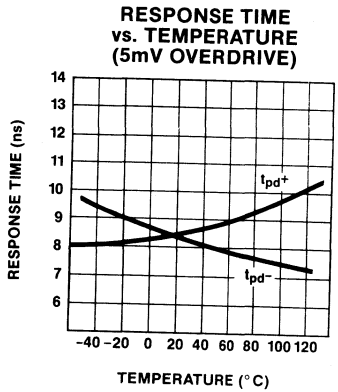
High-Speed, Low-Power Voltage Comparators

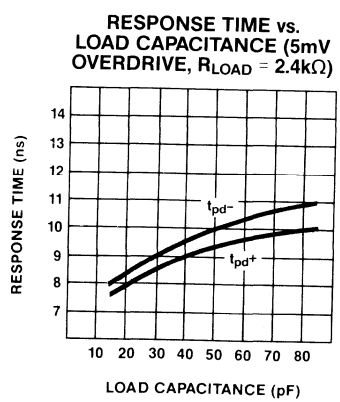
Typical Operating Characteristics (continued)











Pin Descriptions

MAX900

PIN	NAME	FUNCTION
1, 10, 11, 20	IN- (A, B, C, D)	Negative Input (Channels A, B, C, D)
2, 9, 12, 19	IN+ (A, B, C, D)	Positive Input (Channels A, B, C, D)
3	GND	Ground Terminal
4, 7, 14, 17	LATCH (A, B, C, D)	Latch Input (Channels A, B, C, D)
5, 6, 15, 16	OUT (A, B, C, D)	Output (Channels A, B, C, D)
8	V_{EE}	Negative Analog Supply and Substrate
13	V_{DD}	Positive Digital Supply
18	V_{CC}	Positive Analog Supply

MAX901

PIN	NAME	FUNCTION
1, 8, 9, 16	IN- (A, B, C, D)	Negative Input (Channels A, B, C, D)
2, 7, 10, 15	IN+ (A, B, C, D)	Positive Input (Channels A, B, C, D)
3	GND	Ground Terminal
4, 5, 12, 13	OUT (A, B, C, D)	Output (Channels A, B, C, D)
6	V_{EE}	Negative Analog Supply and Substrate
11	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

MAX902

PIN	NAME	FUNCTION
1, 8	IN- (A, B)	Negative Input (Channels A, B)
2, 9	IN+ (A, B)	Positive Input (Channels A, B)
3	GND	Ground Terminal
4, 11	LATCH (A, B)	Latch Input (Channels A, B)
5, 12	OUT (A, B)	Output (Channels A, B)
6, 13	N.C.	No Connect
7	V_{EE}	Negative Analog Supply and Substrate
10	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

MAX903

PIN	NAME	FUNCTION
1	V_{CC}	Positive Analog Supply
2	IN+	Positive Input
3	IN-	Negative Input
4	V_{EE}	Negative Analog Supply and Substrate
5	LATCH	Latch Input
6	GND	Ground Terminal
7	OUT	Output
8	V_{DD}	Positive Digital Supply

High-Speed, Low-Power Voltage Comparators

Applications Information

Circuit Layout

Because of the large gain-bandwidth transfer function of the MAX900-903, special precautions must be taken to realize their full high-speed capability. A printed circuit board with a good, low-inductance ground plane is mandatory. All decoupling capacitors (the small 100nF ceramic type is a good choice) should be mounted as close as possible to the power-supply pins. Separate decoupling capacitors for analog V_{CC} and for digital V_{DD} are also recommended. Close attention should be paid to the bandwidth of the decoupling and terminating components. Short lead lengths on the inputs and outputs are essential to avoid unwanted parasitic feedback around the comparators. Solder the device directly to the printed circuit board instead of using a socket.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of the MAX900-903 can create oscillation problems when the input traverses the linear region. For clean output switching without oscillation or steps in the output waveform, the input must meet minimum slew-rate requirements. Oscillation is largely a function of board layout and of coupled source impedance and stray input capacitance. Both poor layout and large source impedance will cause the part to oscillate and increase the minimum slew-rate requirement. In some applications, it may be helpful to apply some positive feedback between the output and + input. This pushes the output through the transition region cleanly, but applies a hysteresis in threshold seen at the input terminals.

TTL Output and Latch Inputs

The comparator TTL output stages are optimized for driving low-power Schottky TTL with a fan-out of four.

When the latch is connected to a logic high level or left floating, the comparator is transparent and immediately responds to changes at the input terminals. When the latch is connected to a TTL low level, the comparator output latches in the same state as at the instant that the latch command is applied, and will not respond to subsequent changes at the input. No latch is provided on the MAX901.

Power Supplies

The MAX900-903 can be powered from separate analog and digital supplies or from a single +5V supply. The analog supply can range from +5V to +10V with V_{EE} grounded for single-supply operation (Figures 1A and 1B) or from a split ±5V supply (Figure 1C). The V_{DD} digital supply always requires +5V.

In high-speed, mixed-signal applications where a common ground is shared, a noisy digital environment can adversely affect the analog input signal. When set up with separate supplies (Figure 1C), the MAX900-903 isolate analog and digital signals by providing a separate AGND(V_{EE}) and DGND.

Typical Power-Supply Alternatives

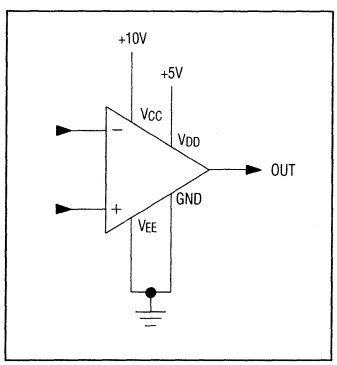


Figure 1A. Separate Analog Supply, Common Ground

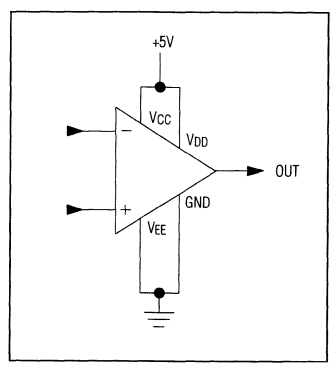


Figure 1B. Single +5V Supply, Common Ground

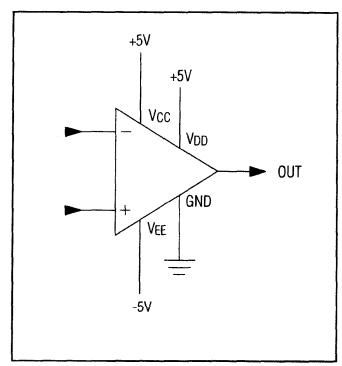


Figure 1C. Split ±5V Supply, Separate Ground

Definition of Terms

V_{OS} **Input Offset Voltage:** Voltage applied between the two input terminals to obtain TTL logic threshold (+1.4V) at the output.

V_{IN} Input Voltage Pulse Amplitude: Usually set to 100mV for comparator specifications.

V_{OD} **Input Voltage Overdrive:** Usually set to 5mV and in opposite polarity to V_{IN} for comparator specifications.

t_{pd+} Input to Output High Delay: The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold of an output low to high transistion.

t_{pd-} Input to Output Low Delay: The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold of an output high to low transition.

t_{pd+} (D) Latch Disable to Output High Delay: The propagation delay measured from the latch signal crossing the TTL threshold in a low to high transition to the point of the output crossing TTL threshold in a low to high transition.

t_{pd-} (D) Latch Disable to Output Low Delay: The propagation delay measured from the latch signal crossing the TTL threshold in a low to high transition to the point of the output crossing TTL threshold in a high to low transition.

t_s **Minimum Setup Time:** The minimum time before the negative transition of the latch signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time:** The minimum time after the negative transition of the latch signal that an input signal must remain unchanged in order to be acquired and held at the output.

t_{pw} (D) **Minimum Latch Disable Pluse Width:** The minimum time that the latch signal must remain high in order to acquire and hold an input signal change.

High-Speed, Low-Power Voltage Comparators

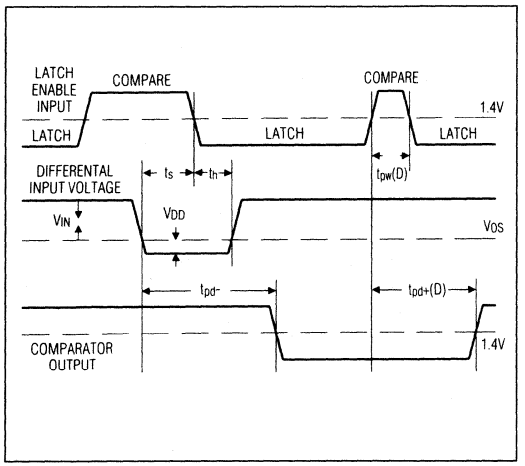


Figure 2. MAX900/902/903 Timing Diagram

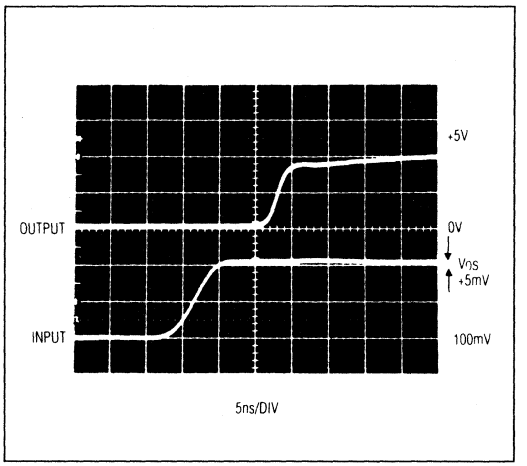


Figure 3. t_{pd}+ Response Time to 5mV Overdrive

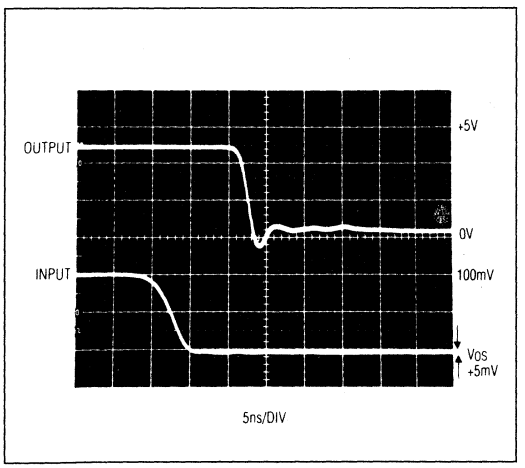


Figure 4. t_{pd}- Response Time to 5mV Overdrive

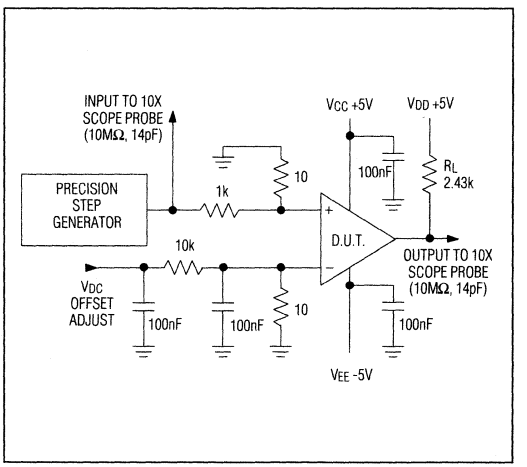


Figure 5. Response-Time Setup

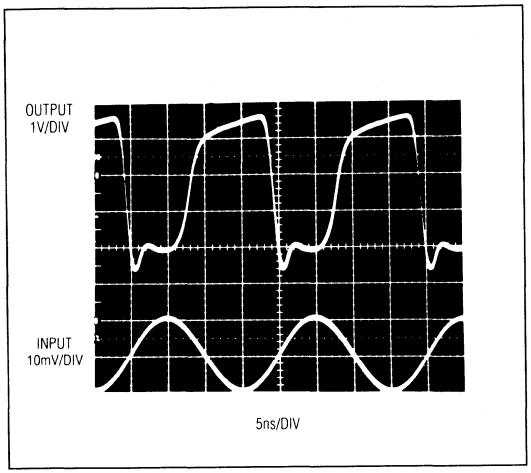


Figure 6. Response to 50MHz Sine Wave

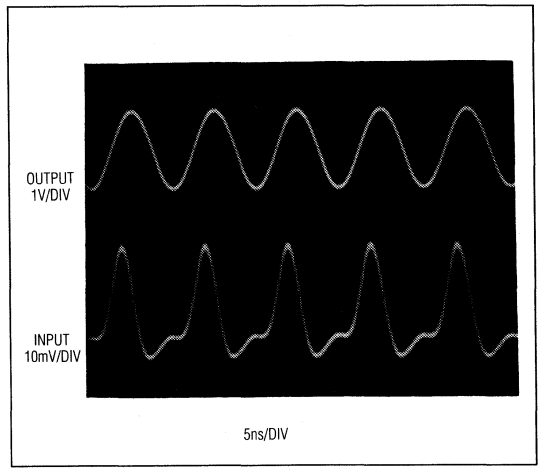


Figure 7. Response to 100MHz sine wave photo

Typical Application

Programmed, Variable-Alarm Limits

By combining two quad analog comparators with an octal, 8-bit D/A converter (the MX7228), several alarm and limit-defect functions can be performed simultaneously without external adjustments.

The MX7228's internal latches allow the system processor to set the limit points for each comparator independently and update them at any time. Set the upper and lower thresholds for a single transducer by pairing the D/A converter and comparator sections.

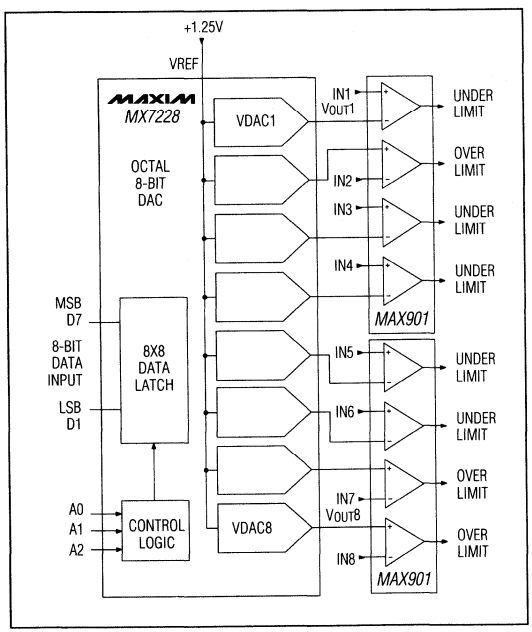


Figure 8. Alarm Circuit Level-Monitors Eight Separate Inputs

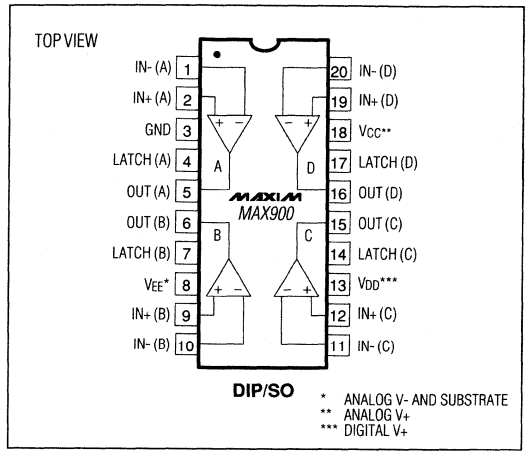
High-Speed, Low-Power Voltage Comparators

Ordering Information (continued)

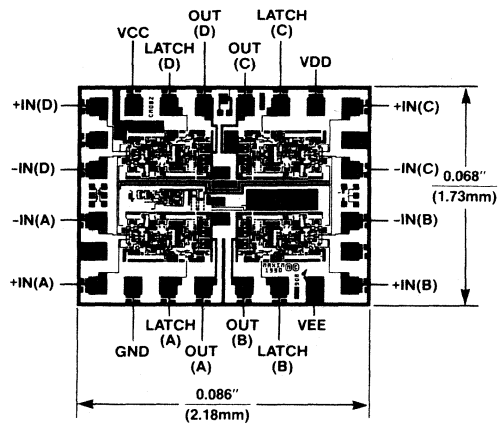
PART	TEMP. RANGE	PIN-PACKAGE
MAX901ACPE	0°C to +70°C	16 Plastic DIP
MAX901BCPE	0°C to +70°C	16 Plastic DIP
MAX901ACSE	0°C to +70°C	16 Narrow SO
MAX901BCSE	0°C to +70°C	16 Narrow SO
MAX901BC/D	0°C to +70°C	Dice*
MAX901AEPE	-40°C to +85°C	16 Plastic DIP
MAX901BEPE	-40°C to +85°C	16 Plastic DIP
MAX901AESE	-40°C to +85°C	16 Narrow SO
MAX901BESE	-40°C to +85°C	16 Narrow SO
MAX901AMJE	-55°C to +125°C	16 CERDIP
MAX901BMJF	-55°C to +125°C	16 CERDIP
MAX902CPD	0°C to +70°C	14 Plastic DIP
MAX902CSD	0°C to +70°C	14 Narrow SO
MAX902C/D	0°C to +70°C	Dice*
MAX902EPD	-40°C to +85°C	14 Plastic DIP
MAX902ESD	-40°C to +85°C	14 Narrow SO
MAX902MJD	-55°C to +125°C	14 CERDIP
MAX903CPA	0°C to +70°C	8 Plastic DIP
MAX903CSA	0°C to +70°C	8 SO
MAX903C/D	0°C to +70°C	Dice*
MAX903EPA	-40°C to +85°C	8 Plastic DIP
MAX903ESA	-40°C to +85°C	8 SO
MAX903MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Pin Configurations (continued)



Chip Topography



Note: Substrate connected to V_{EE}.
MAX900/901/902/903

ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

High-Speed, Clocked D – Flip Flop, ECL Voltage Comparators

General Description

The MAX905/MAX906 high-speed, ECL compatible voltage comparators eliminate oscillation by separating the comparator input and output stages with a clocked, master-slave D flip-flop. Typical comparator propagation delay is 2ns.

The MAX905/MAX906 feature separate analog and digital grounds, and can operate from dual, single positive, or single negative supplies.

The MAX905 is a single ECL comparator, and comes in 14-lead DIP and SO packages. The MAX906 is a dual ECL comparator, and comes in 16-lead DIP and SO packages.

Applications

High-Speed A/D Converters

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Features

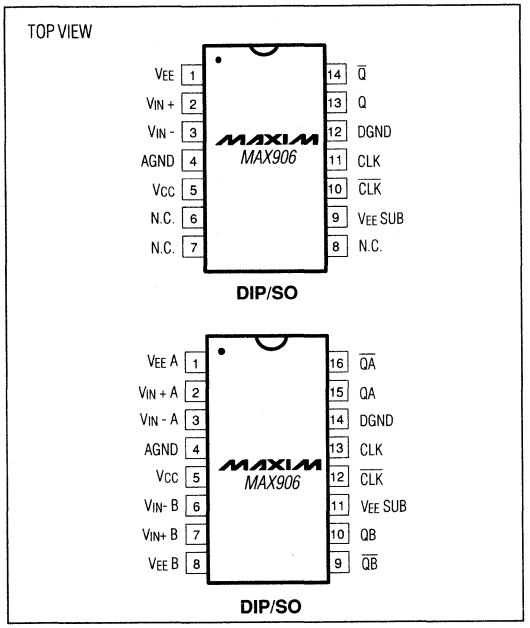
- ♦ **Immune to Oscillation**
- ♦ **Resolves ±1mV Input Voltages**
- ♦ **Typical 2ns Propagation Delay**
- ♦ **Propagation Delay Insensitive to Input Overdrive**
- ♦ **Input Common Mode Range Includes Negative Supply**

Ordering Information

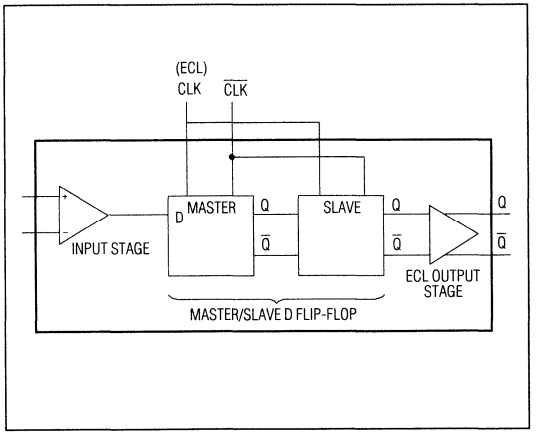
PART	TEMP. RANGE	PIN-PACKAGE
MAX905CPD	0°C to +70°C	14 Plastic DIP
MAX905CSD	0°C to +70°C	14 SO
MAX905C/D	0°C to +70°C	Dice*
MAX905EPD	-40°C to +85°C	14 Plastic DIP
MAX905ESD	-40°C to +85°C	14 SO
MAX905MJD	-55°C to +125°C	14 CERDIP
MAX906CPE	0°C to +70°C	16 Plastic DIP
MAX906CSE	0°C to +70°C	16 SO
MAX906C/D	0°C to +70°C	Dice*
MAX906EPA	-40°C to +85°C	16 Plastic DIP
MAX906ESE	-40°C to +85°C	16 SO
MAX906MJE	-40°C to +125°C	16 CERDIP

Contact factory for dice specifications.

Pin Configurations



Functional Diagram



8

MAXIM

D/A Converters

MAXIM

CMOS Quad, Serial Interface, 8-Bit D/A Converter

General Description

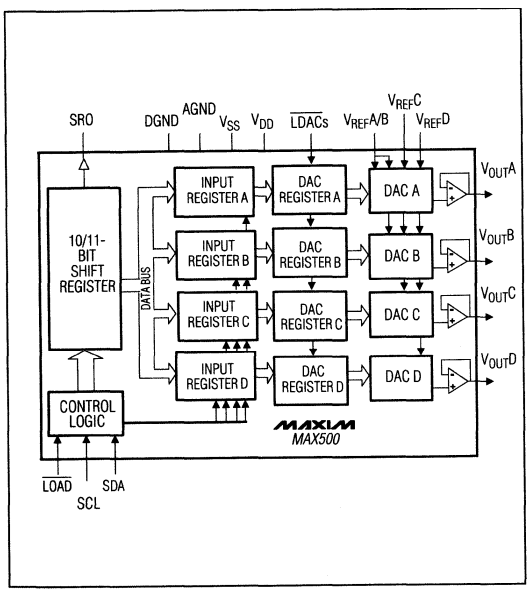
MAX500 is a quad 8-bit voltage output digital to analog converter (DAC) with a cascadable serial interface. The MAX500 circuit includes four output buffer amplifiers and input logic for an easy-to-use two- or three-wire serial interface. In a system with several MAX500s, only one serial data line is required to load all the DACs by cascading them. The MAX500 contains double-buffered logic and a 10-bit shift register which allows all four DACs to be updated simultaneously using one control signal. There are three reference inputs so that the range of two of the DACs can be independently set while the other two DACs track each other.

The MAX500 achieves 8-bit performance over the full operating temperature ranges without external trimming.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment

Functional Block Diagram



Features

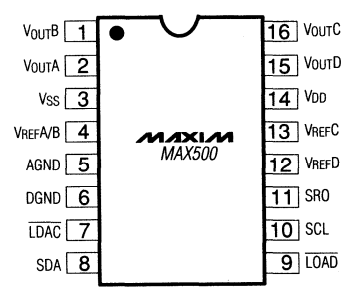
- ♦ **Buffered Voltage Outputs**
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **Requires No External Adjustments**
- ♦ **Two- or Three-Wire Cascadable Serial Interface**
- ♦ **16-Pin Package**
- ♦ **Operates from Single or Dual Supplies**

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX500ACPE	0°C to +70°C	Plastic DIP	±1 LSB
MAX500BCPE	0°C to +70°C	Plastic DIP	±2 LSB
MAX500ACWE	0°C to +70°C	Wide SO	±1 LSB
MAX500BCWE	0°C to +70°C	Wide SO	±2 LSB
MAX500BC/D	0°C to +70°C	Dice	±2 LSB
MAX500AEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX500BEWE	-40°C to +85°C	Wide SO	±2 LSB
MAX500AEJE	-40°C to +85°C	CERDIP	±1 LSB
MAX500BEJE	-40°C to +85°C	CERDIP	±2 LSB
MAX500AMJE	-55°C to +125°C	CERDIP	±1 LSB
MAX500BMJE	-55°C to +125°C	CERDIP	±2 LSB

Pin Configuration

Top View



CMOS Quad, Serial Interface, 8-Bit D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... -7V, V_{DD} +0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
V_{REF} to AGND ..... -0.3V, V_{DD} +0.3V
V_{OUT} to AGND (Note 1) ..... -0.3V, V_{DD} +0.3V

Power Dissipation (any package) to +75°C 500mW
Derate Above +75°C ..... 8mW/°C
Operating Temperature Range
MAX500XC ..... 0°C to +70°C
MAX500XE ..... -40°C to +85°C
MAX500XM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Dual Supply Specifications

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{DD} = 15V ±5% V_{REF} = 10V	MAX500A MAX500B			±1 ±2	LSB
Relative Accuracy		MAX500A MAX500B				±½ ±1	LSB
Differential Nonlinearity Guaranteed Monotonic						±1	LSB
Full Scale Error		MAX500A MAX500B				±½ ±1	LSB
Full Scale Tempco		V_{REF} = 10V			±5		ppm/°C
Zero Code Error		T_A = 25°C	MAX500A MAX500B			±15 ±20	mV
		T_A = T_{MIN} to T_{MAX}	MAX500A MAX500B			±20 ±30	
Zero Code Tempco					±30		µV/°C
REFERENCE INPUT							
Reference Input Range				2		V_{DD} - 4	V
Reference Input Resistance Pins 12, 13 Reference Input Resistance Pin 4				11 5.5			kΩ
Reference Input Capacitance		(Note 2) Code Dependent				100	pF
Channel-to-Channel Isolation		(Note 3)		-60			dB
AC Feedthrough		(Note 3)		-70			dB
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}			2.4			V
Digital Input Low Voltage	V_{IL}					0.8	V
Digital Output High Voltage	V_{OH}	I_{OUT} = -1mA, SRO only		V_{DD} -1			V
Digital Output Low Voltage	V_{OL}	I_{OUT} = 1mA, SRO only		0.4			V

ELECTRICAL CHARACTERISTICS: Dual Supply Specifications (continued)

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input Leakage Current		(Note 4)	Excluding $\overline{LOAD}$ $\overline{LOAD}$ = 0V			±1 30	µA
Digital Input Capacitance		(Note 5)				8	pF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		(Note 5)		3			V/µs
V_{OUT} Settling Time		To ±½ LSB, V_{REF} = 10V, V_{DD} = +15V, 2kΩ in parallel with 100pF load				4	µs
Digital Feedthrough		(Note 6)			50		nV-s
Digital Crosstalk		(Note 6)			50		nV-s
Output Load Resistance		V_{OUT} = 10V		2			kΩ
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specificed performance		11.4		16.5	V
Positive Supply Current	I_{DD}	Outputs unloaded.	T_A = 25°C T_A = T_{MIN} to T_{MAX}			10 12	mA
Negative Supply Current	I_{SS}	Outputs unloaded.	T_A = 25°C T_A = T_{MIN} to T_{MAX}			-9 -10	mA
SWITCHING CHARACTERISTICS (Note 5)							
THREE-WIRE MODE							
SDA Valid to SCL Setup	t_{S1}			150			ns
SDA Valid to SCL Hold	t_H			0			ns
SCL High Time	t_1			350			ns
SCL Low Time	t_2			350			ns
$\overline{LOAD}$ Pulse Width	t_{LDW}			150			ns
$\overline{LOAD}$ Delay from SCL	t_{LDS}			150			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}			150			ns
SRO Output Delay	t_{D1}	C_{LOAD} = 50pF				150	ns
TWO-WIRE MODE							
SDA Valid to SCL Hold	t_H			0			ns
SCL High Time	t_1			350			ns
SCL Low Time	t_2			350			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}			150			ns
SCL Valid to SDA Setup	t_{S1}	(Start condition)		150			ns
SDA Valid to SCL Setup	t_{S2}	(Stop condition)		100			ns
SDA Valid to Rising SCL	t_{S3}			125			ns
SRO Output Delay	t_{D1}	C_{LOAD} = 50pF				150	ns

CMOS Quad, Serial Interface, 8-Bit D/A Converter

ELECTRICAL CHARACTERISTICS: Single Supply Specifications

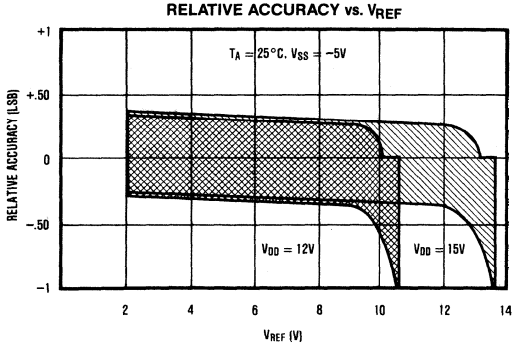
(V_{DD} = +15V ±5%, V_{SS} = AGND = DGND = 0V, V_{REF} = 10V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{DD} = 15V ±5% V_{REF} = 10V	MAX500A MAX500B			±1 ±2	LSB
Relative Accuracy			MAX500A MAX500B			±½ ±1	LSB
Differential Nonlinearity Guaranteed Monotonic						±1	LSB
Full Scale Error			MAX500A MAX500B			±½ ±1	LSB
Full Scale Tempco		V_{REF} = 10V			±5		ppm/°C
Zero Code Error		T_A = 25°C	MAX500A MAX500B			±15 ±20	mV
		T_A = T_{MIN} to T_{MAX}	MAX500A MAX500B			±20 ±30	mV
Zero Code Tempco					±30		µV/°C
REFERENCE INPUT – All specifications are the same as for dual supplies.							
DIGITAL INPUTS – All specifications are the same as for dual supplies.							
DYNAMIC PERFORMANCE – All specifications are the same as for dual supplies.							
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		14.25		15.75	V
Positive Supply Current	I_{DD}	Outputs Unloaded T_A = 25°C T_A = T_{MIN} to T_{MAX}				10 12	mA
SWITCHING CHARACTERISTICS – All specifications are the same as for dual supplies.							

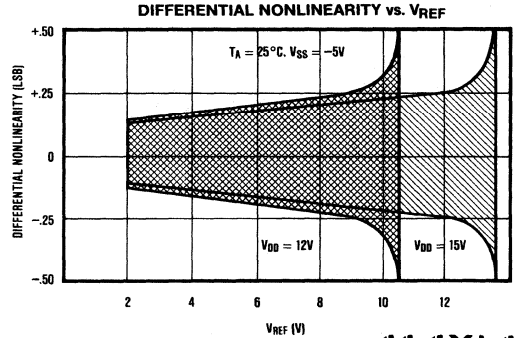
Note 1: The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.
Note 2: Guaranteed by design. Not production tested.
Note 3: V_{REF} = 10 kHz, 10V peak-to-peak sine wave.
Note 4: $\overline{LOAD}$ has a weak internal pull-up resistor to V_{DD}.
Note 5: Sample tested at +25°C to ensure compliance.
Note 6: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

Typical Operating Characteristics

RELATIVE ACCURACY vs. V_{REF}

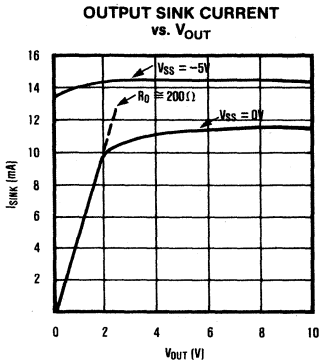


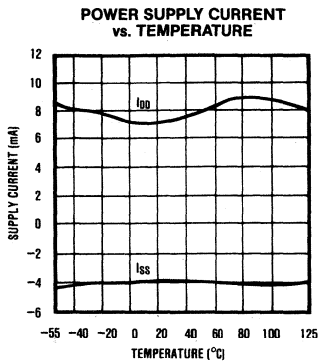
DIFFERENTIAL NONLINEARITY vs. V_{REF}

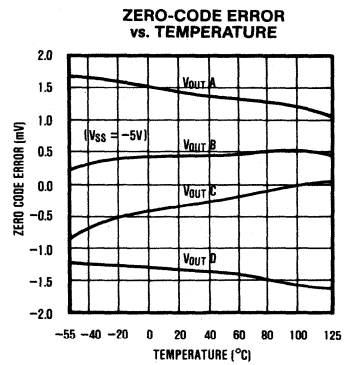


CMOS Quad, Serial Interface, 8-Bit D/A Converter

Typical Operating Characteristics (Continued)







Detailed Description

The MAX500 has four matched voltage output digital-to-analog converters (DAC). The DACs are "inverted" R-2R ladder networks which convert 8 digital bits into equivalent analog output voltages in proportion to the applied reference voltage(s). Two DACs in the MAX500 have a separate reference input while the other two DACs share one reference input. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

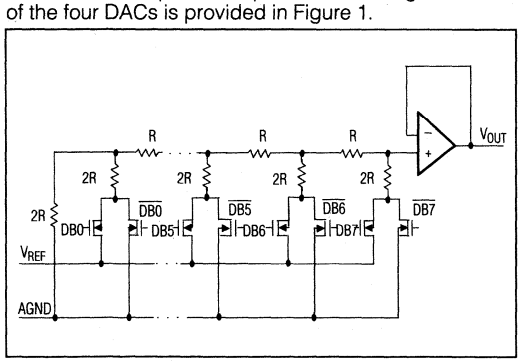


Figure 1. Simplified DAC Circuit Diagram

VREF Input

The voltage at V_{REF} pins (pins 4, 12 and 13) sets the full scale output of the DAC. The input impedance of the V_{REF} inputs is code dependent. The lowest value, approximately 11kΩ (5.5kΩ for pin 4), occurs when the input code is 01010101. The maximum value of infinity occurs when the input code is 00000000. Because the input resistance at V_{REF} is code dependent, the DAC's reference sources should have an output impedance of no more than 20Ω (no more than 10Ω for pin 4). The input capacitance at V_{REF} is also code dependent and typically varies from 15pF to 35pF (30pF to 70pF for pin 4).

$V_{OUT}A$, $V_{OUT}B$, $V_{OUT}C$, and $V_{OUT}D$ can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_b \times \frac{V_{REF}}{256}$$

where N_b is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All voltage outputs are internally buffered by precision unity gain followers which slew at greater than 3V/µs. When driving 2kΩ in parallel with 100pF with a full scale transition (0V to +10V or +10V to 0V), the output settles to ±½ LSB in less than 4µs. The buffers will also drive 2kΩ in parallel with 500pF to 10V levels without oscillation. Typical dynamic response and settling performance of the MAX500 is shown in Figures 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to AGND is provided by a PMOS input structure. The output circuitry incorporates a pull-down circuit to actively drive V_{OUT} to within +15mV of the negative supply (V_{SS}). The buffer circuitry allows each DAC output to sink, as well as source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to AGND, so that the zero error is kept at or under ½ LSB (V_{REF} = +10V). A plot of the output sink current versus output voltage is shown in the Typical Operating Characteristics section.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however, the power supply current (I_{DD}) is somewhat dependent on the input logic level. Supply current is specified for TTL input levels (worst case) but is reduced (by about 150µA) when the logic inputs are driven near DGND or 4 volts above DGND.

CMOS Quad, Serial Interface, 8-Bit D/A Converter

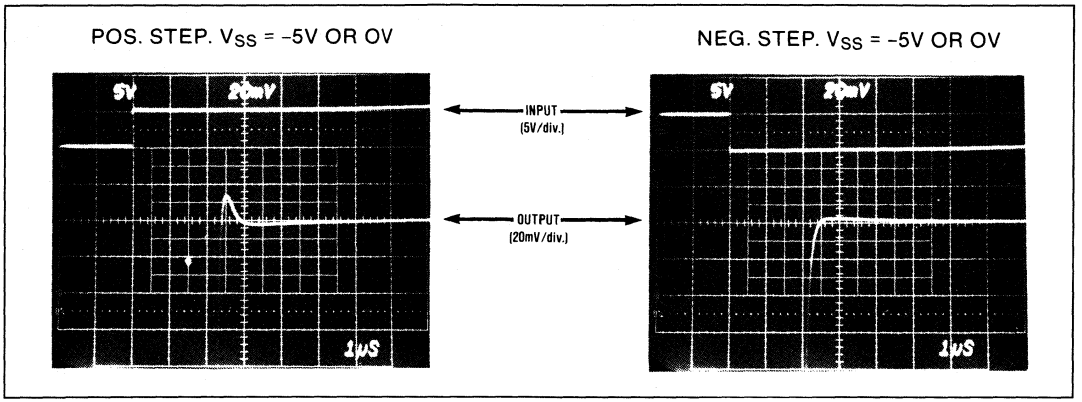


Figure 2. Positive and Negative Settling Times, V_{SS} = 0V or -5V

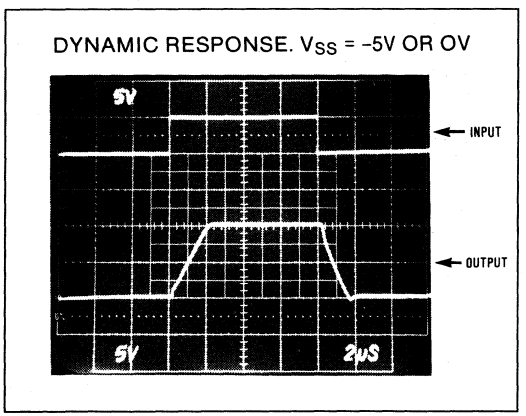


Figure 3. Dynamic Response, V_{SS} = 0V or -5V

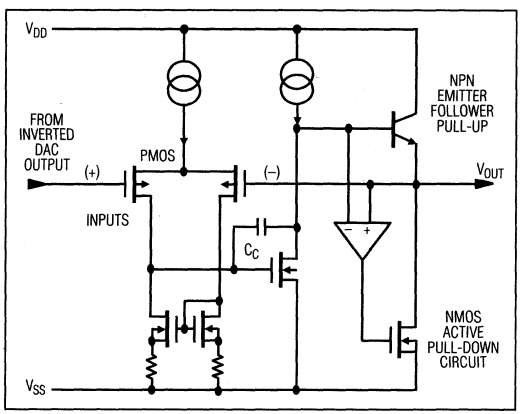


Figure 4. Simplified Output Buffer Circuit

The MAX500 allows the user to choose between a three-wire serial interface and a two-wire serial interface. The choice between the two-wire and the three-wire interface is set by the LOAD signal. If the LOAD is allowed to float (it has a weak internal pull-up resistor to V_{DD}), the two-wire interface is selected. If the LOAD signal is kept to a TTL logical high level, the three-wire interface is selected.

Three-Wire Interface

The three-wire interface uses the classic Serial Data (SDA), Serial Clock (SCL), and LOAD signals used in standard shift registers. The data is clocked in on the falling edge of SCL until all 10 bits (8 data bits and 2 address bits) are entered into the SHIFT REGISTER. A low level on LOAD line initiates the transfer of data from the SHIFT REGISTER to the addressed INPUT REGISTER. The data can stay in this register until all four of the INPUT REGISTERs are updated. Then all of the DAC REGISTERs can be simultaneously updated using the LDAC (LOAD DAC) signal. When LDAC is low, the INPUT REGISTER's data is loaded into the DAC REGISTERs (see Figure 5 for timing diagram). This mode is cascadable by connecting Serial Output (SRO) to the second chip's SDA pin. The delay of the SRO pin from SCL does not cause setup/hold time violations no matter how many MAX500s are cascaded.

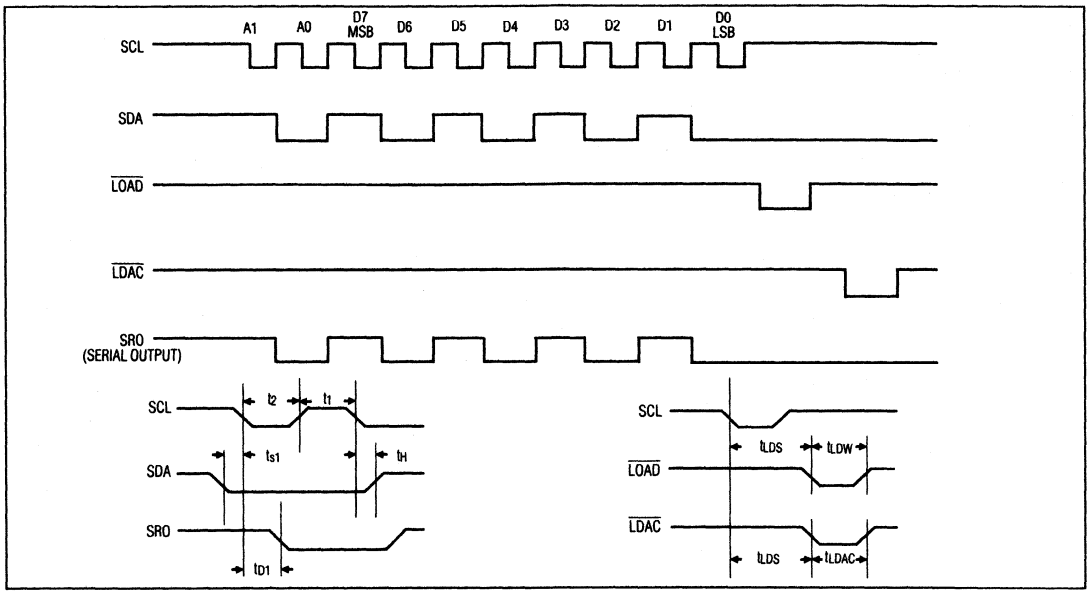


Figure 5. 3-Wire Mode

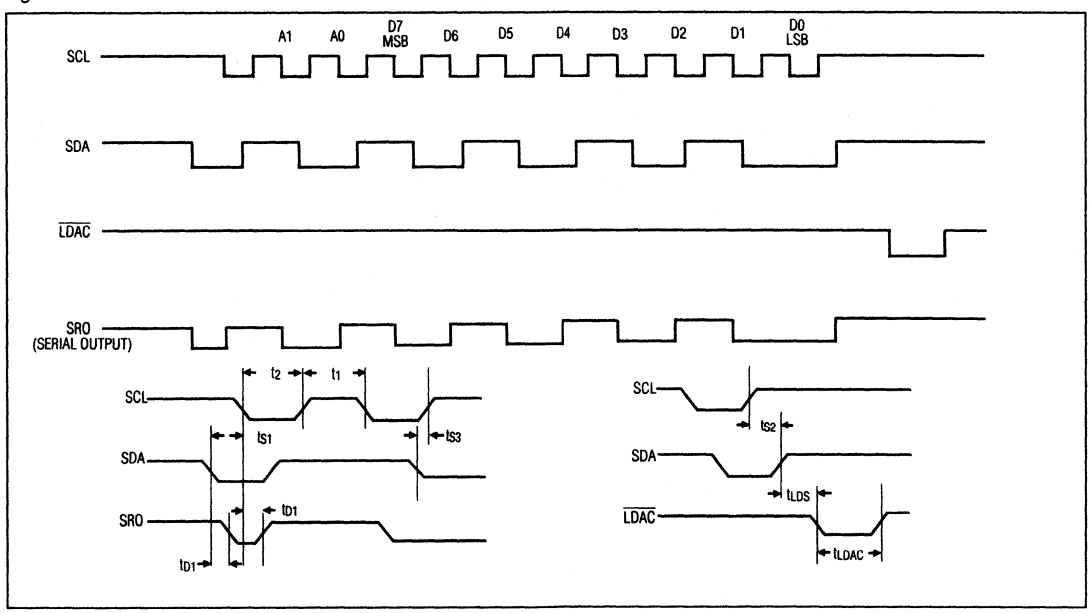


Figure 6. 2-Wire Mode

CMOS Quad, Serial Interface, 8-Bit D/A Converter

Two-Wire Interface

The two-wire interface uses SDA and SCL only. $\overline{LOAD}$ must be floating or tied to V_{DD}. Each data frame (8 data bits and 2 address bits) is synchronized by a timing relationship between SDA and SCL (see Figure 6 for the timing diagram). Both SDA and SCL should normally be high when inactive. A falling edge of SDA (while SCL is high) followed by a falling edge of SCL (while SDA is low) is the start condition. This always loads a 0 into the first bit of the SHIFT REGISTER. The SHIFT REGISTER is extended to 11 bits so this "data" will not affect the INPUT REGISTER information. The timing now follows the three-wire interface except the SDA line is not allowed to change when SCL is high (this prevents the MAX500 from retriggering its start condition). After the last data bit is entered, the SDA line should go low (while the SCL line is low), then the SCL line should rise followed by the SDA line rising. This is defined as the stop condition, or end of frame.

Cascading the two-wire interface can be done, but the user must be careful of both timing and formatting. Timing must take into account the intrinsic delay of the SRO pin from the internally generated start/stop conditions. The t_{S2} value should be increased by n times t_{D1}, (where n = number of cascaded MAX500s). The t_{LDS} value should also be increased by n times t_{D1}. No other timing parameters need to be modified. A more serious concern is one of formatting. Generally since each frame has a start/stop condition, each chip that has data cascaded through it will accept that data as if it were its own data. Therefore, to circumvent this limitation, the user should not generate a stop bit until all DACs have been loaded. For example, if there are three MAX500s cascaded in the two-wire mode, the data transfer should begin with a start condition, then followed by 10 data bits, a zero bit, 10 data bits, a zero bit, 10 data bits, and then a stop condition. This will prevent each MAX500 from decoding the middle data for itself.

The data is entered into the SHIFT REGISTER in the following order:

A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
(First) (MSB) (Last)

where address bits A1 and A0 select which DAC register receives data from the internal SHIFT REGISTER. Table 1 lists the channel addresses. D7 through D0 (D7 is MSB) is the data byte.

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Since $\overline{LDAC}$ is asynchronous with respect to SCL, SDA, and LOAD, care must be taken to assure that incorrect data is not latched through to the DAC REGISTERs. If the three-wire serial interface is used, $\overline{LDAC}$ can be tied low permanently or $\overline{LDAC}$ can be tied to $\overline{LOAD}$ as long as t_{LDS} is always maintained. However, if the two-wire interface is used, $\overline{LDAC}$ should not fall before the stop condition is internally detected. (This is the reason for the t_{LDS} delay of $\overline{LDAC}$ after the last rising edge of SDA.)

The SRO output swings from V_{DD} to DGND. Cascading to other MAX500s poses no problem. If SRO is used to drive a TTL compatible input, then a clamp diode between TTL +5V and V_{DD} and current limiting resistor should be used. This will prevent potential latchup problems with the 5V supply.

Table 2 shows the truth table for SDA, SCL, $\overline{LOAD}$, and $\overline{LDAC}$ operation. Figures 5 and 6 show the timing diagrams for the MAX500.

Table 2. Logic Input Truth Table

SCL	SDA	$\overline{LOAD}$	$\overline{LDAC}$	FUNCTION
F	Data	V_{DD}	H	Latching data into Shift Register (2W)
H	Data	V_{DD}	H	Data should not be changing (2W)
L	X	V_{DD}	H	Data is allowed to change (2W)
F	Data	M	H	Latching data into Shift Register (3W)
H	X	M	H	Data is allowed to change (3W)
L	X	M	H	Data is allowed to change (3W)
H	X	L	H	Loads Input Register from Shift Register (3W)
H	X	L	L	DAC register reflects data held in their respective Input Registers

Notes:

H = Logical High
L = Logical Low
M = TTL Logical High
X = Don't Care

2W = 2-Wire
3W = 3-Wire
F = Falling Edge

CMOS Quad, Serial Interface, 8-Bit D/A Converter

Applications Information

Power Supply and Reference Operating Ranges

The MAX500 is fully specified to operate with V_{DD} between +12V ± 5% and +15V ±10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. 8-bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however, zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. The MAX500 is specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 shows suggested circuit board layouts for minimizing crosstalk.

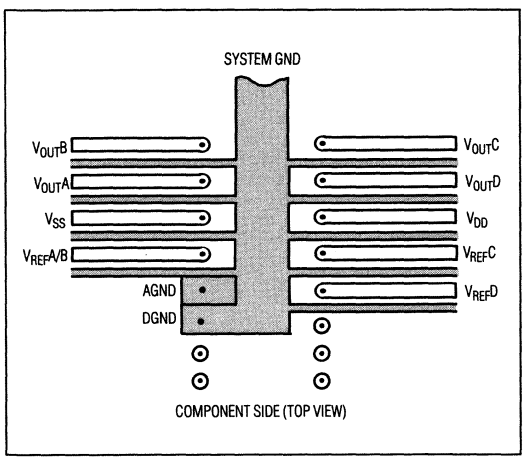


Figure 7. Suggested MAX500 PCB Layout for Minimizing Crosstalk

Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configuration is shown in Figure 8 for the MAX500. The device can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to AGND. The unipolar code table is given in Table 3.

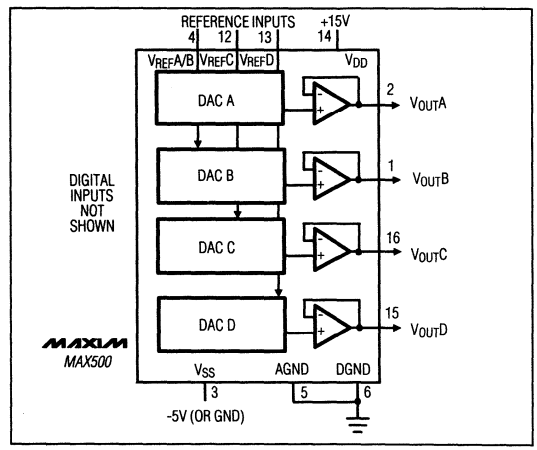


Figure 8. MAX500 Unipolar Output Circuit

Table 3. Unipolar Code Table

MSB				DAC CONTENTS				LSB	ANALOG OUTPUT
1	1	1	1		1	1	1	1	$+V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0		0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0		0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0	1	1	1		1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0		0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0		0	0	0	0	0V

Note: 1 LSB = $(V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

CMOS Quad, Serial Interface, 8-Bit D/A Converter

Bipolar Output

Each DAC output may be configured for bipolar operation using the circuit in Figure 9. One op-amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF}(2D_A - 1)$$

where D_A is a fractional representation of the digital word in Register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 9.

Table 4. Bipolar Code Table

DAC CONTENTS MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Note: 1 LSB = $(V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

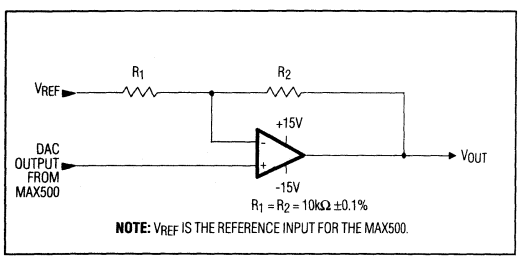


Figure 9. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 10. The output voltage at $V_{OUT}A$ is:

$$V_{OUT}A = V_{BIAS} + D_AV_{IN}$$

where D_A is a fractional representation of the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Since AGND current is a function of the 4 DAC codes, it should be driven by a low impedance source. V_{BIAS} must be positive.

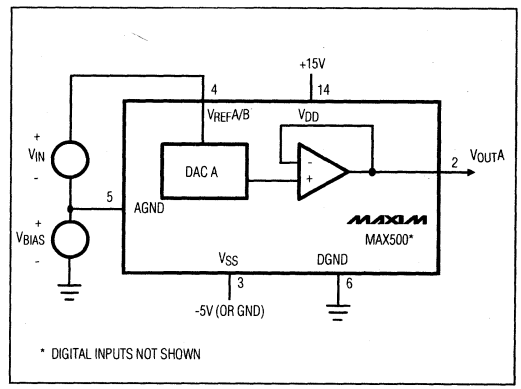


Figure 10. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the MAX500 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 11 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

Generating Vss

The performance of the MAX500 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 12.

Digital Interface Applications

Figures 13 through 16 show examples of interfacing the MAX500 to most popular microprocessors.

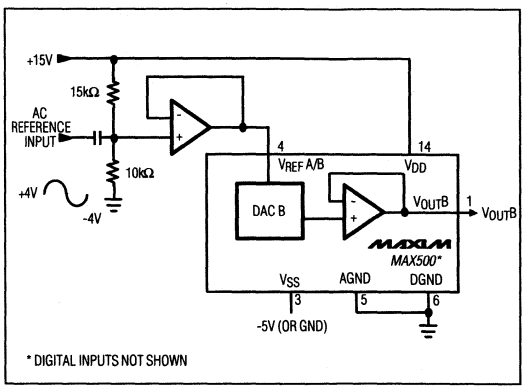


Figure 11. AC Reference Input Circuit

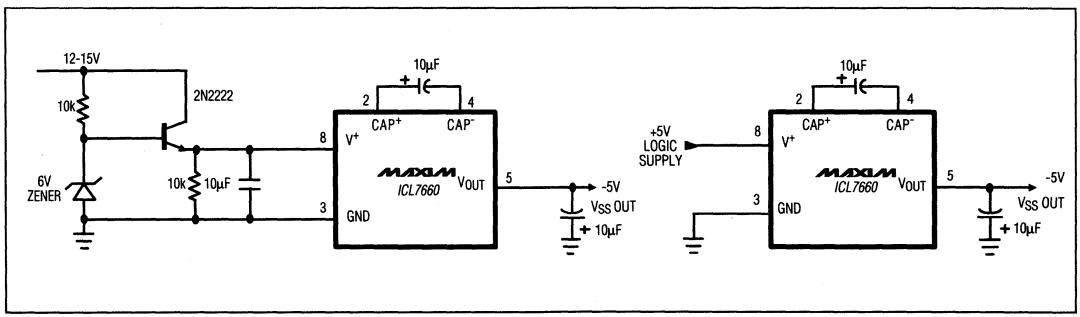


Figure 12. Generating -5V for V_{SS}

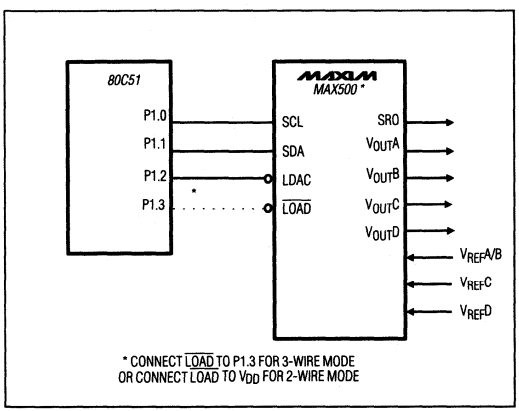


Figure 13. 80C51 Interface

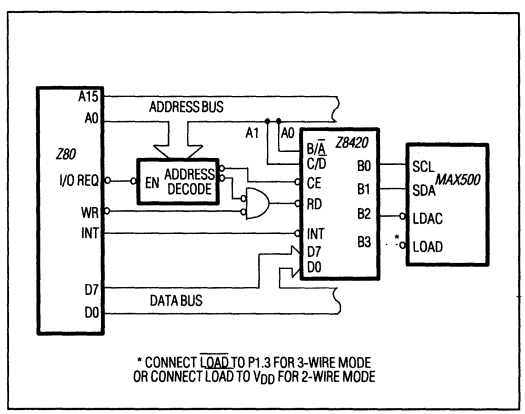


Figure 14. Z-80 with Z8420 PIO Interface

CMOS Quad, Serial Interface, 8-Bit D/A Converter

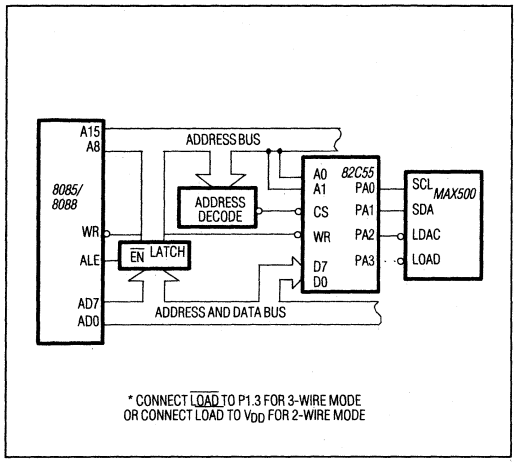


Figure 15. 8085/8088 with Programmable Peripheral Interface

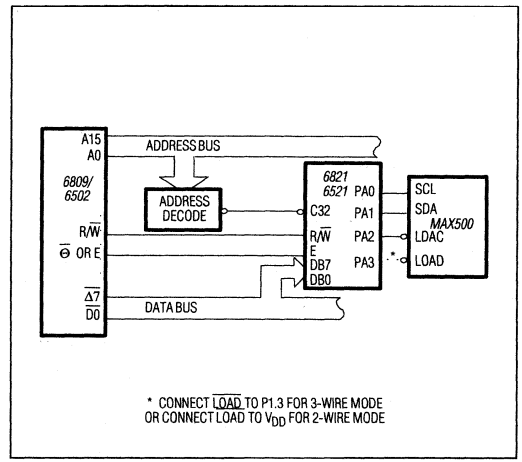
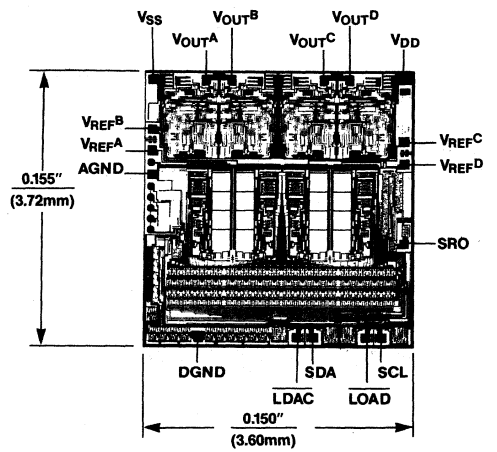


Figure 16. 6809/6502 Interface

Chip Topography



MAXIM

Voltage Output, 12-Bit Multiplying DAC

General Description

The MAX501/MAX502 are 12-bit, 4-quadrant, votlage-output, multiplying digital-to-analog converters (DACs) with an output amplifier. Thin-film resistors, laser-trimmed at the wafer level, maintain accuracy over the full operating temperature range.

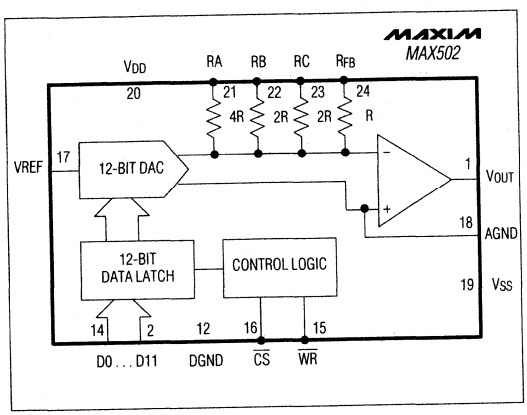
The MAX501/MAX502 has buffered latches that are easily interfaced with microprocessors. Data is transferred into the input register from a right-justified 8+4-bit format (MAX501) or a 12-bit wide data path (MAX502). For the MAX501, an $\overline{LDAC}$ signal transfers data from the input register to the DAC register. For the MAX502, the input registers are controlled by standard CHIP SELECT ($\overline{CS}$), $\overline{WRITE}$ ($\overline{WR}$) signals. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs are grounded making all latches transparent. All logic inputs are level-triggered and compatible with TTL and +5V CMOS logic levels.

The internally compensated, low input offset-voltage output amplifier provides an output voltage from +10V to -10V while sourcing and sinking up to 5mA.

Applications

Attenuators
Programmable-Gain Amplifiers
Servo Controls
Digital-to-4-20mA Converters
Automatic Test Equipment

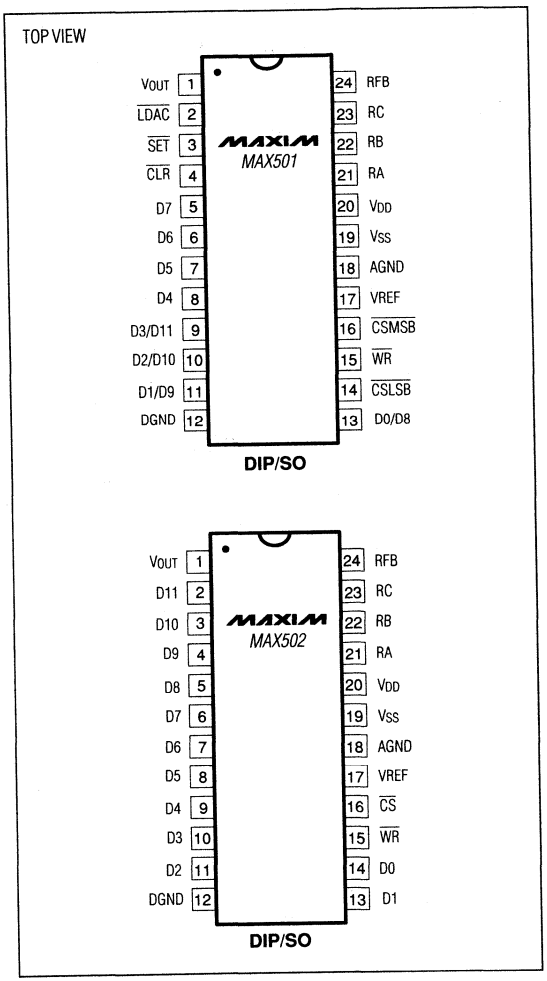
Functional Diagram



Features

- ♦ 12-Bit Voltage Output DAC
- ♦ Monotonic Over Temperature
- ♦ Four Range-Scaling Resistors
- ♦ Available in Commercial, Extended & Military Temperature Ranges
- ♦ 24-Pin DIP & Wide SO Packages

Pin Configurations



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MAXIM

CMOS Quad 8-Bit D/A Converters

General Description

Maxim's MAX505/MAX506 each contain four 8-bit voltage output digital-to-analog converters (DACs). They include output buffer amplifiers and input logic for simple microprocessor and TTL/CMOS interfaces. 8-bit performance is achieved over the full operating temperature range without external trimming.

The MAX505 contains double-buffered logic inputs which allow all analog outputs to be simultaneously updated using one control signal. There are also four separate reference inputs so that the range of each DAC can be independently set.

The MAX506 has separate input registers for each of its four DACs. Data is transferred into an input register from a common 8-bit TTL/CMOS compatible input port. Address inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. All DACs share a common reference input.

Applications

Minimum Component Count Analog Systems

Digital Offset/Gain Adjustment

Industrial Process Control

Arbitrary Function Generators

Automatic Test Equipment

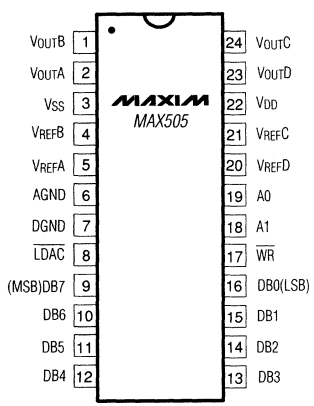
Microprocessor Controlled Calibration

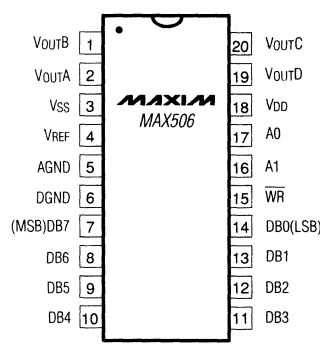
Features

- **Buffered Voltage Output**
- **Double-Buffered Inputs (MAX505)**
- **Microprocessor and TTL/CMOS Compatible**
- **Operates from Single or Dual Supplies**
- **Requires No External Adjustments**
- **Outputs Swing Rail to Rail**
- **Available in Commercial, Extended & Military Temperature Ranges**
- **Available in Plastic DIP, Small Outline, and CERDIP Packages**

Pin Configurations

TOP VIEW





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MAXIM

Voltage Output, 12-Bit DAC With Internal Reference

General Description

The MAX507/MAX508 are complete, 12-bit voltage output digital-to-analog converters (DACs). The DAC output voltage and the reference have the same polarity, allowing single-supply operation. The DAC reference voltage is provided by an internal buried-zener reference. Integrating a DAC, voltage-output amplifier, and reference on one monolithic device greatly enhances reliability over multi-chip circuits.

Doubled-buffered logic inputs interface easily to microprocessors (µP). Data is transferred into the INPUT register from either a 12-bit-wide data bus (MAX507) for 16-bit µPs, or a right-justified (8+4) -bit format (MAX508) for 8- or 16-bit µPs. All logic signals are level triggered and are TTL and CMOS compatible. Interface timing specifications insure compatibiltiy with all common µPs.

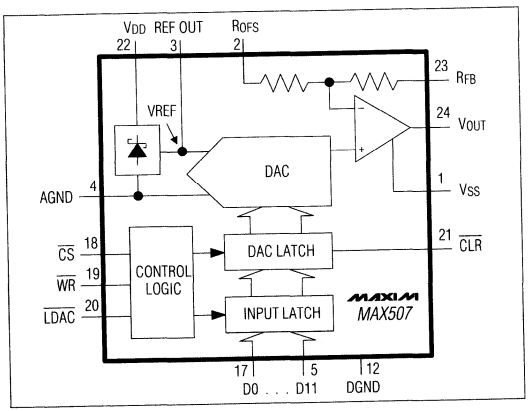
The DACs are specified and tested for both dual- and single-supply operation. Usable supplies range from single +12V to dual ±15V.

On-board gain-setting resistors allow three output-voltage ranges: 0V to +5V and 0V to +10V can be generated when using either single or dual supplies. With dual supplies, an additional output range of ±5V is available. The output amplifier can drive a 2kΩ load to +10V.

Applications

Digital Offset and Gain Adjustment
Industrial Control
Arbitrary Function Generators
Automatic Test Equipment
Automated Calibration
Machine and Motion Control

Functional Diagram

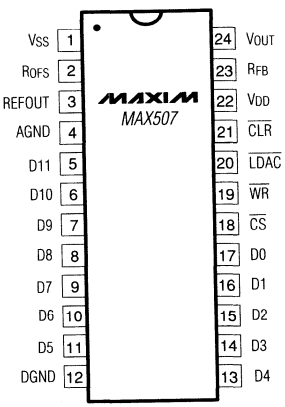


Features

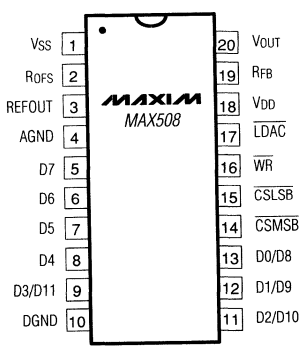
- ♦ 12-Bit Voltage Output
- ♦ Low Noise Voltage Reference
- ♦ Fast µP Interface
- ♦ 12 (MAX507) and 8+4 (MAX508) Data Bus Width
- ♦ Single +12V to Dual ±15V Supply Operation
- ♦ 20- and 24-Pin DIP and Wide SO Packages

Pin Configurations

TOP VIEW



DIP/SO



DIP/SO

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ADVANCE INFORMATION
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MAXIM

Quad-CMOS 12-Bit Serial Input Multiplying D/A Converter

General Description

The MAX514 is a quad 12-bit current-output multiplying digital-to-analog converter (DAC) that is packaged in a space-saving 28-pin DIP or 28-pin surface mount SO. Its 3-wire serial interface saves additional circuit board space and also results in low power dissipation. When used with microprocessors (µP) with a serial port, the MAX514 minimizes the digital noise feedthrough from its input pins to its output. The serial ports can be used as a dedicated analog bus and kept inactive while the MAX514 is in use. Serial interfacing also reduces the complexity of opto- or transformer-isolated applications.

The MAX514 contains four 12-bit R-2R type DACs, each with a serial-in parallel-out shift register, a DAC register and control logic. On the rising edge of the clock (CLK) pulse, the serial input (SRI) data is shifted into the respective DAC. When all the data is clocked in, it is transferred into the DAC register by taking the appropriate LOAD input low.

The MAX514 is specified both with a single +5V and +15V power supply. With a +5V supply, the digital inputs are TTL and +5V CMOS compatible. High voltage CMOS compatibility is maintained with a +15V supply.

Maxim's MAX514 uses low tempco thin-film resistors laser trimmed to ±1/4 LSB linearity and better than ±1 LSB gain accuracy. The digital inputs are protected against electrostatic discharge (ESD) damage and can typically withstand over 5,000V of ESD voltages.

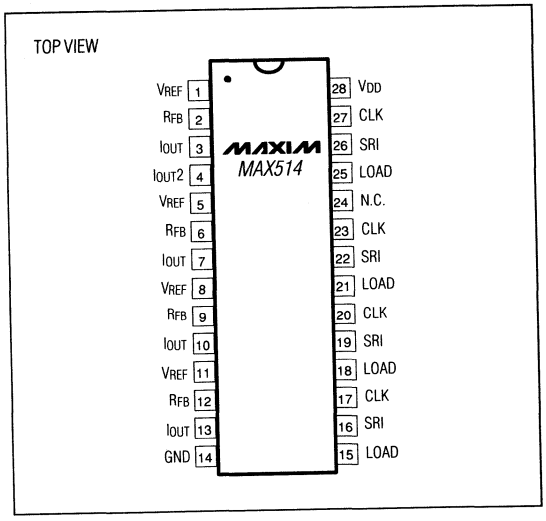
Applications

Automatic Calibration
Motion Control Systems
µP Controlled Systems
Programmable Amplifiers/Attenuators
Digitally Controlled Filters

Features

- **Quad 12-Bit Accuracy in 28-Pin DIP or SO**
- **Fast 3-Wire Serial Interface**
- **Low INL and DNL (±1/2 LSB Max)**
- **Gain Accuracy to ±1 LSB Max**
- **Low Gain Tempco (5ppm/°C Max)**
- **Operates with +5V or +15V Supplies**
- **ESD Protected**

Pin Configuration



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19-4446; Rev. 0; 8/91

MAXIM

Quad Comparator with Programmable Threshold

General Description

The MAX516 combines four low-power, programmable-threshold comparators on a single CMOS IC. Separate 8-bit digital-to-analog converters (DACs) drive the comparator inverting (-) inputs so that individual trip thresholds can be digitally set. All noninverting (+) comparator inputs are brought out as analog inputs (AIN0-AIN3). Each comparator output swings high when its analog input exceeds its digitally set threshold. All four DACs share a common reference input to optimize matching and eliminate external trims.

Digital inputs and comparator outputs are compatible with TTL and CMOS logic. A separate logic supply (V_{CC}) allows comparator output levels to be set independently of V_{DD}. The MAX516 operates conveniently from a single supply with V_{DD} tied to V_{CC}. Commercial, extended, and military temperature ranges are provided in 24-pin narrow DIP and wide SO packages.

Applications

Window Comparators

Power-Supply Monitors

Alarm Limit Detectors

Battery Chargers

Automated Test Equipment

Process Control

Features

- ♦ 4 Comparators and 4 DACs
- ♦ Digitally Set Threshold
- ♦ Monotonic Over Temperature
- ♦ Parallel Microprocessor Interface
- ♦ +5V to +15V Supply Operation

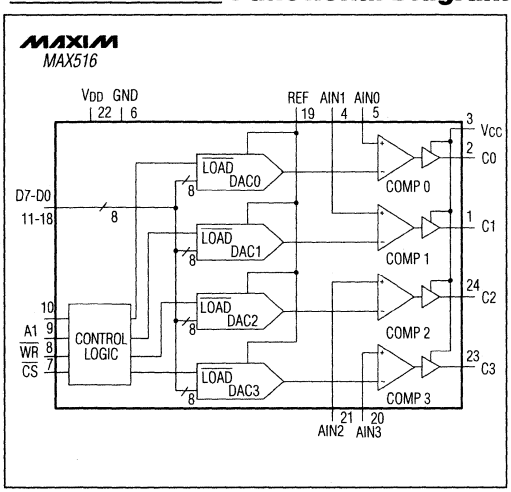
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX516ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX516BCNG	0°C to +70°C	24 Narrow Plastic DIP	±2
MAX516ACWG	0°C to +70°C	24 Wide SO	±1
MAX516BCWG	0°C to +70°C	24 Wide SO	±2
MAX516BC/D	0°C to +70°C	Dice*	±2
MAX516AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX516BENG	-40°C to +85°C	24 Narrow Plastic DIP	±2
MAX516AEWG	-40°C to +85°C	24 Wide SO	±1
MAX516BEWG	-40°C to +85°C	24 Wide SO	±2
MAX516AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX516BMRG	-55°C to +125°C	24 Narrow CERDIP**	±2

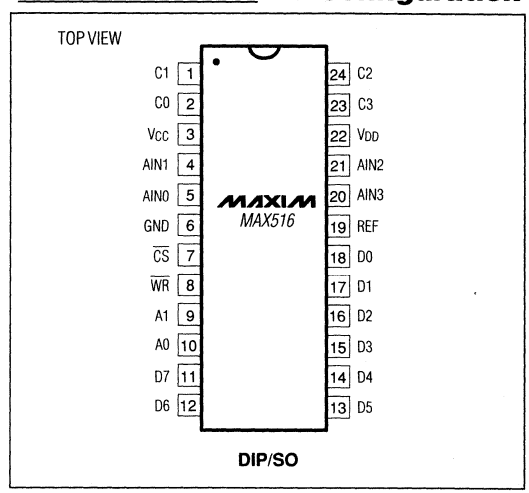
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



Quad Comparator with Programmable Threshold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . -0.3V, +17V
V_{CC} to GND . . . . . -0.3V, V_{DD} + 0.3V
V_{DD} to V_{CC} . . . . . -0.3V, +17V
Digital Input Voltage to GND . . . . . -0.3V, V_{DD} + 0.3V
REF to GND . . . . . -0.3V, V_{DD} + 0.3V
Comparator Input to GND . . . . . -0.3V, V_{DD} + 0.3V
C0–C3 to GND (Note 1) . . . . . GND, V_{CC} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 8.7mW/°C above +70°C) 480mW
Wide SO (derate 11.8mW/°C above +70°C) 650mW
Narrow CERDIP (derate 12.5mW/°C above +70°C) . 690mW

Operating Temperature Ranges:
MAX516_ C__ . . . . . 0°C to +70°C
MAX516_ E__ . . . . . -40°C to +85°C
MAX516_ MRG . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +165°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Note 1: The outputs may be shorted to GND or V_{DD}, provided the package's power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error	TUE	MAX516A				±1	LSB
		MAX516B				±2	
Relative Accuracy	INL	MAX516A				±0.5	LSB
		MAX516B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Full-Scale Error		MAX516A				±0.5	LSB
		MAX516B				±1	
Full-Scale Temperature Coefficient		V_{DD} = 15V, REF = 10V			±5		ppm/°C
Zero-Code Error		T_A = +25°C	MAX516A			±5	mV
		T_A = T_{MIN} to T_{MAX}				±10	
		T_A = +25°C	MAX516B			±10	
		T_A = T_{MIN} to T_{MAX}				±15	
Zero-Code Temperature Coefficient					±30		µV/°C
REFERENCE INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Reference Input Range	REF			1.25		V_{DD} -3.50	V
Reference Input Resistance	RREF	Worst-case code		3.0	4.5		kΩ
Reference Input Capacitance	CREF	Worst-case code (Note 2)			100	250	pF
COMPARATOR INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Comparator Input Range	V_{AIN}			0		V_{DD}	V
Comparator Input Bias Current	I_B	T_A = +25°C			50	300	nA
		T_A = T_{MIN} to T_{MAX}			100	400	

ELECTRICAL CHARACTERISTICS (continued)

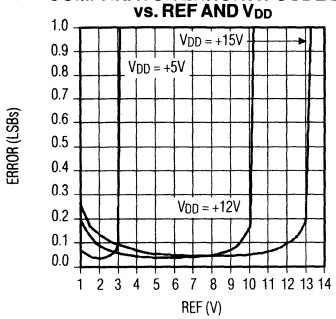
(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS D0-D7, $\overline{WR}$, $\overline{CS}$, (4.75V ≤ V_{DD} ≤ 16.5V)						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 2)			10	pF
DIGITAL OUTPUTS C0–C3 (V_{CC} = 5V)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	V_{CC}-1			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE (1.25V ≤ REF ≤ V_{DD} -3.5V, 0V ≤ AIN < V_{DD} -2V)						
Digital Input to Comparator Out Delay	t_{DCO}	(Note 3)		0.8	2.0	µs
Analog Input to Comparator Out Delay	t_{ACO}	(Note 4)		0.8	1.5	µs
TIMING CHARACTERISTICS						
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}		0			ns
Address to $\overline{WR}$ Setup Time	t_{AS}		50	30		ns
Address to $\overline{WR}$ Hold Time	t_{AH}		5	0		ns
Data Valid to $\overline{WR}$ Setup Time	t_{DS}		50	30		ns
Data Valid after $\overline{WR}$ Hold Time	t_{DH}		5	0		ns
$\overline{WRITE}$ Pulse Width	t_{WR}		120	50		ns
POWER SUPPLIES						
V_{DD} Range	V_{DD}		4.75		16.5	V
V_{CC} Range	V_{CC}		4.75		V_{DD}+0.30	V
Positive Supply Current	I_{DD}	Logic inputs < V_{IL} or > V_{IH}			10	mA
Logic Supply	I_{CC}				10	µA

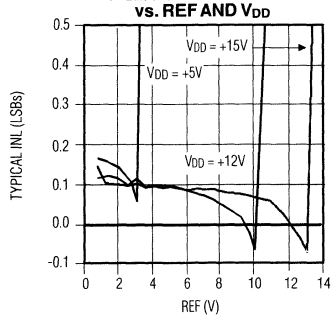
Note 2: Guaranteed by design. Not production tested.
Note 3: V_{DD} = 5.00V, differential comparator input voltage changes by 1.25V with 5mV overdrive. V_{IN} must be 3.5V less than V_{DD}, or longer propagation delays will result.
Note 4: Not tested, but guaranteed by correlation to t_{DCO}.

Typical Operating Characteristics

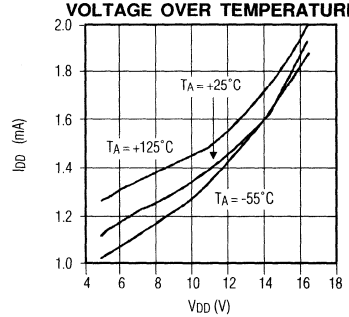
COMPARATOR ERROR AT CODE 255 vs. REF AND V_{DD}



RELATIVE ACCURACY vs. REF AND V_{DD}



SUPPLY CURRENT vs. SUPPLY VOLTAGE OVER TEMPERATURE



Quad Comparator with Programmable Threshold

Pin Description

PIN	NAME	FUNCTION
1, 2	C1, C0	Comparator Outputs
3	V_{CC}	Comparator Output Supply
4, 5	AIN1, AIN0	Comparator Analog Inputs
6	GND	Ground
7	$\overline{CS}$	CHIP SELECT
8	$\overline{WR}$	WRITE
9, 10	A1 , A0	DAC Address Inputs
11-18	D7-D0	DAC Data Inputs, 8 bits
19	REF	Reference Input
20, 21	AIN3, AIN2	Comparator Analog Inputs
22	V_{DD}	Positive Supply Voltage
23, 24	C3, C2	Comparator Outputs

Detailed Description

The MAX516 contains four analog comparators and four matched 8-bit digital-to-analog converters (DACs). The voltage output of each DAC is expressed in the equation:

$$V_{DAC} = REF \times N/256,$$

where N is the numerical equivalent of the 8-bit DAC input code (D0-D7). N ranges from 0 to 255 and may be set to a different level for each DAC (Table 1). The DAC output, V_{DAC}, does not appear on an output pin of the MAX516 but is instead compared to an analog input signal by one of four internal comparators (see *Functional Diagram*). A comparator output is high when AIN is more positive than the comparator's digitally set threshold.

Table 1. Comparator Threshold vs. DAC Input Code

DAC CODE MSB	DAC CODE LSB	COMPARATOR THRESHOLD
1111	1111	$+REF\left(\frac{255}{256}\right)$
1000	0001	$+REF\left(\frac{129}{256}\right)$
1000	0000	$+REF\left(\frac{128}{256}\right) = +\frac{REF}{2}$
0111	1111	$+REF\left(\frac{127}{256}\right)$
0000	0001	$+REF\left(\frac{1}{256}\right)$
0000	0000	0V

NOTE: $1LSB = (REF)(2^{-8}) = +REF\left(\frac{1}{256}\right)$

Reference Input

Comparator trip thresholds vary digitally between 0V and 1LSB below REF. All DACs share the same reference input.

The input impedance of REF is code dependent. The lowest impedance, typically 2kΩ, occurs when 0101 0101 (HEX 55) is loaded into D0-D7 on all four DACs. When 0000 0000 is loaded into all DACs, REF appears as an open circuit. Because the input resistance at REF is code dependent, the reference source should have an output impedance of no more than 4Ω to maintain linearity. Input capacitance at REF is also code dependent and typically varies between 100pF and 250pF.

Comparator Inputs

The "+" input of each comparator is brought out to AIN0-AIN3. Comparator input bias current is typically 100nA. Analog source resistances below 1.25kΩ generate less than 250µV of bias-current induced comparator offset error.

Digital Interface

The digital inputs (D0-D7, $\overline{CS}$, $\overline{WR}$) are both TTL and 5V CMOS logic compatible; however, the power-supply current, I_{DD}, depends on input logic levels. Supply currents will be highest with TTL levels (tested limits are with worst-case logic levels). Supply current is reduced when digital inputs are driven near GND and above 4V.

Address lines A0 and A1 select which DAC receives data from the input port. Because $\overline{CS}$ and $\overline{WR}$ are internally ORed, the write cycle begins only after both go low, but data is latched and transferred to a DAC when either input returns high. Figure 1 shows the input control logic, Table 2 lists DAC addresses, and Table 3 is the truth table for $\overline{WR}$ and $\overline{CS}$. Figure 2 shows write-cyle timing.

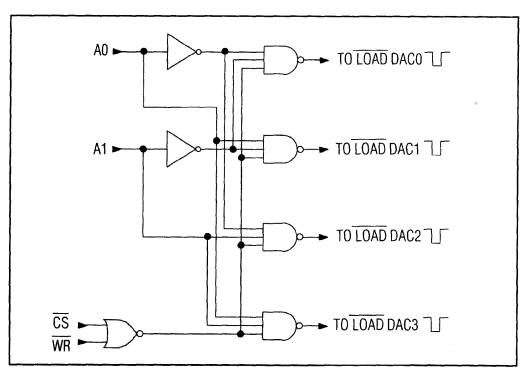


Figure 1. Input Control Logic

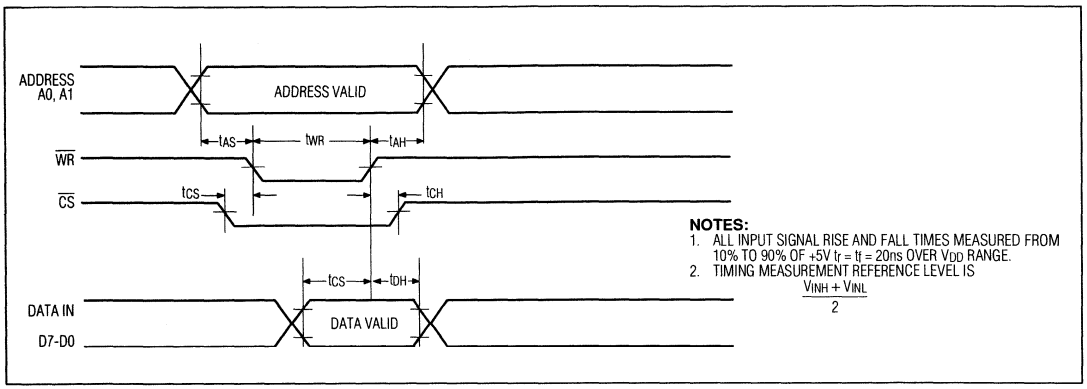


Figure 2. Write-Cycle Timing

Table 2. DAC Addressing

A1	A0	SELECTED DAC
0	0	DAC0 Input Register
0	1	DAC1 Input Register
1	0	DAC2 Input Register
1	1	DAC3 Input Register

Table 3. Write-Cycle Truth Table

$\overline{CS}$	$\overline{WR}$	FUNCTION
1	X	No operation. The MAX516 is deselected. Existing register contents remain unchanged.
0	0	DAC contents for selected address are loaded, but do not update the DAC until $\overline{WR}$ goes high.
0	↑	Latch D0-D7 into input register of the selected DAC on rising edge.

NOTES: X = Don't Care, ↑= Rising Edge

Applications Information

Power-Supply and Reference Operating Ranges

The MAX516 is fully specified to operate with V_{DD} between +4.75V and +16.5V and is specified to operate with a reference input range of +1.25V to V_{DD} -3.5V.

The comparator output supply, V_{CC}, has a range of +4.5V to (V_{DD} + 0.3V). This allows the comparators' logic-high output levels to be set independently from V_{DD}. In most applications, simply connect V_{CC} and V_{DD} together. Comparator outputs typically swing within 200mV of the supply rails when loaded with CMOS logic inputs.

Hysteresis

When analog input signals are slow moving or contain noise, comparator outputs may "chatter" near the threshold point. Be sure that proper power-supply bypass capacitors are in place (see *Grounds and Bypassing* section), because supply current rises when an output switches.

Hysteresis may be added to any or all comparators to further resist oscillation during output transitions. This is accomplished with two resistors, as shown in Figure 3. When hysteresis is added, the threshold point will shift slightly as a result of the voltage divider formed by R1 and R2. The amount of shift is described below:

$$V_{TH} = V_T\left(\frac{R1}{R2} + 1\right)$$

$$V_{TL} = V_T\left(\frac{R1}{R2} + 1\right) - V_{CC}\left(\frac{R1}{R2}\right)$$

$$V_{HYST} = V_{TH} - V_{TL}$$

$$V_{HYST} = V_{CC}\left(\frac{R1}{R2}\right)$$

V_T is the threshold voltage set by the internal DAC with no hysteresis connected. V_{TH} is the shifted high-going threshold with hysteresis added. V_{TL} is the shifted low-going threshold with hysteresis. V_{HYST} is the total hysteresis and equals V_{TH} - V_{TL}. Note that V_{TL} and V_{HYST} change with V_{CC}. With V_{CC} = 5V, R1 = 1kΩ, and R2 = 200kΩ, V_{HYST} = 25mV. Even though R1 is relatively small, the impedance seen by the signal source is large: R1 + R2. However, if R1 is large, input bias current (400nA

Quad Comparator with Programmable Threshold

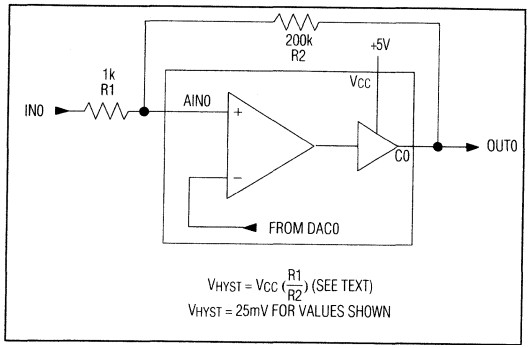


Figure 3. Adding Hysteresis to Any Comparator

max over temp.) may add offset error. 1kΩ x 400nA = 0.4mV offset error is due to bias current.

Grounds and Bypassing

Careful PC-board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate AIN0-AIN3 and REF from each other by running a ground trace between these pins.

Bypass both V_{DD} and V_{CC} to GND with a combination of a 0.1µF low ESR and a 4.7µF capacitor close to the device. If V_{DD} and V_{CC} are connected together, only one set of bypass capacitors is needed. If REF is not an AC input, it should be bypassed as well. Keep bypass-capacitor leads short for best supply noise rejection.

Applications

Threshold detection is often useful in automated test applications. Four individual thresholds can be independently altered under software control.

Figure 4 shows the connection for a hardware window comparison. DAC0 provides the upper trip point, DAC1 the lower trip point. The difference between the trip points is the window size. The AIN0 and AIN1 inputs are tied together. One logic output is inverted and then ORed with the noninverted comparator output. The window output goes high when the analog input sits between the thresholds set by DAC0 and DAC1. The external logic in Figure 4 can also be simulated in software, or use a single comparator to perform a window comparison by loading two threshold limits in succession and noting the comparator results of each (Figure 5).

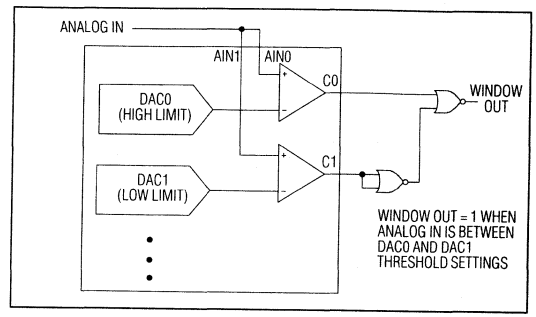


Figure 4. Window Comparison

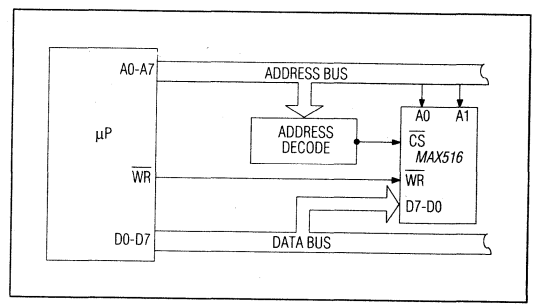
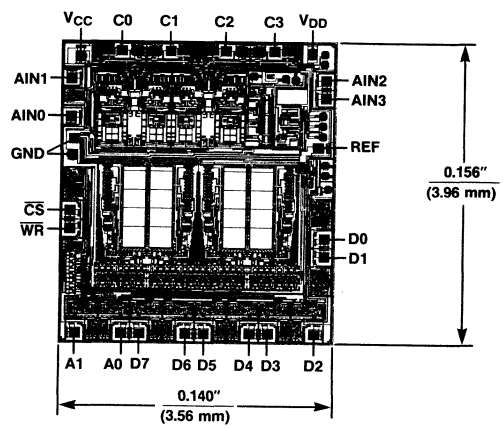


Figure 5. Microprocessor Interface

Chip Topography



NOTE: Substrate connected to V_{DD}

ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

CMOS Quad 12-Bit Voltage Output D/A Converter

General Description

The MAX526 contains four 12-bit, voltage-output digital-to-analog converters (DACs). Precision output buffer amplifiers are included on-chip to provide voltage outputs while reducing external component count. 12-bit performance is achieved over the full operating temperature range without external trimming.

This device features double buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. The MAX526 has an 8-bit wide data bus. Data is loaded into the input register using 2 write operations; an 8-bit LSB load and a 4-bit MSB load. An asynchronous $\overline{LDAC}$ input transfers data from the input register to the DAC register. All logic inputs are TTL and CMOS compatible.

The MAX526 is available in a 24 pin, 300 mil wide plastic DIP or CERDIP and a 24 pin, 300 mil wide SOIC package.

Applications

Minimum Component Count Analog Systems

Digital Offset/Gain Adjustment

Arbitrary Function Generators

Industrial Process Control

Automatic Test Equipment

Features

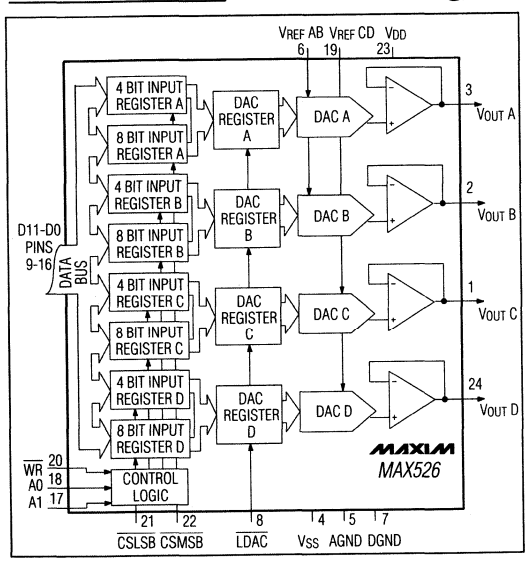
- ♦ **Buffered Voltage Output**
- ♦ **Double Buffered Digital Inputs**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **Requires No External Adjustments**

Ordering Information

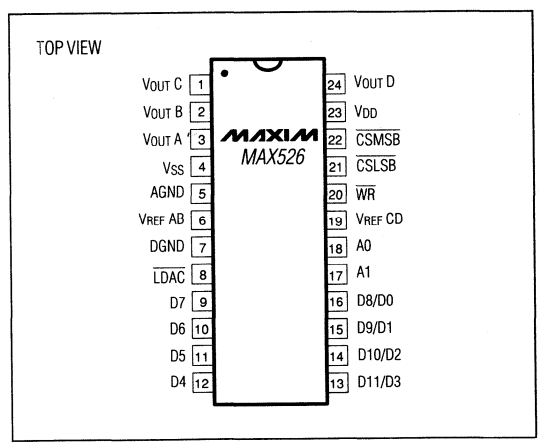
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX526CPG	0°C to +70°C	24 Plastic DIP	±1
MAX526CWG	0°C to +70°C	24 Wide SO	±1
MAX526C/D	0°C to +70°C	Dice*	±1
MAX526EPG	-40°C to +85°C	24 Plastic DIP	±1
MAX526ERG	-40°C to +85°C	24 Narrow CERDIP	±1
MAX526EWG	-40°C to +85°C	24 Wide SO	±1
MAX526MRG	-55°C to +125°C	24 Narrow CERDIP†	±1

** Contact factory for dice specifications.*
† /883

Functional Diagram



Pin Configuration



ADVANCE INFORMATION

First Page of Data Sheet in Preparation

MAXIM

Octal, 8-Bit, Serial DAC

MAX528

General Description

The MAX528 is an octal, 8-bit, voltage-output digital-to-analog converter (DAC) with serial interface and two sets of reference inputs. It operates from single +5V to +15V supplies or split supplies including +5V/-5V, and +5V/-15V.

Three output modes are serially programmable for each of eight analog outputs. The unbuffered mode connects the internal R-2R DAC network directly to the output pin, reducing power consumption and avoiding buffer DC errors. The full-buffer mode inserts a buffer between the R-2R network and the output, allowing +5mA to -2mA output currents to be generated. The half-buffer mode inserts a buffer allowing +5mA output drive and 0mA sink current. This mode uses less power and provides output swings to ground with single supply operations.

Serial data can be "daisy-chained" from one chip to another. On power-up, all data bits are set to zero and analog outputs are put in the unbuffered mode. The MAX528 has a shutdown pin to reduce current consumption to under 50µA, while retaining all internal register data.

Applications

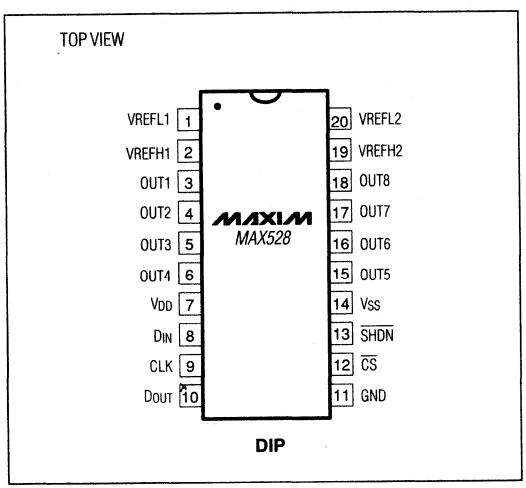
Digital Gain and Offset Adjustment

Microprocessor-Controlled Set Points

Digital Calibration

Trimming

Pin Configuration



Features

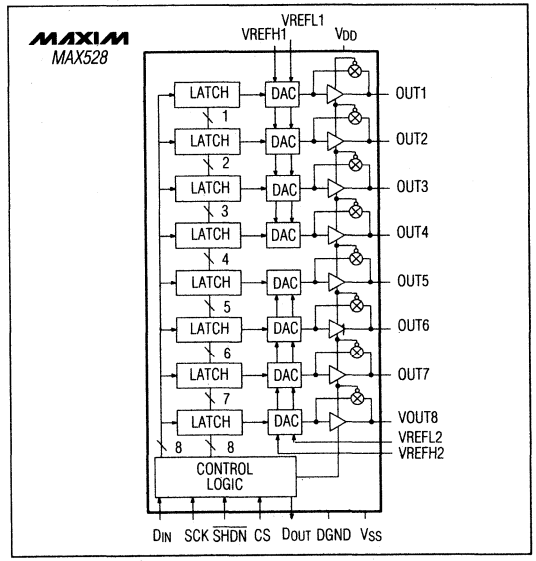
- ♦ **8 Outputs**
- ♦ **2 Reference Inputs**
- ♦ **Serial Interface I/P and O/P**
- ♦ **Shutdown with Memory**
- ♦ **DAC or Buffered DAC Outputs**
- ♦ **Single or Dual Supplies**
- ♦ **CMOS and TTL Compatible Inputs**
- ♦ **±1/2LSB Full-Scale Error**
- ♦ **20-Pin or 24-Pin SO Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX528CPP	0°C to +70°C	20 Plastic DIP
MAX528CWG	0°C to +70°C	24 SO
MAX528C/D	0°C to +70°C	Dice*
MAX528EJP	-40°C to +85°C	20 CERDIP
MAX528EWG	-40°C to +85°C	24 SO
MAX528MJP	-55°C to +125°C	20 CERDIP

** Contact factory for dice specifications.*

Functional Diagram



9

MAXIM

CMOS 12-Bit Serial Input Multiplying D/A Converter

General Description

The MAX543 is a 12-bit current-output multiplying digital-to-analog converter (DAC) that is packaged in a space-saving 8-pin DIP or 16-pin surface mount SO. Its 3-wire serial interface saves additional circuit board space and also results in low power dissipation. When used with microprocessors (μP) with a serial port, the MAX543 minimizes the digital noise feed-through from its input pins to its output. The serial port can be used as a dedicated analog bus and kept inactive while the MAX543 is in use. Serial interfacing also reduces the complexity of opto- or transformer-isolated applications.

The MAX543 contains a 12-bit R-2R type DAC, a serial-in parallel-out shift register, a DAC register and control logic. On the rising edge of the clock (CLK) pulse the serial input (SRI) data is shifted into the MAX543. When all the data is clocked in, it is transferred into the DAC register by taking the LOAD input low.

The MAX543 is specified both with a single +5V and +15V power supply. With a +5V supply, the digital inputs are TTL and +5V CMOS compatible. High voltage CMOS compatibility is maintained with a +15V supply.

Maxim's MAX543 uses low tempco thin-film resistors laser trimmed to ±1/4 LSB linearity and better than ±1 LSB gain accuracy. The digital inputs are protected against electrostatic discharge (ESD) damage and can typically withstand over 5,000V of ESD voltages.

Applications

Automatic Calibration

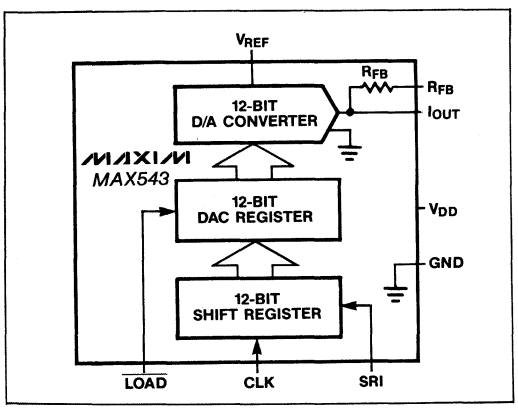
Motion Control Systems

μP Controlled Systems

Programmable Amplifiers/Attenuators

Digitally Controlled Filters

Functional Block Diagram



Features

- ♦ 12-Bit Accuracy in 8-Pin Mini-DIP
- ♦ Fast 3-Wire Serial Interface
- ♦ Low INL and DNL (±1/2 LSB Max)
- ♦ Gain Accuracy to ±1 LSB Max
- ♦ Low Gain Tempco (5ppm/°C Max)
- ♦ Operates with +5V or +15V Supplies
- ♦ TTL/CMOS Compatible
- ♦ ESD Protected

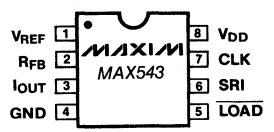
Ordering Information

PART	TEMP. RANGE	PACKAGE	LINEARITY
MAX543ACPA	0°C to +70°C	Plastic DIP	±1/2 LSB
MAX543BCPA	0°C to +70°C	Plastic DIP	±1 LSB
MAX543ACWE	0°C to +70°C	Wide SO	±1/2 LSB
MAX543BCWE	0°C to +70°C	Wide SO	±1 LSB
MAX543AEWE	-40°C to +85°C	Wide SO	±1/2 LSB
MAX543BEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX543BC/D	0°C to +70°C	Dice	±1 LSB
MAX543AEJA	-40°C to +85°C	CERDIP	±1/2 LSB
MAX543BEJA	-40°C to +85°C	CERDIP	±1 LSB
MAX543AMJA	-55°C to +125°C	CERDIP	±1/2 LSB
MAX543BMJA	-55°C to +125°C	CERDIP	±1 LSB

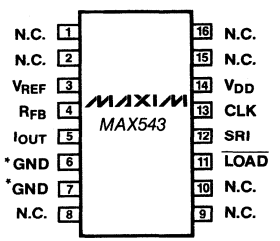
All DIP packages are 8 leads; all SO packages are 16 leads.

Pin Configurations

Top View



DIP



SO

* Leads 6 and 7 must be connected together as close to the package as possible.

CMOS 12-Bit Serial Input Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
V_{IOUT} to GND ..... -0.3V, V_{DD} + 0.3V
Power dissipation to +75°C (any package) 470mW
Derate above +75°C by ..... 6mW/°C

Operating Temperature Ranges
MAX543AC/BC ..... 0°C to 70°C
MAX543AE/BE ..... -40°C to +85°C
MAX543AM/BM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{IOUT} = GND = 0V; over specified temperature range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL			MAX543A MAX543B			±1/2 ±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits over temperature		MAX543A MAX543B			±1/2 ±1	LSB
Gain Error	FSE	Using internal R_{FB}	T_A = +25°C	MAX543A MAX543B			±1 ±2	LSB
			$T_A = T_{MIN}$ to T_{MAX}	All			±2	
Gain Tempco ΔGain/ΔTemp (Note 1)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD} = ±5%.					±0.001	%/%
DYNAMIC PERFORMANCE (Note 1)								
Current Settling Time	t_S	To 1/2LSB. I_{OUT} load is 100Ω|| 13pF. DAC register alternately loaded with all 1s and all 0s.	T_A = +25°C			0.25	1	μs
Digital to Analog Glitch	Q	V_{REF}= 0V. I_{OUT} load is 100Ω||13pF. DAC register alternately loaded with all 1s and all 0s.				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	V_{REF} = ±10Vp-p at 10kHz. DAC register loaded with all 0s.				0.4	1	mVp-p
Total Harmonic Distortion	THD	V_{REF} = 6V_{rms} at 1kHz. DAC register loaded with all 1s.				-85		dB
Output Noise Voltage Density	en	10Hz to 100kHz. Measured between R_{FB} and I_{OUT}.				13	15	nV/Hz
REFERENCE INPUT								
Input Resistance	RREF	V_{REF} pin to I_{OUT}			7	11	15	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{IOUT} = GND = 0V; over specified temperature range unless otherwise noted.)

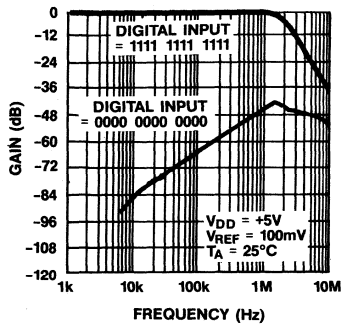
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUT								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s.	T_A = +25°C			±0.5	±5	nA
			$T_A = T_{MIN}$ to T_{MAX}	MAX543AC/BC/AE/BE			±25	
				MAX543AM/BM			±100	
I_{OUT} Capacitance (Note 1)	C_{OUT}	DAC register loaded with all 0s.				55	80	pF
		DAC register loaded with all 1s.				85	110	
DIGITAL INPUTS								
Input High Voltage	V_{IH}		V_{DD} = +5V V_{DD} = +15V		2.4 13.5			V
Input Low Voltage	V_{IL}		V_{DD} = +5V V_{DD} = +15V				0.8 1.5	V
Input Leakage Current	I_{IN}	Digital Inputs at 0V or V_{DD}					±1	µA
Input Capacitance (Note 1)	C_{IN}	Digital Inputs at 0V or V_{DD}					8	pF
SWITCHING CHARACTERISTICS (Note 2)								
CLK Pulse Width High	t_{CH}				90			ns
CLK Pulse Width Low	t_{CL}				120			ns
SRI Data to CLK Setup	t_{DS}				40			ns
SRI Data to CLK Hold	t_{DH}				80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}				120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}				0			ns
$\overline{LOAD}$ High to CLK	t_{LC}				0			ns
POWER SUPPLY								
V_{DD} Range	V_{DD}		V_{DD} = +12V or +15V V_{DD} = +5V		+11.4 +4.75		+15.75 +5.25	V
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH}					500	µA
		All digital inputs at 0V or V_{DD}				5	100	

Note 1: Guaranteed by design and not subject to test.
Note 2: Sample tested at +25°C to ensure compliance.

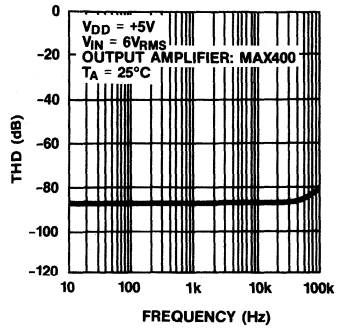
CMOS 12-Bit Serial Input Multiplying D/A Converter

Typical Operating Characteristics

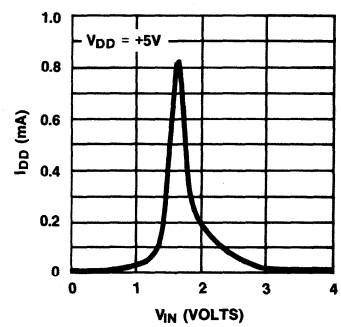
GAIN vs FREQUENCY (OUTPUT AMPLIFIER: MAX400)



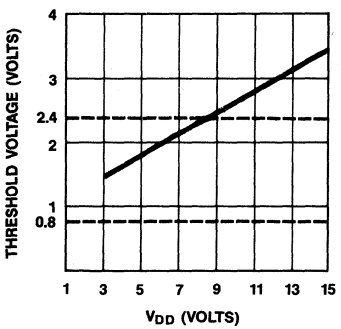
TOTAL HARMONIC DISTORTION vs FREQUENCY (MULTIPLYING MODE)



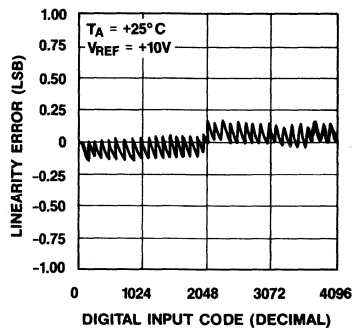
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



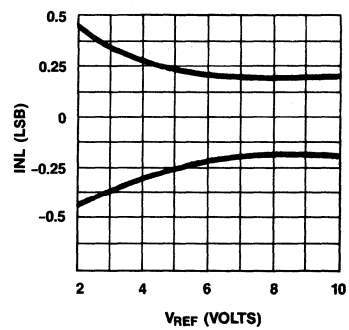
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



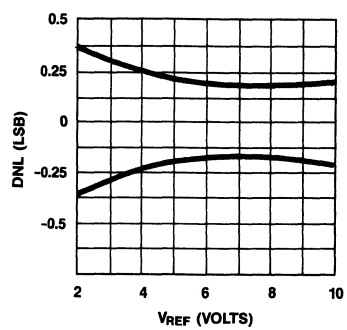
LINEARITY ERROR vs DIGITAL CODE



LINEARITY ERROR vs REFERENCE VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



Detailed Description

D/A Converter

The MAX543 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binary weighted currents are switched to either I_{OUT} or GND depending on the status of each input data bit. Although the current at I_{OUT} and GND depends on the digital input code, the sum of the two output currents are always equal to the input current at V_{REF}.

The current output I_{OUT} can be converted into a voltage by adding an external output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT} pin output capacitance, C_{OUT}, is code dependent and is typically 55pF with all switches to GND and 85pF with all switches to I_{OUT}.

Digital Circuit

Figure 2 shows the timing diagram for the MAX543. The MSB is always loaded first on the rising edge of clock. When all the data is shifted into the MAX543, the DAC register is loaded by taking the LOAD signal low. The DAC register is transparent when LOAD is low and latched when LOAD is high. If the LOAD signal is taken low before the LSB bit is fully shifted into the shift register, the DAC output can produce a "glitch". If this is undesirable, the LOAD signal can be delayed 30ns after the rising edge of the LSB clock edge to avoid this condition.

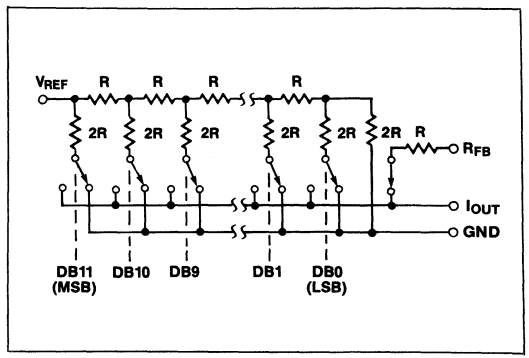


Figure 1. Simplified D/A Circuit of MAX543

The input buffer inverters of the MAX543 act as level shifters converting TTL levels into CMOS logic levels. These input buffers are TTL and +5V-CMOS compatible (0.8V and 2.4V) at V_{DD} = +5V. For V_{DD} = +15V the input buffers are CMOS compatible (1.5V and 13.5V). At this supply voltage the input buffers are in their linear region when the input voltages are between 1V and 6V. Therefore to minimize high supply currents, the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and GND) as possible.

Circuit Configurations

Unipolar Operation

Basic application of the MAX543 is shown in Figure 3. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

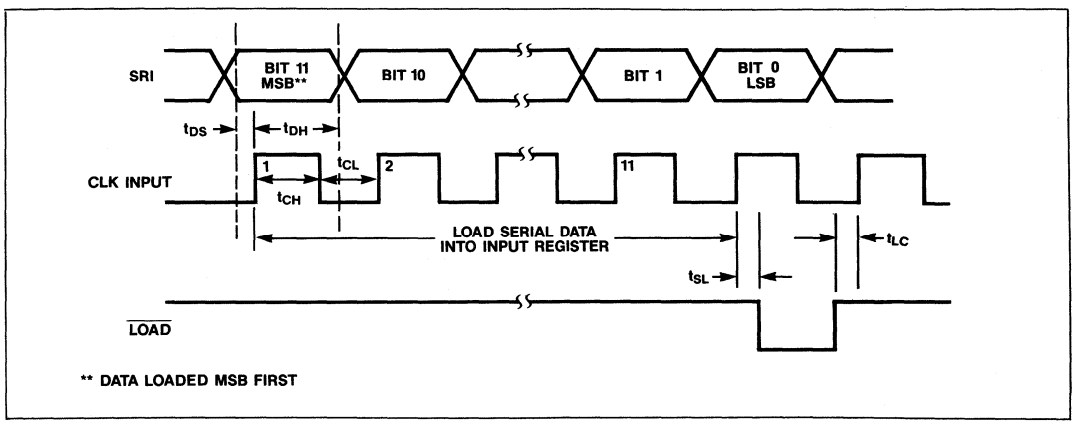


Figure 2. Write Cycle Timing Diagram

CMOS 12-Bit Serial Input Multiplying D/A Converter

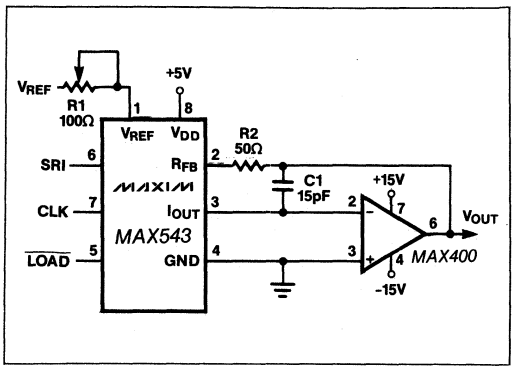


Figure 3. Unipolar Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

In many applications gain adjustment will not be necessary since the gain accuracy of the part is sufficient, or the gain is trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. When trimming is used, and the DAC is operated over a wide temperature range, then low tempco (< 300ppm/°C) resistors should be used for R1 and R2.

The capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the output of the DAC.

Bipolar Operation

Figure 4 shows the MAX543 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4 and R5) are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In

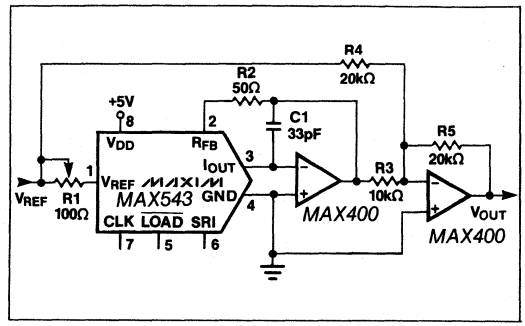


Figure 4. Bipolar Operation

Table 2. Offset Binary Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 3. 2's Complement Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MAX543 work with 2's complement coding. Table 3 shows the code relationships to output voltage for the 2's complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using parts with a guaranteed maximum ±1 LSB gain error. In these cases, the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single Supply Operation (Voltage Mode)

The MAX543 can be conveniently used in single supply (voltage mode) operation with I_{OUT} biased at any voltage between GND and V_{DD}. I_{OUT} must not be allowed to go 0.3V lower than the GND or 0.3V higher than V_{DD}. Otherwise, internal diodes would turn on causing a high current flow from the supply which could damage the device.

Figure 5 shows the MAX543 connected as a voltage output DAC. I_{OUT} is connected to the reference voltage source and GND is grounded. The DAC output, now appears at the V_{REF} pin which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the response time of the circuit depends on the behavior of the reference source with changing load conditions.

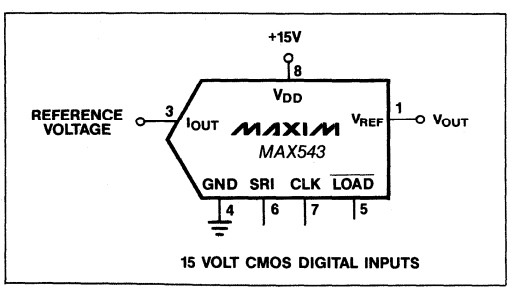


Figure 5. Single Supply Operation Using Voltage Switching Mode

Two advantages of the voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode.

MAX543 Opto-Isolated Application

Figure 6A shows the MAX543 interface to optocouplers for isolated barrier applications. Three optocouplers (OC1 thru OC3) carry the serial data and clocking signals across the isolation barrier. Isolated power sources, V^+ and V^-, supply the MAX543, the output amplifier and optocouplers. If data word updates are infrequent, and large analog output transitions can be tolerated while serial data is being clocked in, then parts count can be reduced by eliminating optocoupler OC3 and tying $\overline{LOAD}$ (pin 5) of the MAX543 low.

Using type 6N136 optocouplers this circuit accepts serial data at a maximum clock rate of 100kHz, or 130μs per data word. The SERIAL DATA and $\overline{LOAD}$ signals should change coincident with the falling edge of CLOCK, as shown in the timing diagram (Figure 6B). A positive CLOCK cycle is masked during the time that $\overline{LOAD}$ is low.

The MAX543 will also work with +5V isolated supplies using the optocoupler circuit of Figure 6A. The values of R1 through R3 should be changed to 3kΩ to maintain switching speed with the lower value of V^+.

Current drawn from V^- for the MAX543 and optocoupler is 3.5mA at 100kHz clock rate when all data bits are set to zero. V^+ current drops to zero (excluding reference and op amp current) when no new data is being loaded and CLOCK, SERIAL DATA, and $\overline{LOAD}$ are static high.

Microprocessor Interfacing

Interfacing to the 8085

Figure 7 shows the MAX543 interfacing to the 8085 microprocessor. The SOD line from the 8085 is used to send serial data to the DAC. This data is clocked into the MAX543 by executing memory write instructions. The CLK input for the DAC can be generated by decoding address 8000 and the $\overline{WR}$ signal. The data is transferred into the DAC register with a memory write instruction to address A000 which brings $\overline{LOAD}$ low. The data for the MAX543 is stored in the right-justified format in registers H and L of the 8085.

CMOS 12-Bit Serial Input Multiplying D/A Converter

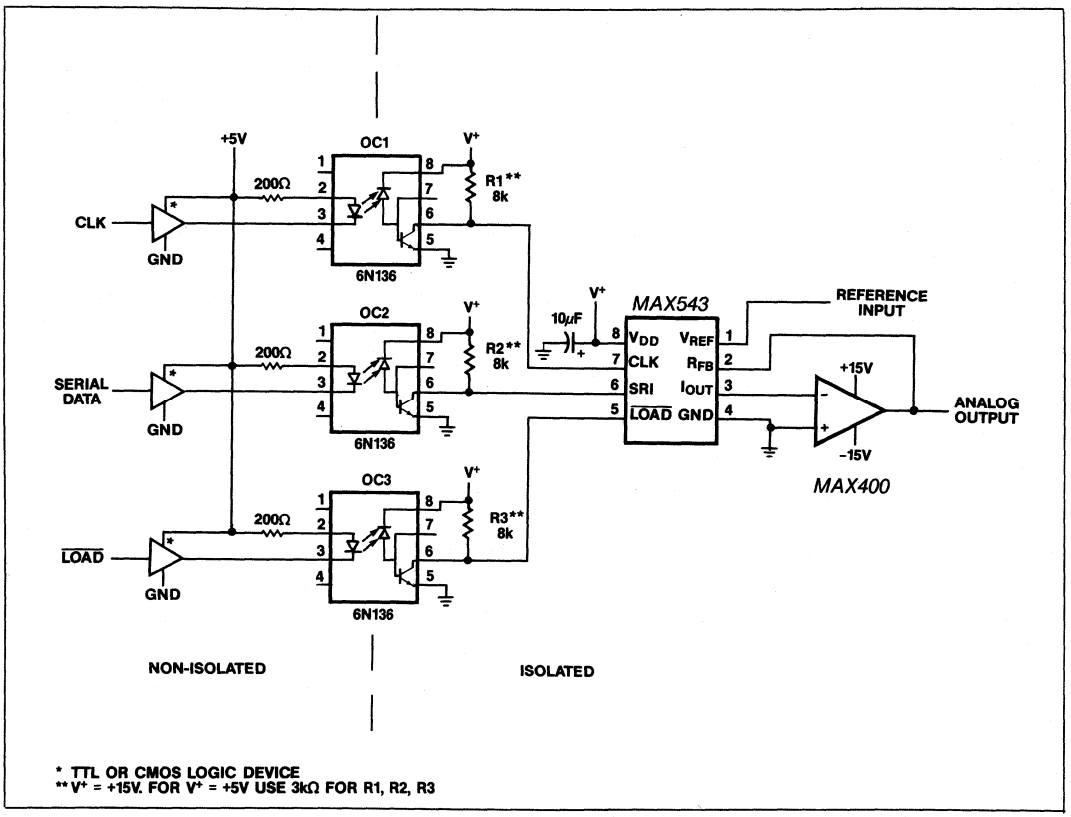


Figure 6A. MAX543 Opto-coupled Application

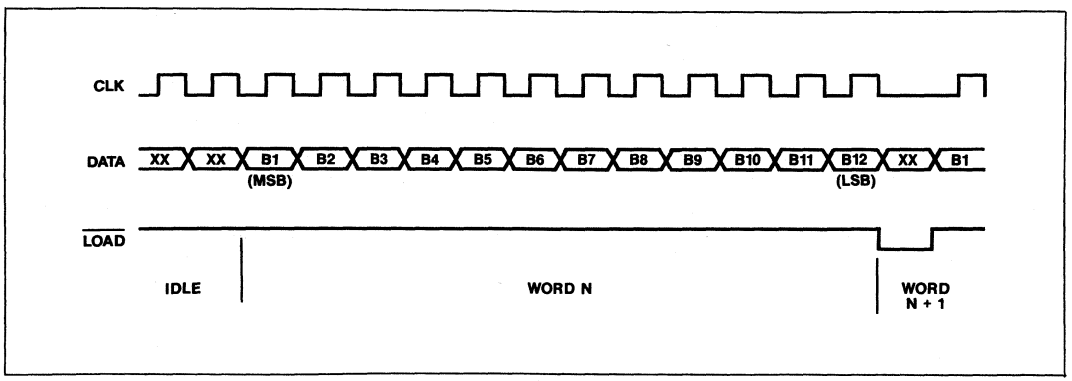


Figure 6B. MAX543 Opto-Isolated Timing

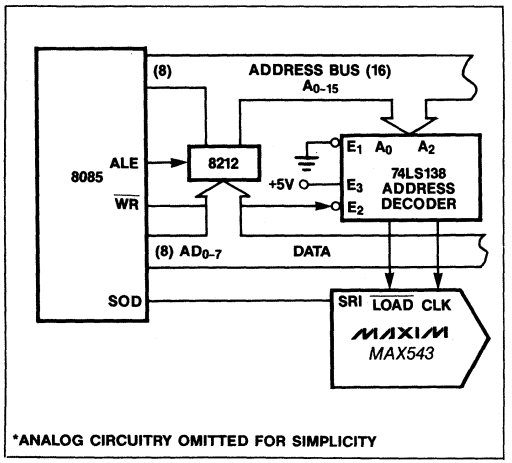


Figure 7. MAX543 - 8085 Interface

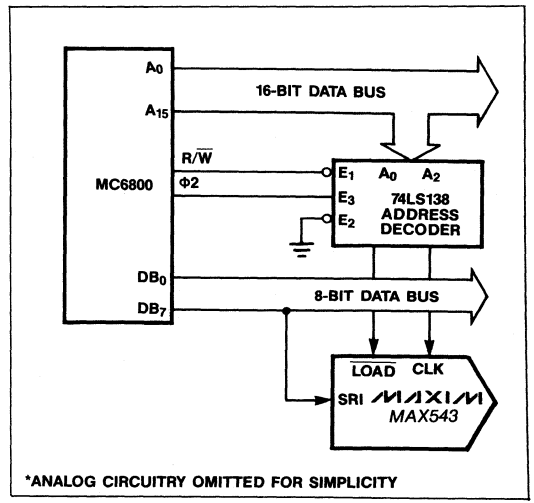


Figure 8. MAX543 - MC6800 Interface

Interfacing to the MC6800

Figure 8 shows the MAX543 interfacing to the MC6800 microprocessor. The data is transferred into the MAX543 by executing successive memory WRITE instructions while changing the data between WRITEs to construct the serial data to the DAC.

The DB7 data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 2000, R/$\overline{W}$, and 02 are decoded to generate the CLK signal for the DAC with each memory WRITE. Similarly, a memory WRITE to address 4000 transfers data into the DAC register by bringing the MAX543's $\overline{LOAD}$ input low.

Application Information

Output Amplifier Offset

For best linearity, I_{OUT} and GND should be terminated at exactly 0V. In most applications I_{OUT} is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will, therefore, degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10LSB.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should, therefore, be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to I_{OUT}. This normally is a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and I_{OUT} pins.

The DAC output follows the digital inputs when the $\overline{LOAD}$ pin is low. In this mode invalid outputs and voltage glitches can appear at the DAC output. Keeping the $\overline{LOAD}$ input high until all the data is shifted into the MAX543 eliminates this problem.

CMOS 12-Bit Serial Input Multiplying D/A Converter

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at I_{OUT} as low as possible.

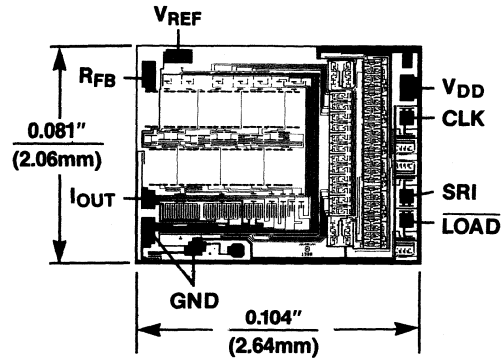
Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected across the DAC V_{DD} and GND as close to the pins as possible.

The MAX543 has high impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



Display Drivers/Counters

10

19-4452; Rev 0; 8/91

MAXIM

Serially Interfaced, 8-Digit LED Display Driver

General Description

The MAX7219 is a compact, serial input/output common-cathode display driver that interfaces microprocessors (µPs) to 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. Only one external resistor is required to set the segment current for all LEDs.

A convenient 3-wire serial interface connects to all common µPs. Individual digits may be addressed and updated without rewriting the entire display. The MAX7219 also allows the user to select code-B decoding or no-decode for each digit.

The MAX7219 includes a 150µA low-power shutdown mode, analog and digital brightness control, a scan-limit register which allows the user to display from 1 to 8 digits, and a test mode which forces all LEDs on.

Applications

Bar-Graph Displays

7-Segment Displays

Industrial Controllers

Panel Meters

LED Matrix Displays

Features

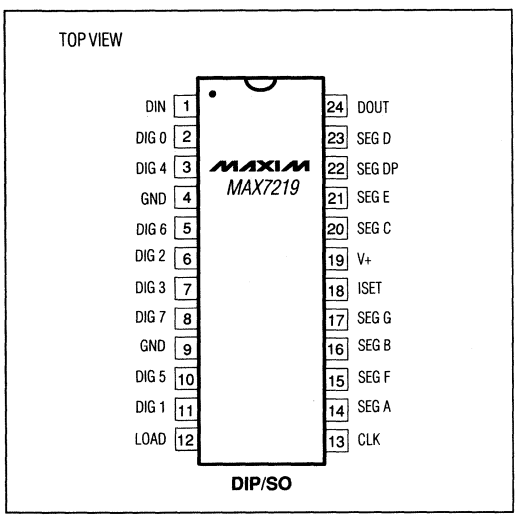
- ♦ **10MHz Serial Interface**
- ♦ **Individual LED Segment Control**
- ♦ **Decode/No-Decode Digit Selection**
- ♦ **150µA Low-Power Shutdown (Data Retained)**
- ♦ **Digital and Analog Brightness Control**
- ♦ **Display Blanked on Power-Up**
- ♦ **24-Pin DIP and SO Packages**
- ♦ **Drives Common-Cathode LED Display**

Ordering Information

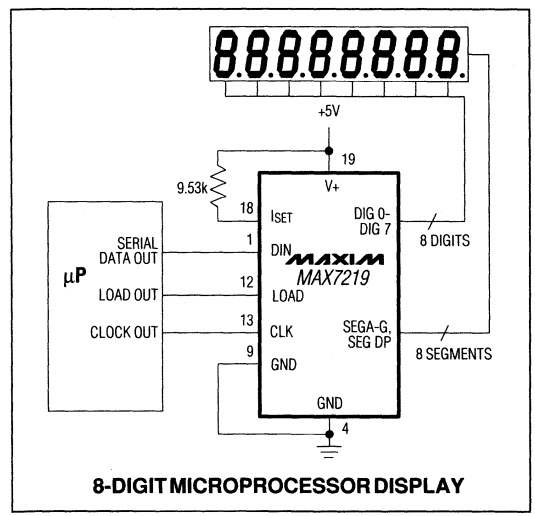
PART	TEMP. RANGE	PIN-PACKAGE
MAX7219CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX7219CWG	0°C to +70°C	24 Wide SO
MAX7219C/D	0°C to +70°C	Dice*
MAX7219ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX7219EWG	-40°C to +85°C	24 Wide SO
MAX7219ERG	-40°C to +85°C	24 Narrow CERDIP

* *Contact factory for dice specifications.*

Pin Configuration



Typical Application Circuit



Serially Interfaced, 8-Digit LED Display Driver

ABSOLUTE MAXIMUM RATINGS

V+ Voltage 7V
DIG0-DIG7 Sink Current 500mA
SEG A-G, DP Source Current 100mA
Input Voltage (any pin) ..... V+ + 0.3V to -0.3V
Continuous Power Dissipation (T_A = +85°C)
Narrow Plastic DIP 0.87W
Wide SO 0.76W
CERDIP 1.1W

Operating Temperature Ranges:
MAX7219C_G ..... 0°C to +70°C
MAX7219E_G ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

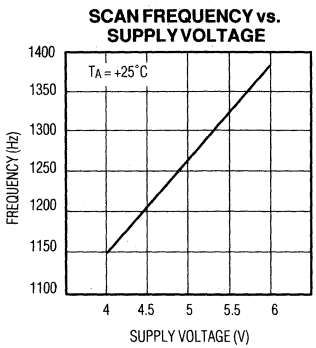
(V+ = 5V ±10%, R_{SET} = 9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

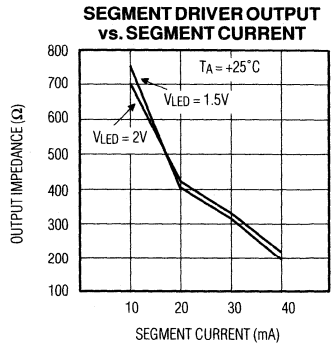
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		4.0		6.0	V
Shutdown Supply Current	I_Q	DIN,CLK and LOAD = GND or V+, shutdown register set to 0, T_A = +25°C			150	µA
Operating Supply Current	I_{OP}	R_{SET} = infinity			8	mA
		All segments and decimal points on, I_{SEGO} = -40mA		330		mA
Display Scan Rate	f_{OSC}	V+ = 5V, 8 digits scanned	500	1300	2000	Hz
Digit Drive Sink Current	I_{DIGI}	T_A = +25°C, V+ = 5V, V_{OUT} = 0.65V	320			mA
Segment Drive Current Source	I_{SEGO}	T_A = +25°C, V+ = 5V, V_{OUT} =V+ - 1V	-30	-37	-40	mA
Segment Drive Current Matching				3.0		%
Digit Drive Source Current	I_{DIGO}	Digit off, V_{OUT} = V+ - 0.3V	-2			mA
Segment Drive Current Sink	I_{SEGI}	Segment off, V_{OUT} = 0.3V	5			mA
LOGIC INPUTS						
Input Current	I	DIN, CLK and LOAD V_{IN} = 0V V_{IN} = V+			-1 1	µA
Logic 1 Input Voltage	V_{IH}		3.5			V
Logic 0 Input Voltage	V_{IL}				0.8	V
Hysteresis Voltage		DIN, CLK, and LOAD		1.0		V
Output High Voltage	V_{OH}	DOUT I_{OUT} = -1mA, I_{OUT} -1µA	V+-1.0	V+		V
Output Low Voltage	V_{OL}	DOUT, I_{OUT} = 1.6mA			0.4	V
Data-Hold Time DATAIN to Clock	t_{IDH}		0	-5		ns
Data-Setup Time DATAIN To Clock	t_{IDS}		25			ns
Clock-to-Serial Output Prop Delay	t_{OPD}	C_{LOAD} = 50pF			25	ns
Clock Low Time	t_{CKL}		50			ns
Clock High Time	t_{CKH}		50			ns
Data-to-Segment Prop Delay (Note 1)	t_{DSPD}	C_{LOAD} = 50pF	0		2.25	ms
Load-Rising Edge to Next Clock Rising Edge	t_{LDCK}		50			ns
Clock-to-Load Rising Edge Setup Time	t_{CKLD}		0			ns
Load Low Time	t_{LDL}		50			ns
Load High Time	t_{LDH}		50			ns

Note 1: Guaranteed by design.

Serially Interfaced, 8-Digit LED Display Driver

Typical Operating Characteristics





Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input. Data is loaded into an internal 16-bit shift register on the rising edge of CLK.
2, 3, 5-8, 10, 11	DIG0-7	8 digit drive lines that sink current from the display.
4, 9	GND	Ground (both GND pins must be connected)
12	LOAD	Load Data Input. On LOAD's rising edge, the last 16 bits of serial input data are latched.
13	CLK	Clock Input. 10MHz maximum rate. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT.
14-17, 20-23	SEG A-G, DP	7-segment drive and decimal point lines that source current to the display.
18	ISET	Connect to V+ through a resistor (R_{SET}) to set the peak segment current (Refer to "*Selecting R_{SET} Resistor*" section).
19	V+	Supply Voltage
24	DOUT	Serial Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later.

Serially Interfaced, 8-Digit LED Display Driver

Block Diagram

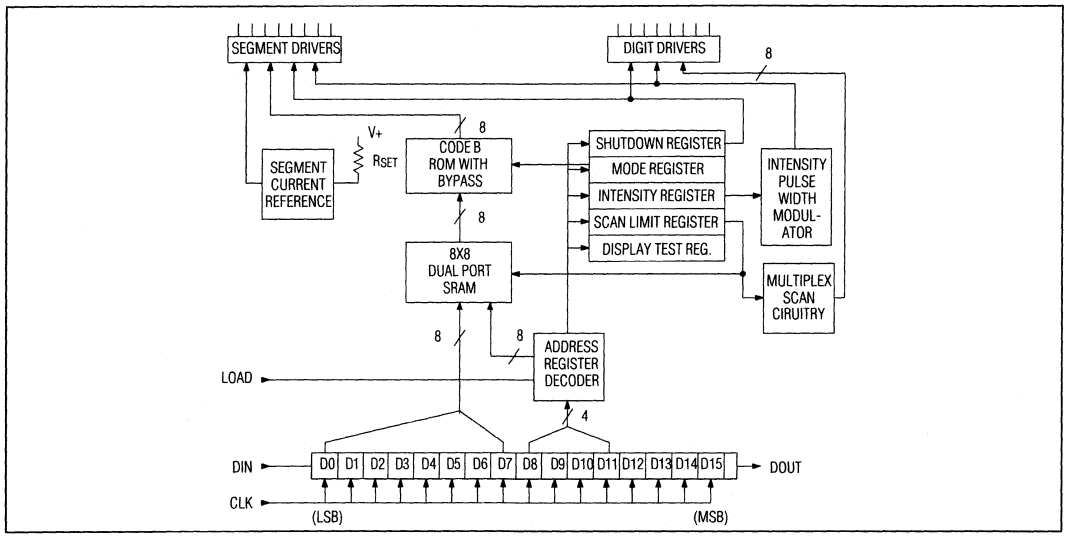


TABLE 1. SERIAL DATA FORMAT (16 BITS)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB	DATA						LSB

X = "don't care" bit

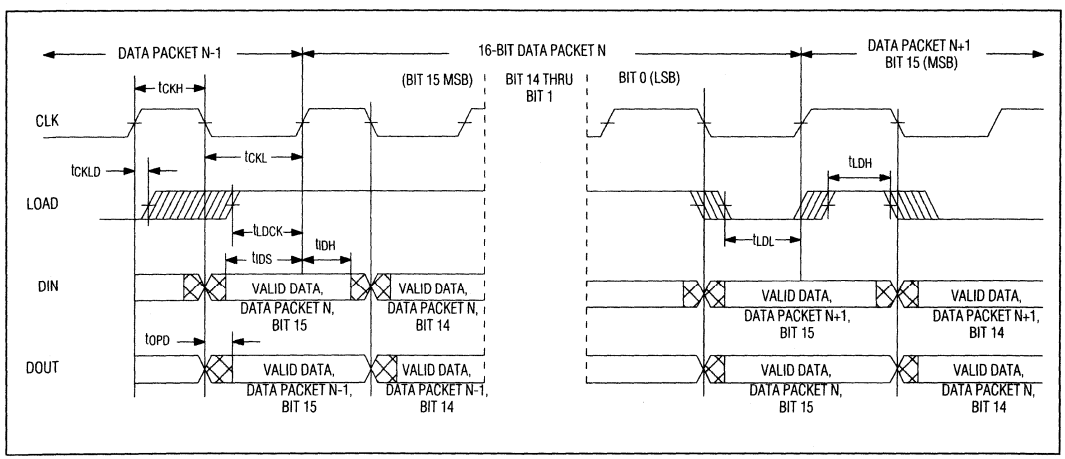


Figure 1. Timing Diagram

Detailed Description

Serial Addressing Modes

Serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK. The data is then latched into either the digit or control registers on the rising edge of LOAD. LOAD must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0-D15 (Table 1). D8-D11 contain the register address, D0-D7 contain the data, and D12-D15 are "don't care" bits. The first bit received is D15, the most significant bit (MSB).

Digit and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip, 8x8 dual-port SRAM. They are addressed directly so that individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of: decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on). A no-operation (no-op) register is also included, which allows data to be passed from DIN to DOUT when devices are cascaded without changing the display or affecting any control registers.

Shutdown Mode

When the MAX7219 is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving the shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS logic levels).

Typically, it takes less than 250µs for the MAX7219 to leave shutdown mode. Note that the display driver can still be programmed while in shutdown mode, and that shutdown mode can be overridden by the display-test function.

Table 3. Register Address Map

REGISTER	D15-D12	D11	ADDRESS D10	D9	D8	HEX CODE
NO-OP	X	0	0	0	0	X0
DIGIT 0	X	0	0	0	1	X1
DIGIT 1	X	0	0	1	0	X2
DIGIT 2	X	0	0	1	1	X3
DIGIT 3	X	0	1	0	0	X4
DIGIT 4	X	0	1	0	1	X5
DIGIT 5	X	0	1	1	0	X6
DIGIT 6	X	0	1	1	1	X7
DIGIT 7	X	0	0	0	0	X8
DECODE MODE	X	1	0	0	1	X9
INTENSITY	X	1	0	1	0	XA
SCAN LIMIT	X	1	0	1	1	XB
SHUTDOWN	X	1	1	0	0	XC
DISPLAY TEST	X	1	1	1	1	XF

Table 3. Shutdown Register Format (Address (Hex) = XC)

	ADDR CODE (HEX)	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0
SHUTDOWN MODE	XC	X	X	X	X	X	X	X	0
NORMAL OPERATION	XC	X	X	X	X	X	X	X	1

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX7219 enters shutdown mode. Therefore the user must program the display driver prior to display use since it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H, L, P, and –) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while a logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

Serially Interfaced, 8-Digit LED Display Driver

Table 4. Decode-Mode Register Examples (Address (Hex) = X9)

	REGISTER DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
NO DECODE FOR DIGITS 7-0	0	0	0	0	0	0	0	0	00
CODE B DECODE FOR DIGIT 0 NO DECODE FOR DIGITS 7-1	0	0	0	0	0	0	0	1	01
CODE B DECODE FOR DIGITS 3-0 NO DECODE FOR DIGITS 7-4	0	0	0	0	1	1	1	1	0F
CODE B DECODE FOR DIGITS 7-0	1	1	1	1	1	1	1	1	FF

Table 5. Code B Font

7-SEGMENT CHARACTER	REGISTER DATA							ON SEGMENTS = 1						
	D7*	D6-D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
-		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

* The decimal point is set by bit D7 = 1

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3-D0), disregarding bits D4-D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7=1 turns the decimal point on). The code-B font is listed in Table 5.

Intensity Control and Interdigit Blanking

The MAX7219 allows the display brightness to be controlled with an external resistor (R_{SET}) connected between V+ and ISET, and digitally using the intensity register. The peak current sourced from the segment drivers will nominally be 100 times the current entering ISET. This resistor can either be fixed, or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53kΩ, which typically sets the segment current at 37mA.

Digital control of segment current is provided by an internal pulse-width modulated DAC, which is loaded from the lower nibble of the intensity register. The DAC scales the average segment current in 16 steps from a maximum of 31/32, down to 1/32 of the peak current set by R_{SET}. The intensity register format is listed in Table 6. Maximum brightness occurs with a duty cycle of 31/32 because the interdigit blanking time is set to 1/32 of a cycle. Interdigit blanking time can be increased by decreasing the duty cycle.

Table 6. Intensity Register Format (Address (Hex) = XA)

DUTY CYCLE	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
1/32 (min on)	X	X	X	X	0	0	0	0	X0
3/32	X	X	X	X	0	0	0	1	X1
5/32	X	X	X	X	0	0	1	0	X2
7/32	X	X	X	X	0	0	1	1	X3
9/32	X	X	X	X	0	1	0	0	X4
11/32	X	X	X	X	0	1	0	1	X5
13/32	X	X	X	X	0	1	1	0	X6
15/32	X	X	X	X	0	1	1	1	X7
17/32	X	X	X	X	1	0	0	0	X8
19/32	X	X	X	X	1	0	0	1	X9
21/32	X	X	X	X	1	0	1	0	XA
23/32	X	X	X	X	1	0	1	1	XB
25/32	X	X	X	X	1	1	0	0	XC
27/32	X	X	X	X	1	1	0	1	XD
29/32	X	X	X	X	1	1	1	0	XE
31/32 (max on)	X	X	X	X	1	1	1	1	XF

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 1300Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is $8f_{OSC}/N$, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). The scan-limit register format is listed in Table 7.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the R_{SET} resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation. Table 8 lists the number of digits displayed and the corresponding maximum recommended segment current when the internal digit drivers are used.

Display-Test Register

The display-test register has two modes of operation, normal and display-test. Display-test mode turns all LEDs on by overriding all control and digit registers, including the shutdown register. The data in these registers is not altered. In display-test mode, 8 digits are scanned and the duty cycle is 31/32 . The display-test register format is listed in Table 9.

Table 7. Scan-Limit Register Format (Address (Hex) = XB)

	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
*DISPLAY DIGIT 0 ONLY	X	X	X	X	X	0	0	0	X0
*DISPLAY DIGITS 0 & 1	X	X	X	X	X	0	0	1	X1
*DISPLAY DIGITS 0 1 2	X	X	X	X	X	0	1	0	X2
DISPLAY DIGITS 0 1 2 3	X	X	X	X	X	0	1	1	X3
DISPLAY DIGITS 0 1 2 3 4	X	X	X	X	X	1	0	0	X4
DISPLAY DIGITS 0 1 2 3 4 5	X	X	X	X	X	1	0	1	X5
DISPLAY DIGITS 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	X6
DISPLAY DIGITS 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	X7

* See "*Scan-Limit Register*" text for application.

Table 8. Maximum Segment Current for 1, 2 or 3 Digit Displays

NUMBER OF DIGITS DISPLAYED	MAXIMUM SEGMENT CURRENT
1	10mA
2	20mA
3	30mA

Table 9. Display-Test Register Format (Address (Hex) = XF)

	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0
NORMAL OPERATION	X	X	X	X	X	X	X	0
DISPLAY TEST MODE	X	X	X	X	X	X	X	1

No-Op Register

The no-op register is used when cascading MAX7219s. Connect all devices' LOAD inputs together and connect DOUT to DIN on adjacent MAX7219s. DOUT is a CMOS logic level output that easily drives DIN of a successively cascaded MAX7219. Refer to the "*Serial Addressing Modes*" section for detailed information on serial input/output timing. For example, if four MAX7219s are cascaded, then to write to the fourth chip, send the desired 16-bit word, followed by three no-op codes (hex X0XX, see Table 2). When load goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

Serially Interfaced, 8-Digit LED Display Driver

Applications Information

Supply Bypassing and Wiring

To minimize power-supply ripple due to the peak digit driver currents, connect a 10µF electrolytic and a 0.1µF ceramic capacitor between V+ and GND as close to the device as possible. The MAX7219 should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electromagnetic interference. Also, both GND pins must be connected to ground.

Selecting R_{SET} Resistor and Using External Drivers

The current per segment is approximately 100 times the current in ISET. To select R_{SET}, see Table 10. The MAX7219's maximum allowable segment current is 40mA. For an LED forward voltage drop of 2.5V, R_{SET} must be greater than 9.53k. For segment current levels above the MAX7219 limits, external drivers will be needed. In this application, the MAX7219 serves as only a controller for other high-current drivers or transistors. Therefore, to conserve power in the MAX7219, use R_{SET} = 47k when using external current sources as segment drivers.

The example in Figure 2 uses the MAX7219's segment drivers, a MAX333 single-pole double-throw analog switch, and external transistors to drive 4.0" AND4107SCL common-cathode displays. The 5.6V zener diode has been added in series with the decimal point LED because the decimal point LED forward voltage is typically 4.2V, while for all other segments the LED forward voltage is typically 8V. Note that since external transistors are used to sink current (DIG 0 and DIG 1 are used as logic switches), peak segment currents of 40mA are allowed even though only two digits are displayed. In applications where the MAX7219's digit drivers are used to sink current and fewer than four digits are displayed, see Table 8 which specifies the maximum allowable segment current. R_{SET} must be selected accordingly (see Table 10).

Refer to the "Power Dissipation" section to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 10. RSET vs. Segment Current and LED Forward Voltage

	V_{LED} (V)				
I_{SEG} (mA)	1.5	2	2.5	3	3.5
40	11.3	10.4	9.8	8.9	7.8
30	16.3	15	14	12.9	11.4
20	26.2	24.6	22.8	20.9	18.6
10	60.1	56	51.7	47	41.9

Table 11. Package Thermal Resistance Data

PACKAGE	THERMAL RESISTANCE (θ_{JA})
24 Narrow DIP	+75°C/W
24 Wide SO	+85°C/W
24 CERDIP	+60°C/W
Maximum Junction Temperature (T_J) = +150°C	
Maximum Ambient Temperature (T_A) = +85°C	

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX7219 is determined from the following equation:

$$PD = (V+ \times 8mA) + (V+ - V_{LED})(DUTY \times I_{SEG} \times N)$$

where:

V+ = Supply Voltage

DUTY = Duty Cycle set by intensity register

N = number of segments driven (worst case is 8)

V_{LED} = LED forward voltage

I_{SEG} = Segment Current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V at 40mA, V+ = 5.25V

$$PD = 5.25V(8mA) + (5.25V - 1.8V)(31/32 \times 40mA \times 8)$$
$$= 1.11W$$

Thus, for a CERDIP package (θ_{JA} = +60C°/W), the maximum allowed ambient temperature T_A is given by:

$$T_J max = T_A + PD \times \theta_{JA}$$
$$+150°C = TA + 1.11W \times +60°C/W$$
$$T_A = +83.4°C$$

Cascading Drivers

The example in Figure 3 drives 16 digits using a 3-wire µP interface. If the number of digits is not a multiple of 8, set both drivers' scan-limit registers to the same number so one display will not appear brighter than the other. For example, if 12 digits are needed, use 6 digits per display

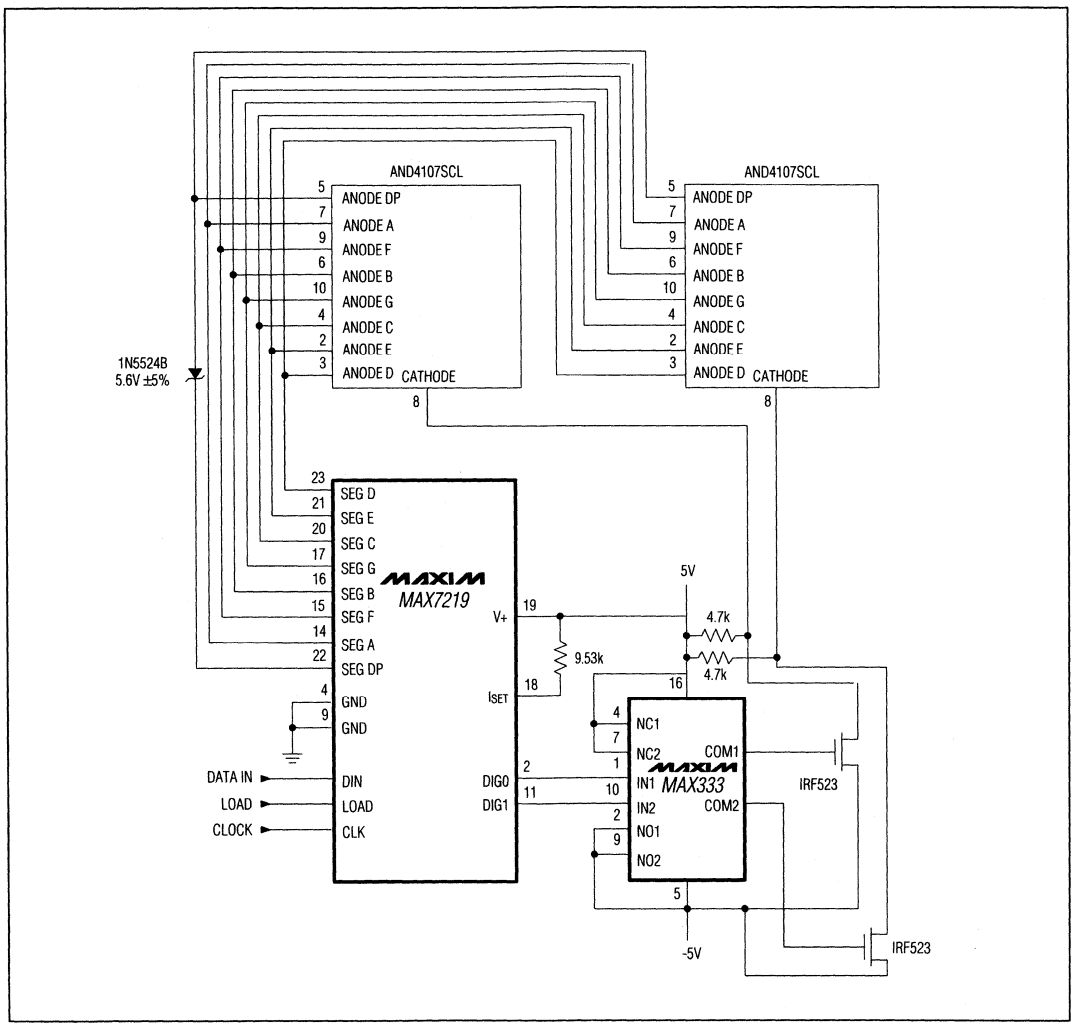


Figure 2. MAX7219 Driving 4 Inch Displays

Serially Interfaced, 8-Digit LED Display Driver

with both scan-limit registers set for 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both scan-limit registers for 6 digits and leave one digit driver unconnected. If one display is set for 6 digits and the other for 5 digits, the second display will appear brighter because its duty cycle per digit will be 1/5 while the first display's will be 1/6. Refer to the "No Op Register" section for additional information.

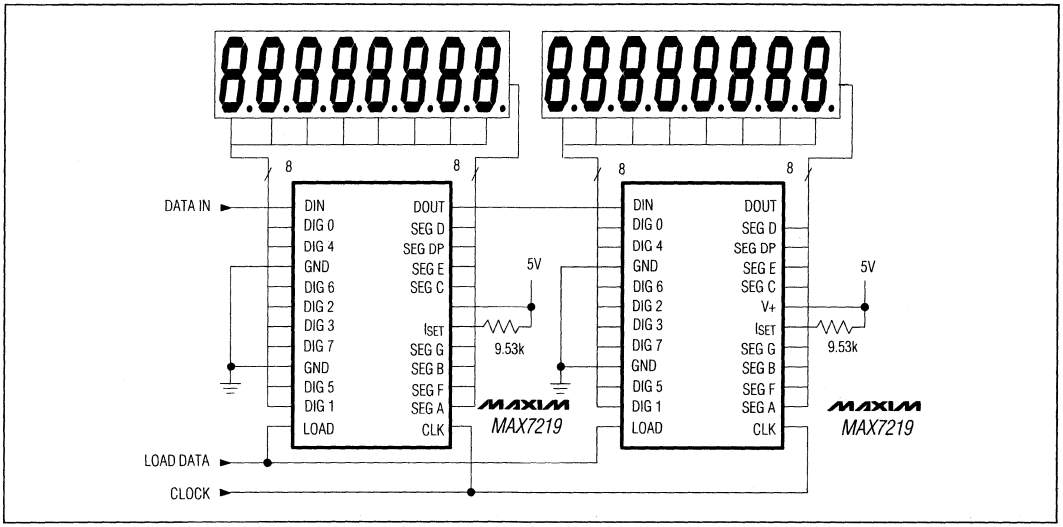
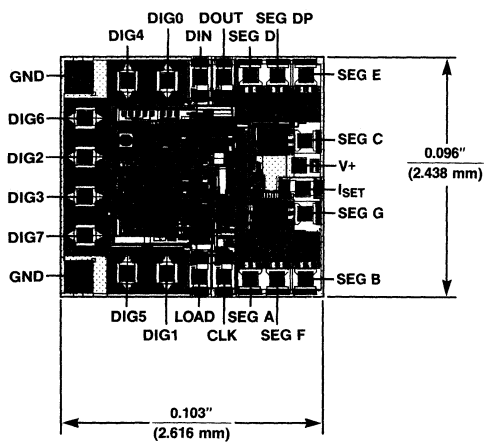


Figure 3. Cascading MAX7219s to drive 16 7-segment LED digits.

Chip Topography



Appendix

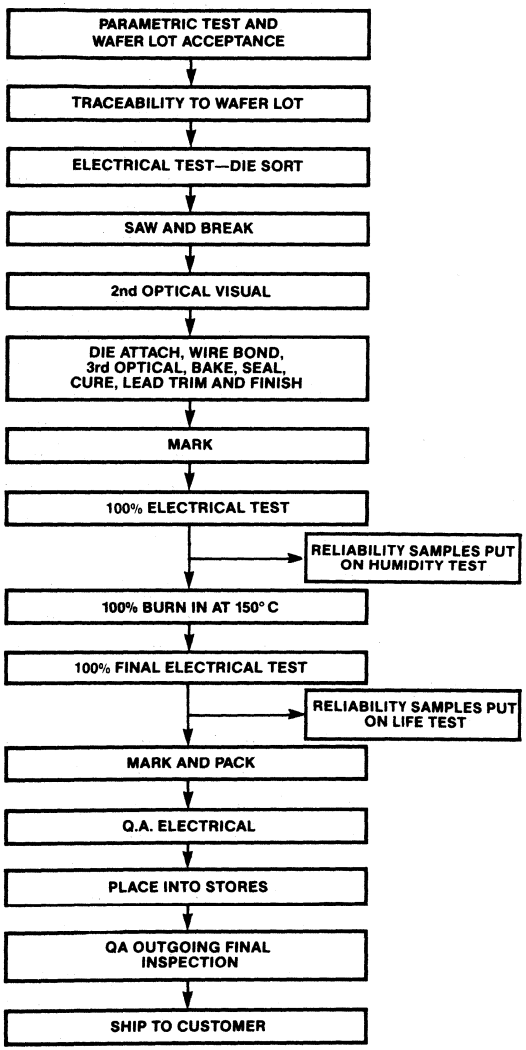
A

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below IpA current levels, and less than IpF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.



Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature.* This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85°C/85%) cycles. In addition, *every unit shipped has been burned-in* (with the exception of reversed lead and Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including a 100% burn-in, at no additional cost.*

Maxim is committed to providing high quality, high reliability 8 to 60 lead plastic surface mount products. With few exceptions, every monolithic product will be offered in a surface mount package. These products are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels, with the exception of 100% burn-in and cold test. They receive the same product conditioning and lot qualification as the DIPs. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a long term life test prior to shipment.

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout as in the 0.300" DIP package equivalents.

0.300" JEDEC SOIC (W) parts also have the same pinout as in the 0.300" DIP package except for selected products in the 16 lead. 14 lead products that are too large for the 0.150" 14 lead (S) package are made available in the 0.300" 16 lead (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-lead products assembled in either 44-lead or 60-lead flatpack. Consult product marketing for specific pin-outs.

Quad Pack Pin Convention

1.) Devices in the 28 Lead Quad Pack are pin for pin number compatible with the DIP package. That is to say, pin 1 on the 28L Quad will be the same function as pin 1 on the DIP package.

2.) All 40 Lead devices planned for the 44 Lead Quad pack will have the following pin convention:

DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#
	1 N/C		12 N/C		23 N/C		34 N/C
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

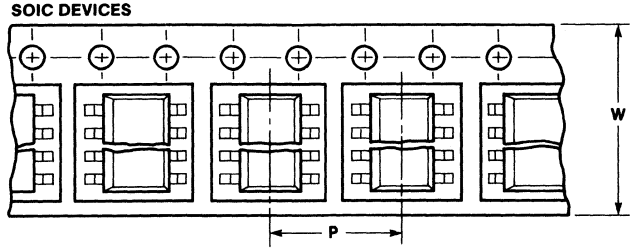
Surface Mount Packages In Reeled Tape

Maxim surface mount packages are normally shipped in antistatic plastic rails. They are also available mounted in pockets on embossed tape for customers using automatic placement systems. The tape is wound and shipped on reels.

The following table and diagrams indicate the tape sizes used for the various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
PFP	44L	24	16
	60L	44	32

SOIC DEVICES



USER DIRECTION OF FEED

A

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow" the standard to ensure lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet 25°C worst case parameters.

Generally, the parameters or parameter limits listed in the packaged unit data sheets are tested during electrical probe. However some parameters are impossible to test or test with absolute accuracy on unassembled product. Information regarding any of these parameters/parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	3"	4"	UNITS
Chip Thickness Backlapped wafers	13 ± 1	15 ± 1	mils
Die length/width tolerance	± 1		mils
Bonding pads dimensions (minimum)	4.0 x 4.0		mils
Bonding pad and interconnect material thickness	10K-15K		A
Storage temperature	-40 to +150		°C
Operating temperature	-20 to +70		°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010.2, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by HF etching or by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

Maxim guarantees die and wafer AQL levels as follows:

Visual 1.0%
Functional Electrical Testing 0.65%
Parametric DC Testing 2.5%
Untested Parameters 6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry ambient—preferably inert gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment or harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Die and wafers are packaged as shown in Figures 1 and 2, respectively.

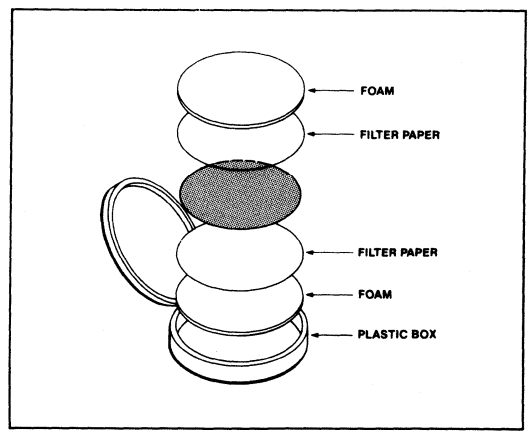


Figure 1. Wafer Carrier Package

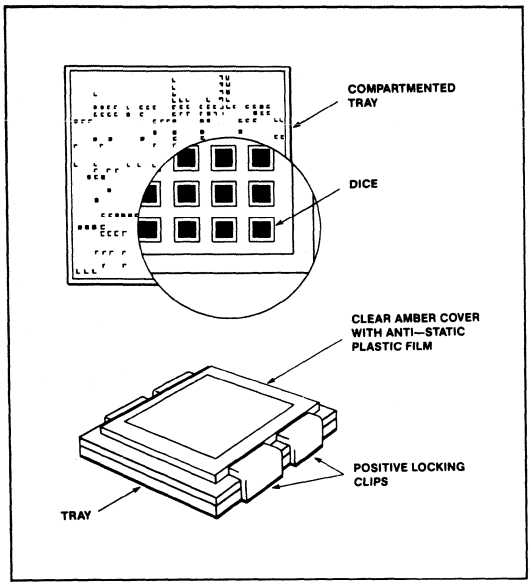


Figure 2. Die Carrier Package

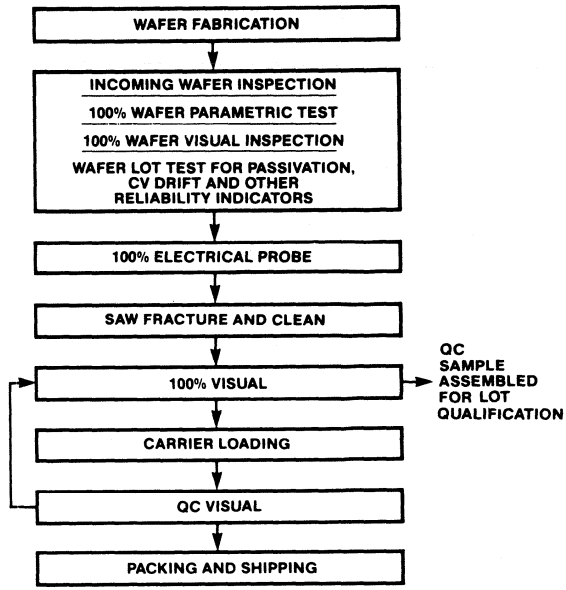
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a /D suffix.
Example: ICL7109C/D

When ordering die in wafer form replace "D" in the part numbers with a "W"
Example: MAX7231C/D Die = MAX7231C/W Wafer.

A

Maxim's /883 and /HR Program

883 PROGRAM

As of July 1st, 1988, Maxim is a certified manufacturer of Mil-Std-883, Class B, Rev. C product. Becoming a manufacturer capable of processing product to 883 requirements entails operator training, equipment calibration, documentation, design baselines etc., that are intangible and transparent for the product. In addition to factory certification, every device must be individually certified and qualified.

In summary, this program produces devices that are tested to operate over the military temperature range (-55°C to +125°C) and are meticulously processed per Mil. Method 5004. Finally, the 883 device manufacturing lots are subjected to Quality Conformance inspection per Mil. Method 5005 (Groups A, B, C, and D testing). Once a manufacturing lot has been processed through these two stringent methods, it is ready for sale as /883 compliant product.

HR PROGRAM

Prior to the inception of the 883 program, Maxim offered its products in an /HR (High Reliability) Flow. Maxim will continue to offer this highly successful processing program for customers requiring military grade product, but who do not want to pay the substantial cost added for certified product in full compliance to Mil-Std-883. The /HR program offers device processing which emulates Mil. Method 5004 processing, including full material traceability and process genealogy from Incoming Raw Materials through Final Shipment. However, full QCI testing will not be performed unless requested. Only Group A of Mil. Method 5005 will be done per lot. Groups B, C, and D must be specifically requested during order placement. This is done simply by placing a single letter suffix (B, C, or D) at the end of the ordered part number (see chart).

Ordered Part #	Processing
MAX358MJE/HR	Device will be processed through the full /HR Flow emulating Mil Method 5004 and QCI tested to Group A of Mil Method 5005.
MAX358MJE/HRB	Same as above with the addition of Mil Method 5005 Group B testing. QCI contains both Group A and B.
MAX358MJE/HRC	Same as above except now QCI includes Group C. QCI now contains Groups A, B, and C.
MAX358MJE/HRD	Same as above except now QCI includes Group D. QCI now contains Groups A, B, C, and D.

To order /883 or /HR devices, contact the Maxim sales representative or distributor in your area.

Maxim's Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped by their functions into certain categories. Maxim presently uses a "MAX" as the prefix to the device's unique number. The categories are as follows:

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op-Amps, Buffers and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power Supply Circuits and Voltage References
MAX700-799	µP Peripherals and Display Drivers
MAX800-899	Open
MAX900-999	Open

Within each category, blocks of numbers are reserved for sub-groups.

3 Letter Suffixes

EXAMPLE: MAX358CPD

- C — Operating Temperature
- P — Package Designator
- D — Lead Count

Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	TO-237
"C"	TO-220
"D"	Ceramic Sidebraze
"F"	Ceramic Flat-Pack
"H"	TO-66
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP (24 pin, 0.3" wide)
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71)
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Z"	TO-92
"/D"	Dice
"/W"	Wafer
"-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8	"P"	20
"B"	10	"Q"	2
"C"	12	"R"	3
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44		
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32		
"L"	40	"Y"	8 (0.200" pin circle, case to pin 4)
"M"	48		
"N"	18	"Z"	10 (0.230" pin circle, case to pin 5)

4 Letter Suffixes

The first letter of the suffix is used to denote product grade, for example, MAX631ACPA means 5% output accuracy (A), the remaining 3 letters denote temperature range, package type and number of leads. Therefore, the MAX631ACPA operates over the 0°C to +70°C and is in a Plastic Dual-in-Line package and has 8 leads.

Second Source Products

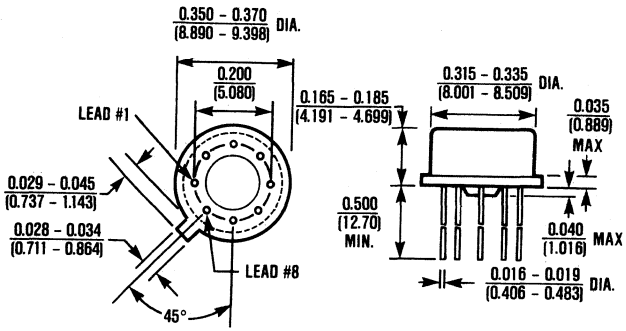
In most cases, Maxim's part number for a multiple source product follows the numbering system that is most widely accepted in the industry for that particular part, rather than our own convention. This includes original designators for package type, temperature range, and performance grades as well as the most commonly recognized prefix.

Multiple source products are frequently supplied by Maxim in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, such a device is given the part number that it would have if the original numbering convention were followed. For example, if a military temperature grade of a product is not supplied by other sources but is available from Maxim, the original manufacturer's designation for military temperature will be used. As a result, a specific part number supplied by Maxim may not be listed by the "original" manufacturer.

Package Information

This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two letter code which indicates package type (Plastic DIP, Small Outline, etc.) and number of leads. This code is also used, along with indicators for temperature range and device grade (where appropriate) in the part number suffix for each of Maxim's proprietary devices.

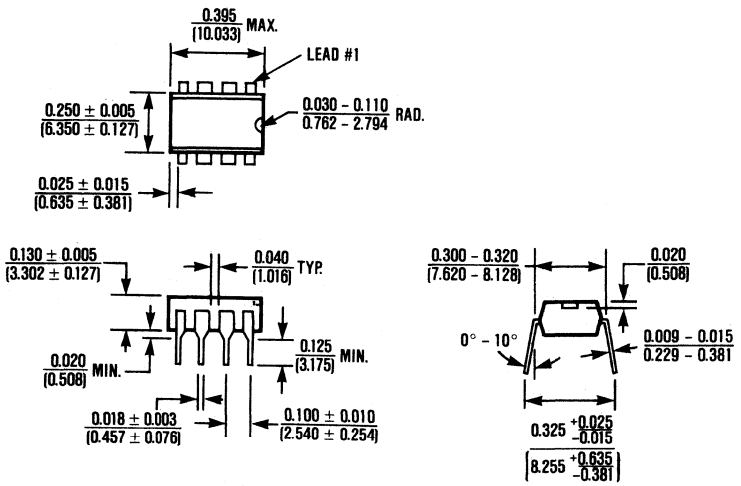
A



8 Lead TO-99

θ_{JA} = 150°C/W

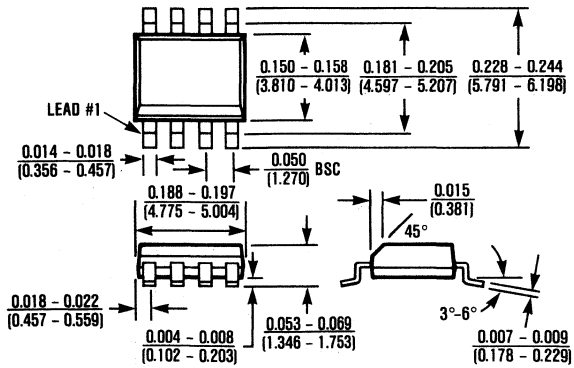
θ_{JC} = 45°C/W



8 Lead Plastic DIP

θ_{JA} = 120°C/W

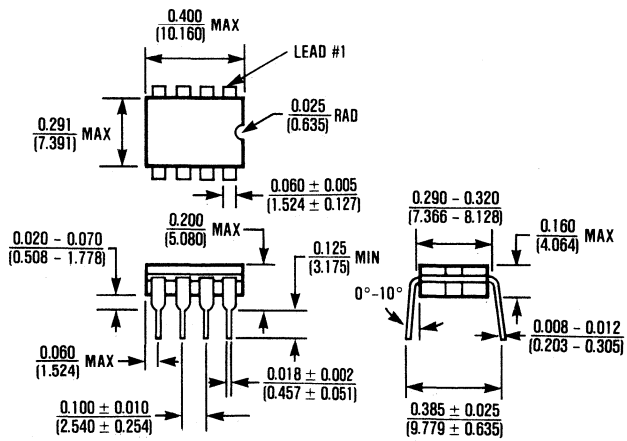
θ_{JC} = 70°C/W



8 Lead Small Outline

θ_{JA} = 170°C/W

θ_{JC} = 80°C/W

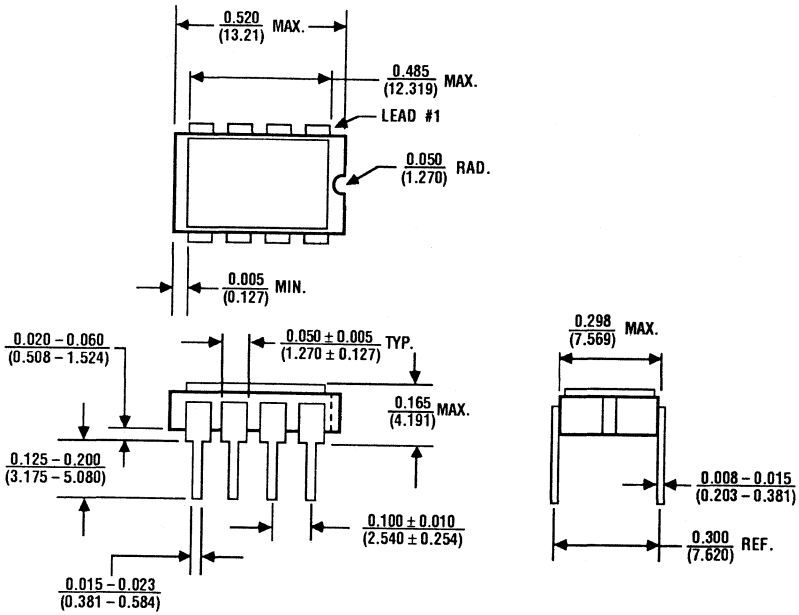


8 Lead CERDIP

θ_{JA} = 125°C/W

θ_{JC} = 55°C/W

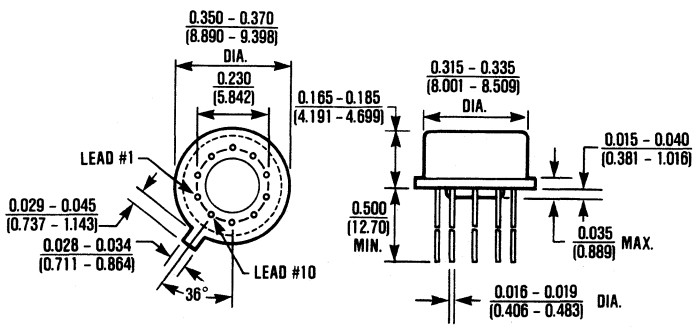
A



8 Lead Ceramic Sidebraze

θ_{JA} = 120°C/W

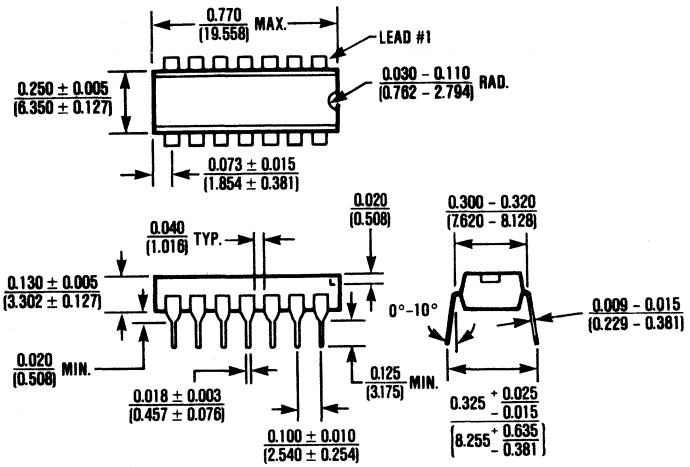
θ_{JC} = 50°C/W



10 Lead TO-100 Can

θ_{JA} = 150°C/W

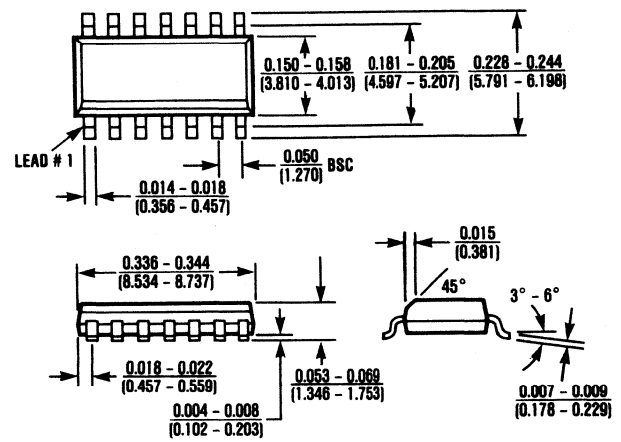
θ_{JC} = 45°C/W



14 Lead Plastic DIP

θ_{JA} = 140°C/W

θ_{JC} = 70°C/W

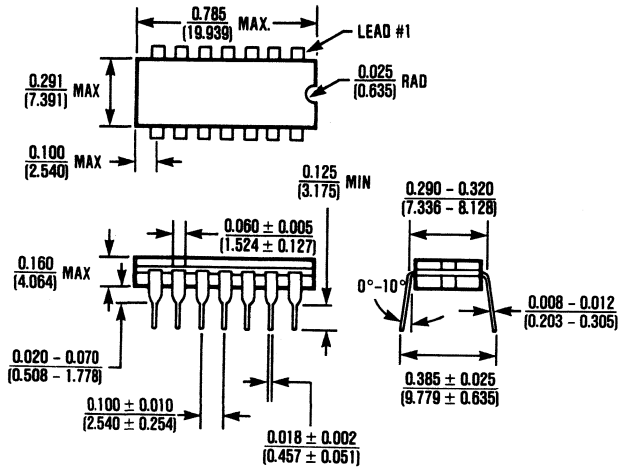


14 Lead Small Outline

θ_{JA} = 115°C/W

θ_{JC} = 60°C/W

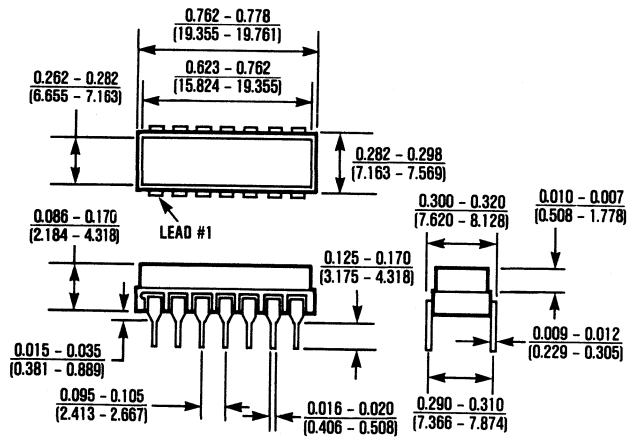
A



14 Lead CERDIP

θ_{JA} = 105°C/W

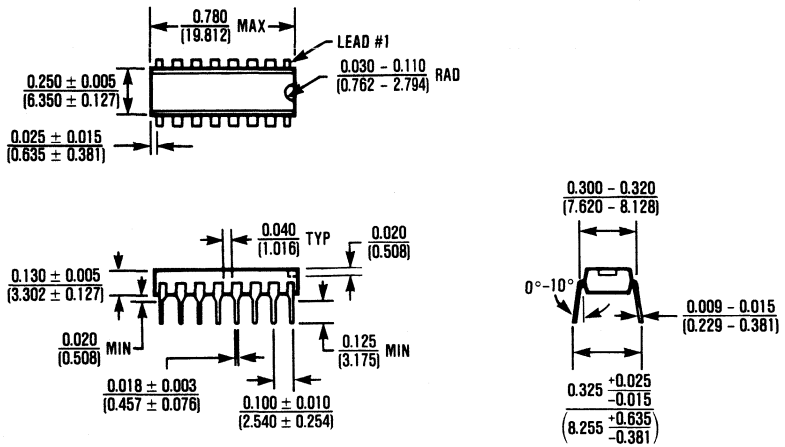
θ_{JC} = 50°C/W



14 Lead Ceramic Sidebraze -1

θ_{JA} = 100°C/W

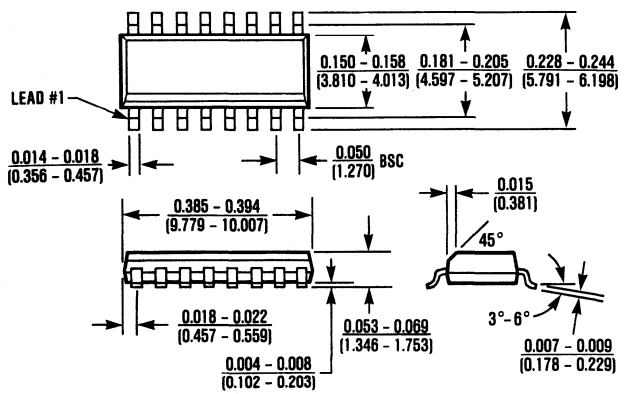
θ_{JC} = 45°C/W



16 Lead Plastic DIP

θ_{JA} = 135°C/W

θ_{JC} = 65°C/W

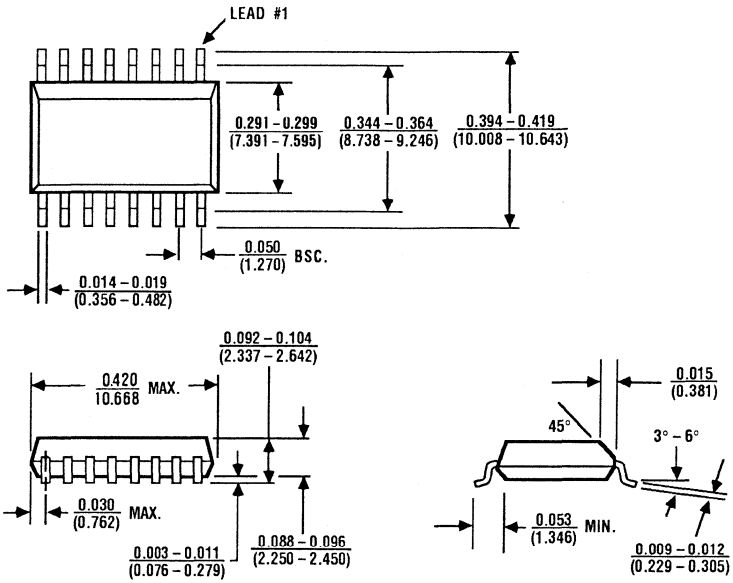


16 Lead Small Outline

θ_{JA} = 110°C/W

θ_{JC} = 60°C/W

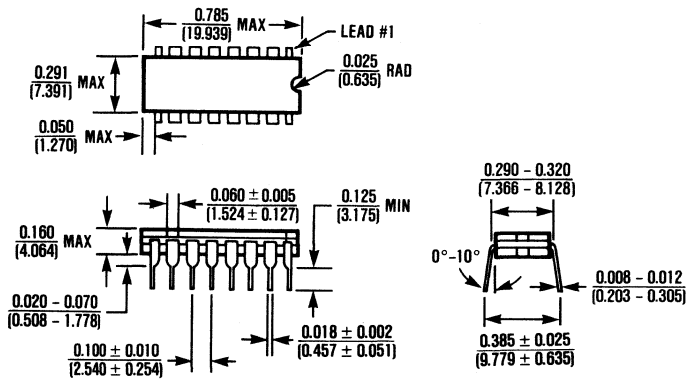
A



16 Lead Small Outline, Wide

θ_{JA} = 105°C/W

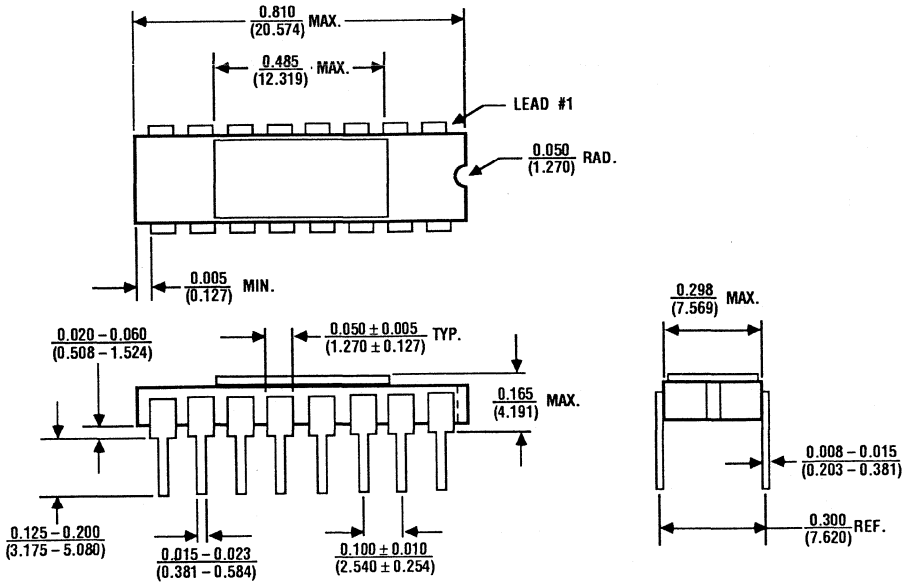
θ_{JC} = 60° C/W



16 Lead CERDIP

θ_{JA} = 100°C/W

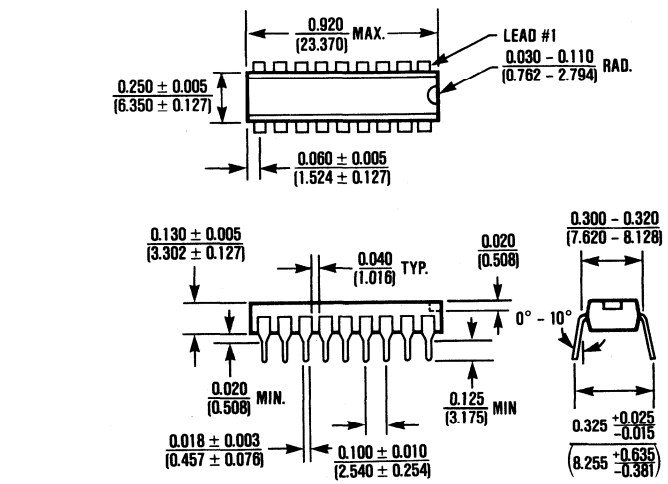
θ_{JC} = 50°C/W



16 Lead Ceramic Sidebraze

θ_{JA} = 95°C/W

θ_{JC} = 45°C/W

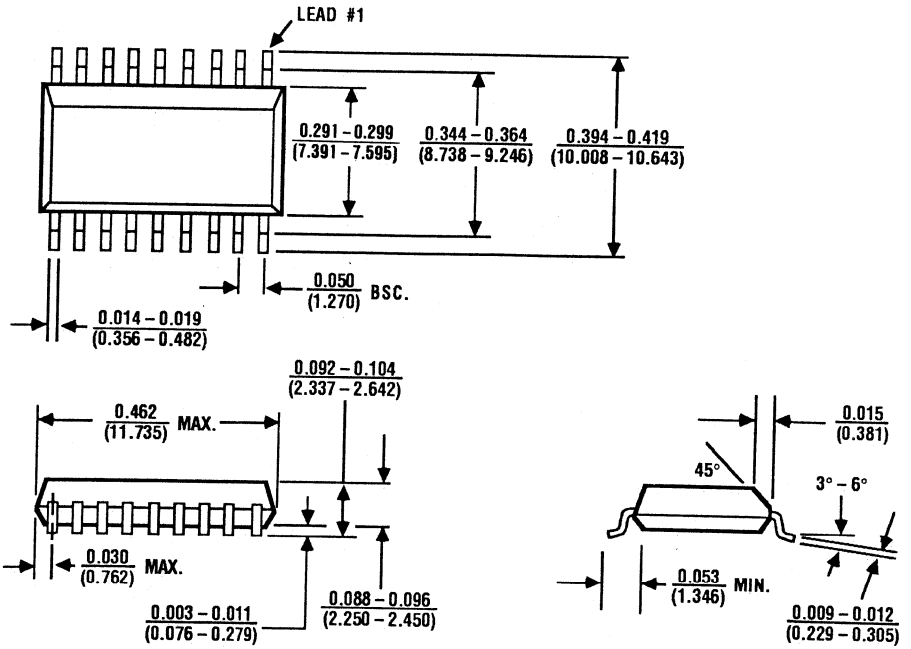


18 Lead Plastic DIP

θ_{JA} = 130°C/W

θ_{JC} = 60°C/W

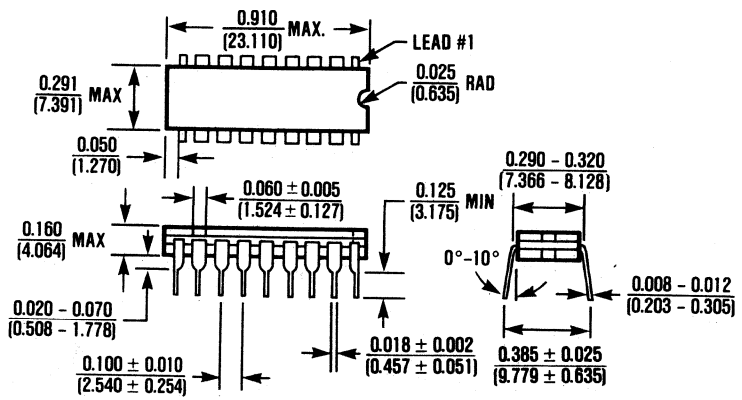
A



18 Lead Small Outline, Wide

θ_{JA} = 105°C/W

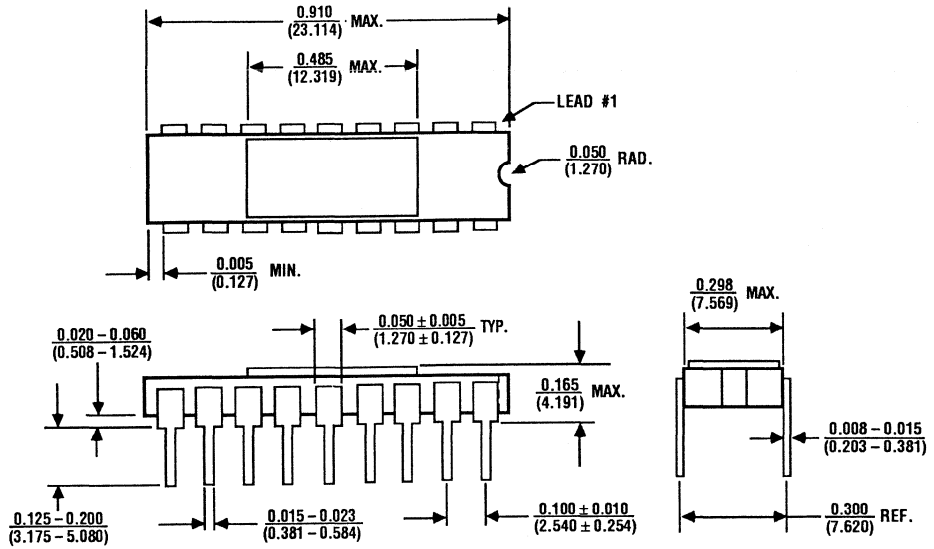
θ_{JC} = 60° C/W



18 Lead CERDIP

θ_{JA} = 90°C/W

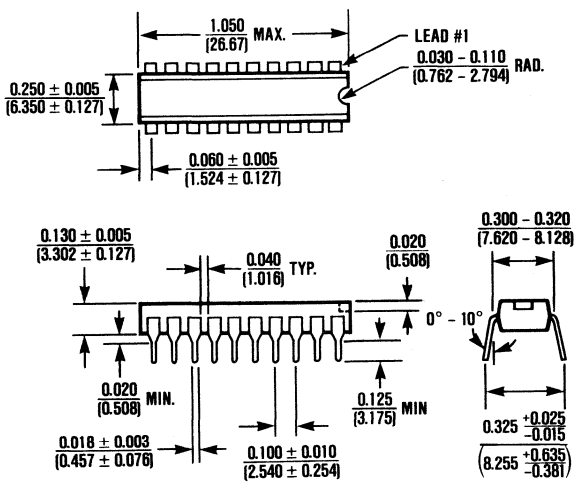
θ_{JC} = 45°C/W



18 Lead Ceramic Sidebraze

θ_{JA} = 90°C/W

θ_{JC} = 40°C/W

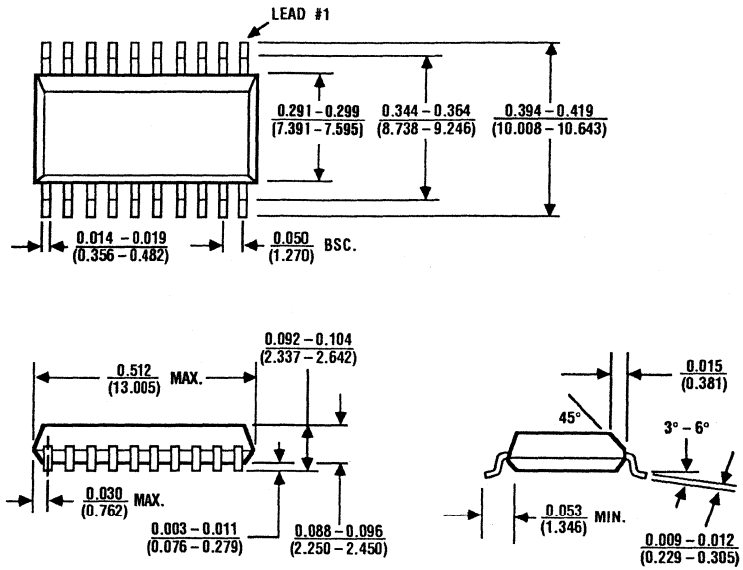


20 Lead Plastic DIP

θ_{JA} = 125°C/W

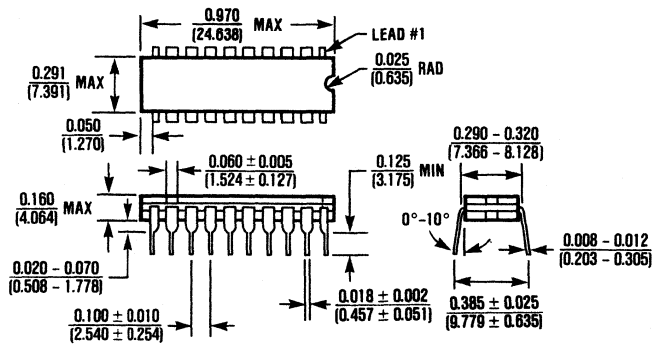
θ_{JC} = 60°C/W

A



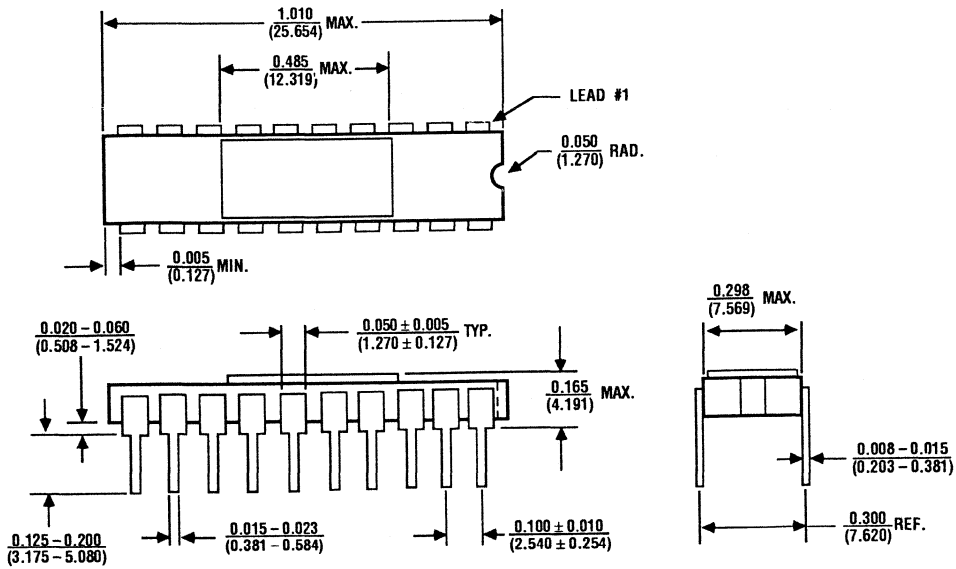
20 Lead Small Outline, Wide

θ_{JA} = 100°C/W
θ_{JC} = 50° C/W



20 Lead CERDIP

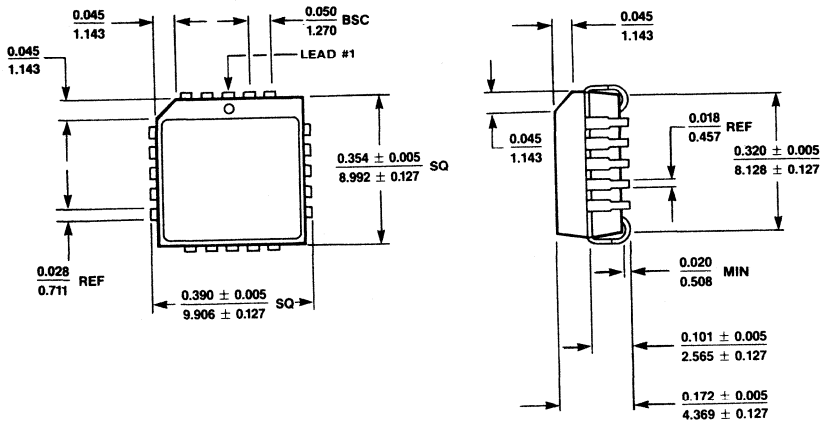
θ_{JA} = 90°C/W
θ_{JC} = 40°C/W



20 Lead Ceramic Sidebraze

θ_{JA} = 85°C/W

θ_{JC} = 35°C/W

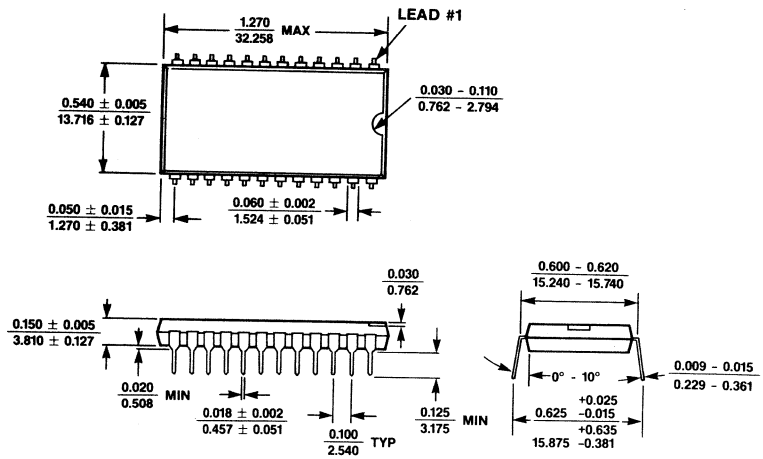


20 Lead Plastic Chip Carrier (Quad Pak)

θ_{JA} = 110°C/W

θ_{JC} = 50°C/W

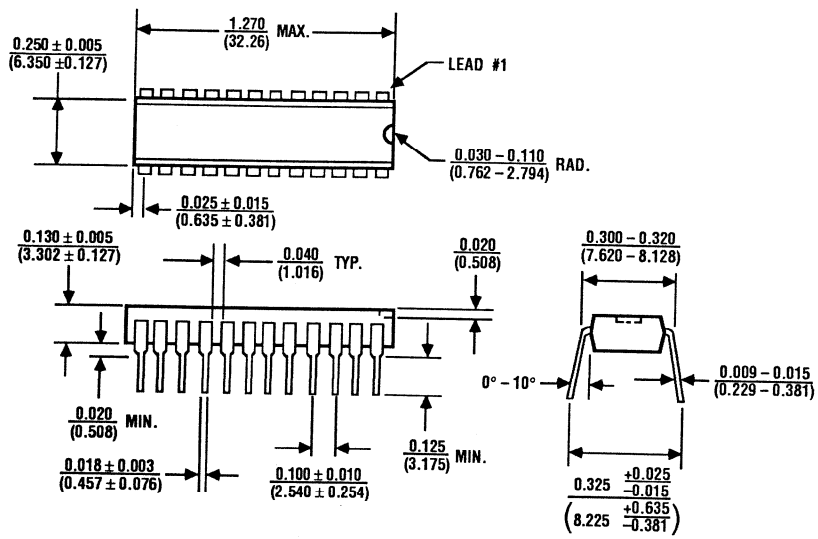
A



24 Lead Plastic DIP

θ_{JA} = 110°C/W

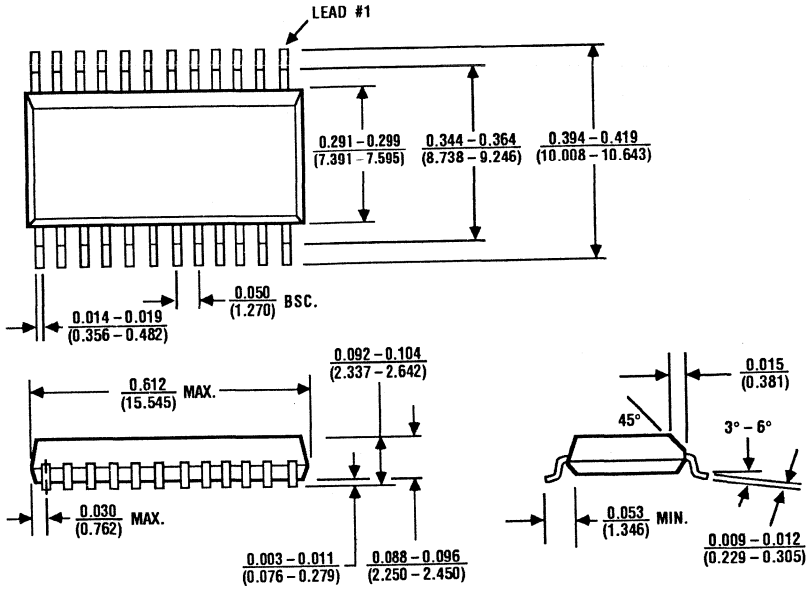
θ_{JC} = 50°C/W



24 Lead Plastic Narrow DIP

θ_{JA} = 120°C/W

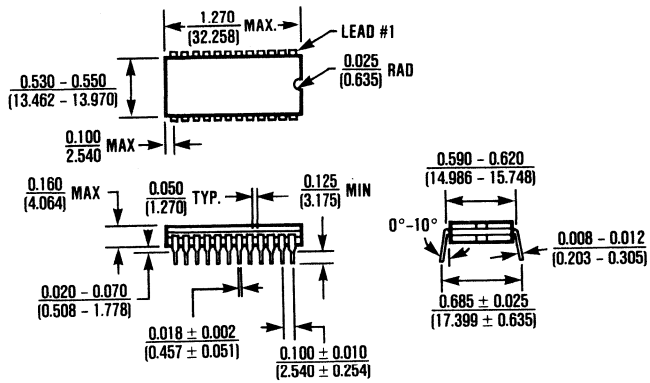
θ_{JC} = 60°C/W



24 Lead Small Outline, Wide

θ_{JA} = 85°C/W

θ_{JC} = 45° C/W

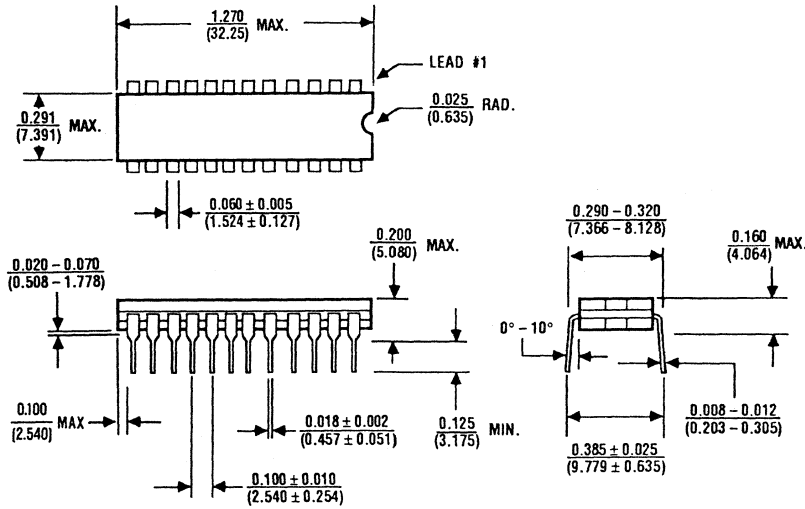


24 Lead CERDIP

θ_{JA} = 55°C/W

θ_{JC} = 20°C/W

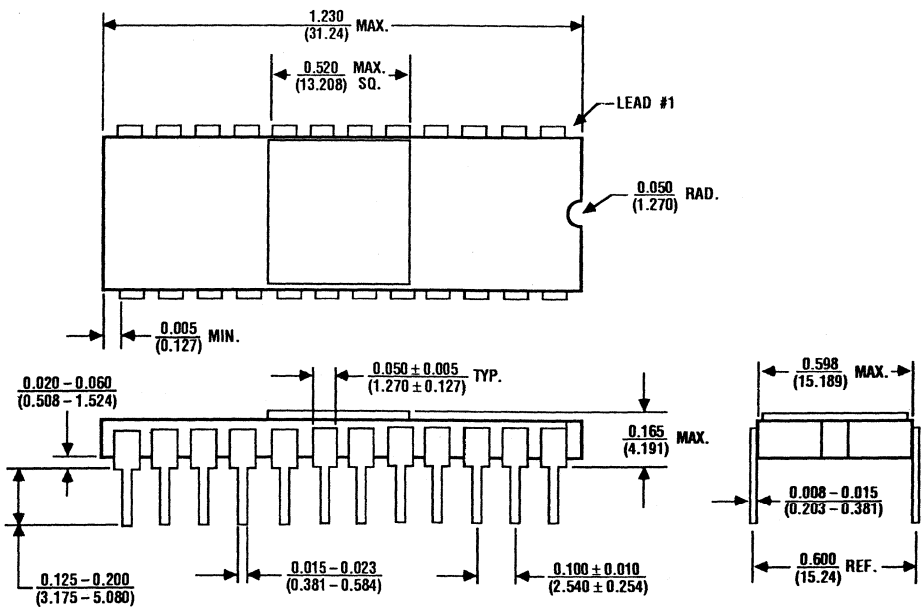
A



24 Lead Narrow CERDIP

θ_{JA} = 80°C/W

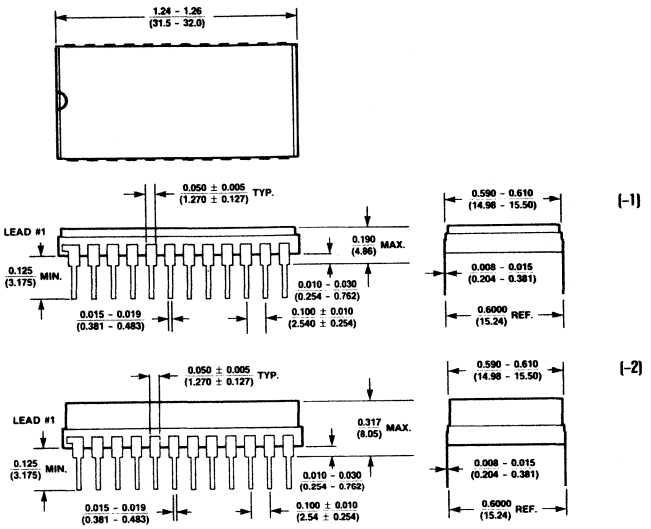
θ_{JC} = 40°C/W



24 Lead Ceramic Sidebraze

θ_{JA} = 50°C/W

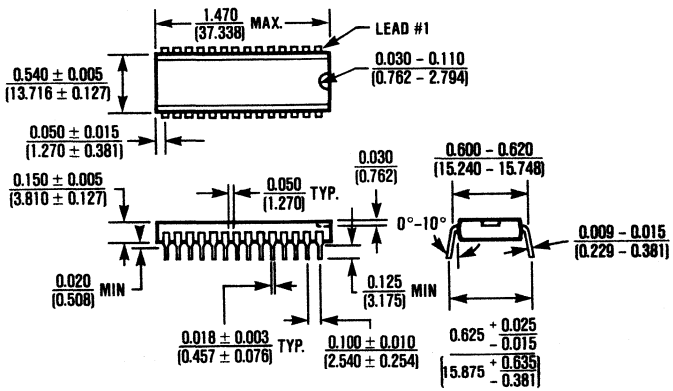
θ_{JC} = 15°C/W



24 Lead Ceramic Sidebraze -1, -2

θ_{JA} = 50°C/W

θ_{JA} = 15°C/W

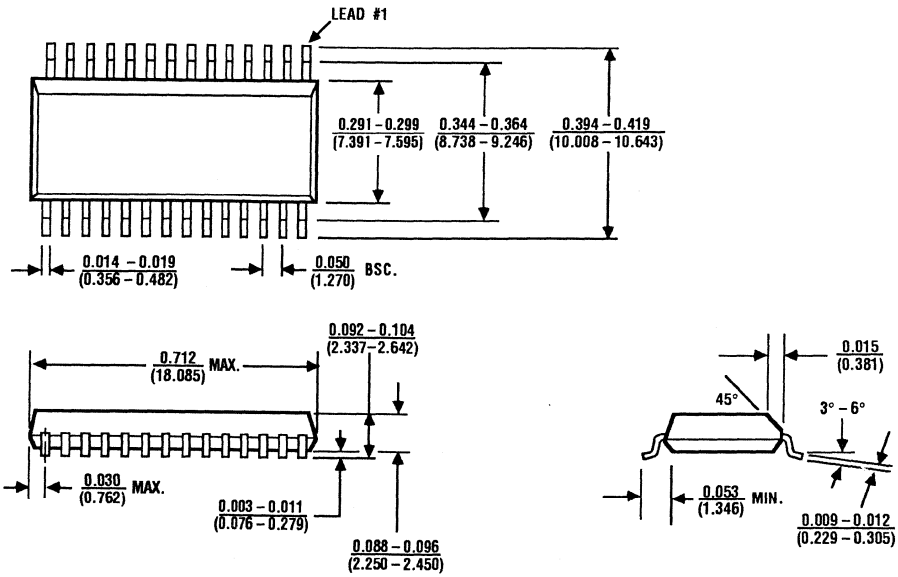


28 Lead Plastic DIP

θ_{JA} = 110°C/W

θ_{JC} = 50°C/W

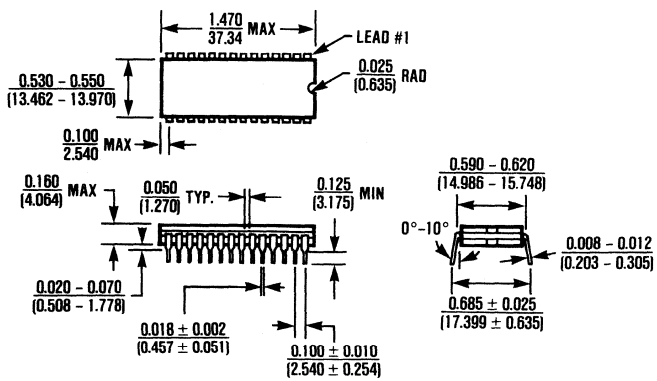
A



28 Lead Small Outline, Wide

θ_{JA} = 80°C/W

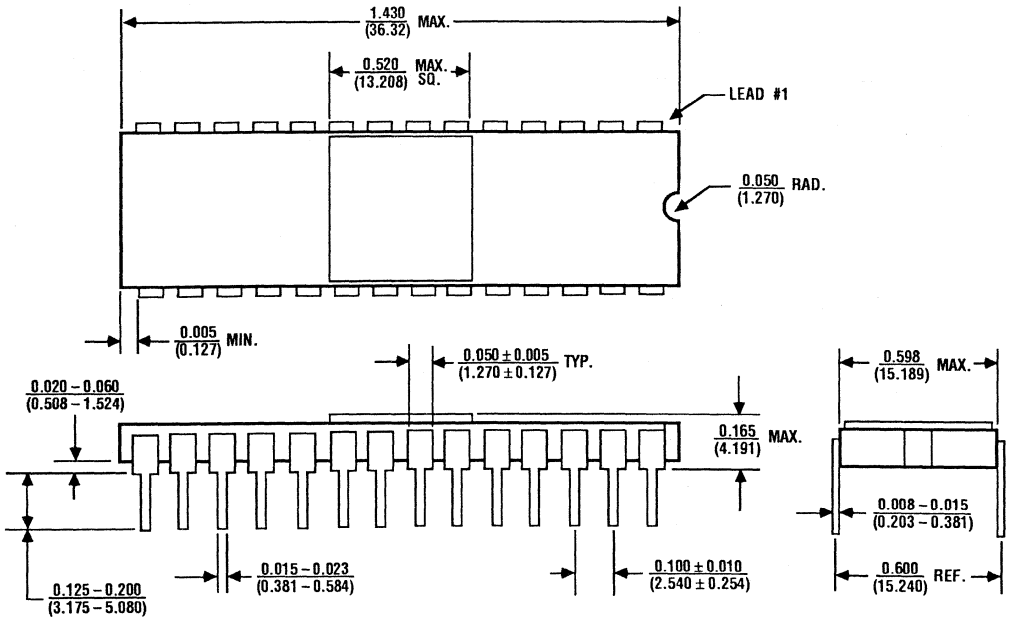
θ_{JC} = 45°C/W



28 Lead CERDIP

θ_{JA} = 55°C/W

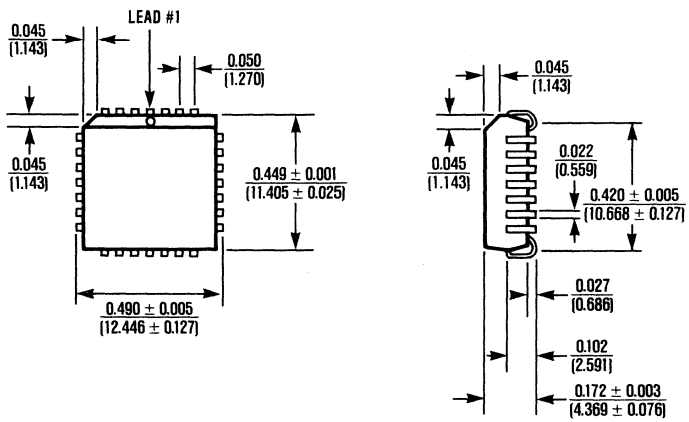
θ_{JC} = 20°C/W



28 Lead Ceramic Sidebraze

θ_{JA} = 50°C/W

θ_{JC} = 15°C/W

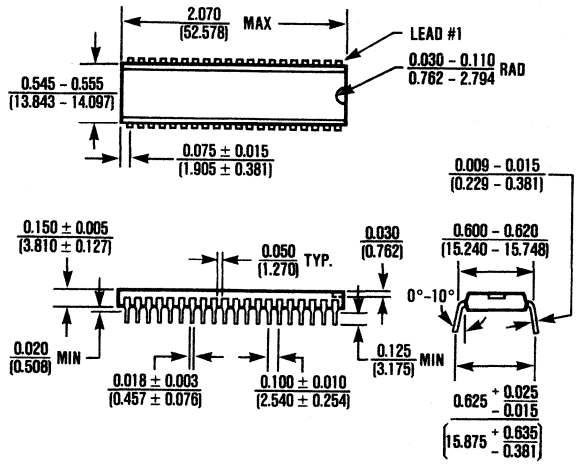


28 Lead Plastic Chip Carrier (Quad Pak)

θ_{JA} = 100°C/W

θ_{JC} = 45°C/W

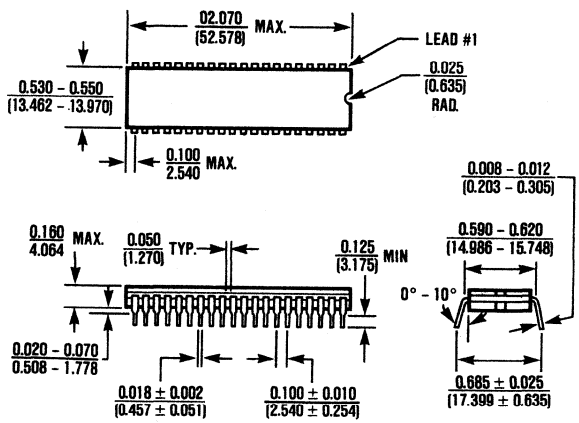
A



40 Lead Plastic DIP

θ_{JA} = 100°C/W

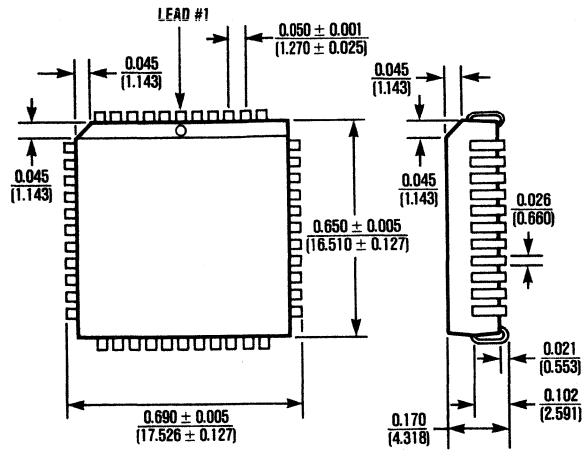
θ_{JC} = 45°C/W



40 Lead CERDIP

θ_{JA} = 45°C/W

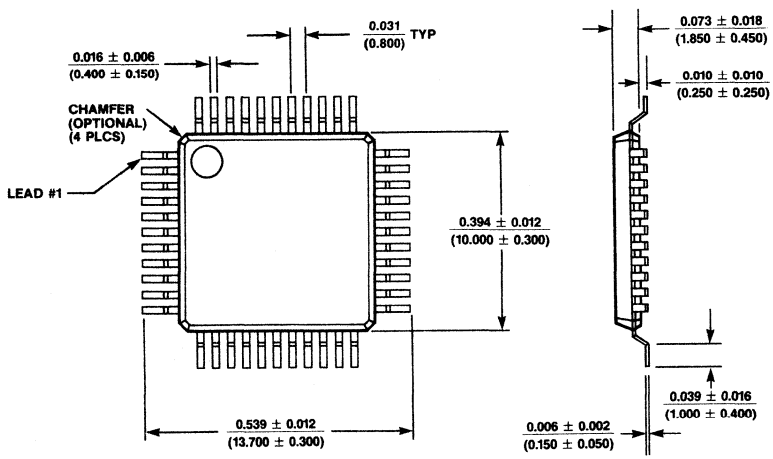
θ_{JC} = 20°C/W



44 Lead Plastic Chip Carrier (Quad Pak)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W



44 Lead Plastic Flat Pack

θ_{JA} = 170°C/W

θ_{JC} = 70°C/W

A